Application Report
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High-Voltage Lifetime of the ISO72x Family of Digital Isolators

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ABSTRACT

This application report examines the high-voltage lifetime characteristics of the isolation barrier in the ISO72x family of digital isolators. This provides the user with information regarding the long-term, high-voltage withstand capability of this family of products.

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1 Introduction

Industrial control systems often use digital isolators where downtime costs are high and reliability is a key concern for suppliers of equipment to this market. Data-sheet specifications adequately cover functional and parametric performance of the isolators, including maximum voltage capability of the isolation barrier for single-event, high-voltage transients. However, these specifications do not sufficiently address the behavior of the isolation properties under long-term application of a high voltage.

This application report provides a long-term prediction of the isolation properties of the ISO72x family of digital isolators when operated with a continuous input to output voltage of 560 V at a junction temperature of 150°C.

This report first defines insulation properties and ratings and then describes the ISO72x isolation barrier. It presents the time-dependent dielectric breakdown (TDDB) model and ISO72x test results.

2 Insulation Properties and Ratings

Dielectrics have intrinsic insulation properties determined by their physical and chemical composition, which includes impurities and imperfections (inclusions) that manufacturing may introduce. It is well understood that these inclusions cause the insulation properties to change over time and result in the eventual failure of the dielectric. These changes are accelerated by applying an electric field across the dielectric and/or by increasing its temperature.

Data-sheet specifications for most digital couplers only include initial ratings. For basic insulation applications, most of the commonly available (including ISO72x family) isolated couplers refer to a 4000-V (V_{IOTM}) rating. Table 1 refers to typical data-sheet ratings provided by the manufacturer. By itself, this rating does not imply that the product can withstand 4000 V if applied for an indefinite time or at an arbitrarily high temperature. In fact, given only this rating, it is impossible to predict the voltage-withstand characteristics over time of such a product which may be subjected to repeated high-voltage strikes on a factory floor environment, for example.

Table 1. Typical Data-Sheet Specifications of Insulation Characteristics

PARAMETER	SYMBOL	MAXIMUM	UNITS
Maximum working insulation voltage	V_{IORM}	560	V peak
Transient overvoltage	V_{IOTM}	4000	V peak
Input-to-output peak test voltage	V_{PR}, Method b	1.875 × V_{IORM}	V peak
	V_{PR}, Method a	1.2 × V_{IORM}	V peak
Insulation resistance	R_{IO}	> 1E9	Ω

The other insulation rating that is of concern is the working voltage (V_{IORM}), or continuous operating voltage. This voltage rating implies that the product retains its insulation properties over the lifetime of the product if it is operated at this voltage applied between the input and output. Usually, semiconductor products last for a minimum of 10 years.

3 ISO72x Device Description

The ISO72x family of products consists of an input and an output semiconductor device separated by a high-impedance isolation barrier designed for the transfer of electrical signals across the barrier. The ISO72x uses capacitive coupling to transmit signals across the barrier while maintaining isolation of the output side with reference to input. The capacitor dielectric is semiconductor-grade silicon dioxide and is the isolation barrier. Figure 1 shows the capacitor is constructed from a top plate consisting of plated copper and a bottom plate made from doped silicon substrate. A BCB (benzocyclobutene) spin-on dielectric passivation over the top plate reinforces the insulation characteristics.

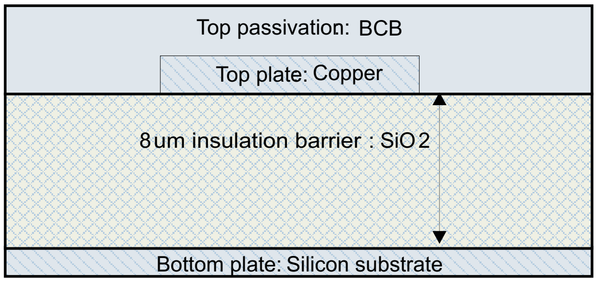
Top passivation: BCB
Top plate: Copper
8um insulation barrier : SiO2
Bottom plate: Silicon substrate

Figure 1. Isolation Barrier for ISO72x Family of Products

4 Modeling and Test Methodology

4.1 The TDDB E-Model for Dielectric Breakdown

Time-dependent dielectric breakdown (TDDB) is an important failure mode for dielectric materials like silicon dioxide (SiO_2). The E-model [1] is the most widely accepted and used model for capacitor breakdown and can be applied to all dielectric thicknesses [2]. The E-model is not only phenomenological [3] but is also backed by a theoretical physical degradation mechanism [4]. The E-model is considered as the most conservative of all models in the literature [5]. More complex systems, such as the one discussed in this document, may experience multiple failure modes, or degradation mechanisms; each of these modes can be modeled with its respective E-model. The sum of all these dielectric degradation rates would determine the overall time to failure.

A capacitor models the input to output of all isolated devices. The capacitor dielectric thickness and material type can vary from product to product. In the ISO72x family of products, this capacitor is part of the active circuit, as opposed to being part of the parasitic circuit in the case of optocouplers or inductive/magnetic-coupled devices.

The lifetime prediction is accomplished by a series of accelerated-stress TDDB testing. According to the E-model, the time to failure (TF) relates to the electric field as Equation 1 shows.

$$\ln(TF) \propto \frac{\Delta H_o}{k_b T} - \gamma Eox \tag{1}$$

where ΔH_o is the enthalpy for oxide breakdown (referred to as activation energy), E_{ox} is the electric field across the isolation barrier, given by the ratio of applied-stress voltage (V_S) to thickness of the insulation barrier, k_b is Boltzmann’s constant, and γ is the field acceleration parameter. The data was taken at 150°C, the worst-case operating condition, to avoid the need for temperature corrections. The only TF acceleration was through applying a higher voltage, V_S. Because V_S is proportional to E_{ox}, and temperature acceleration does not have to be accounted for, a simplified model can be used as is shown in Equation 2.

$$\ln(TF) \propto -MVs \tag{2}$$

where M (voltage acceleration parameter) is a constant proportional to γ. Thus, using Equation 2, the E-model predicts that the relation is exponential, or, if TF is plotted on the y-axis using a log scale and V_S on the x-axis using a linear scale, the relation looks linear on such a plot. In this case, M is the slope of this line.

This line is extrapolated to the operating voltage (V_{IORM}) for lifetime prediction and will always be overly conservative. This is a result of accelerating the testing by applying voltages much higher than the operating voltage. The higher voltages activate additional dielectric-degradation modes leading to an apparent deviation from the E-model. The additional modes, which may not be active at lower voltages, tend to decrease the slope, which results in a lower projected TF.

4.2 Test Methodology

Normally, semiconductor lifetime is studied at the wafer level. However, due to the voltages involved and to get a more accurate analysis of the failure modes of the product, packaged units were used for testing in this application report. Through-hole, dual-in-line packages (DIP) generated artifact-free data in the test setup; therefore, DIP units generated the majority of the data points. Small-outline integrated circuit (SOIC) and DIP devices were tested and analyzed to confirm that the same failure modes were activated. Figure 2 shows the test setup for a device under test (DUT).

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(1) See Reference 1.
(2) See Reference 2.
(3) See Reference 3.
(4) See References 4 and 5.
(5) See References 6 and 7.

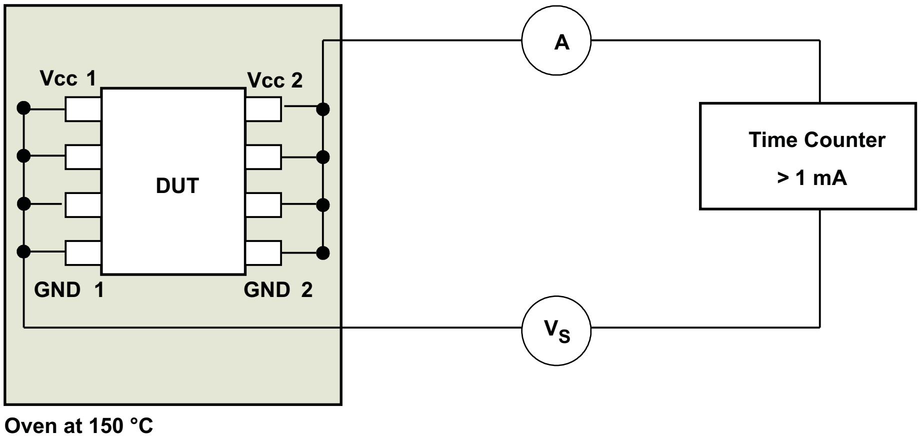


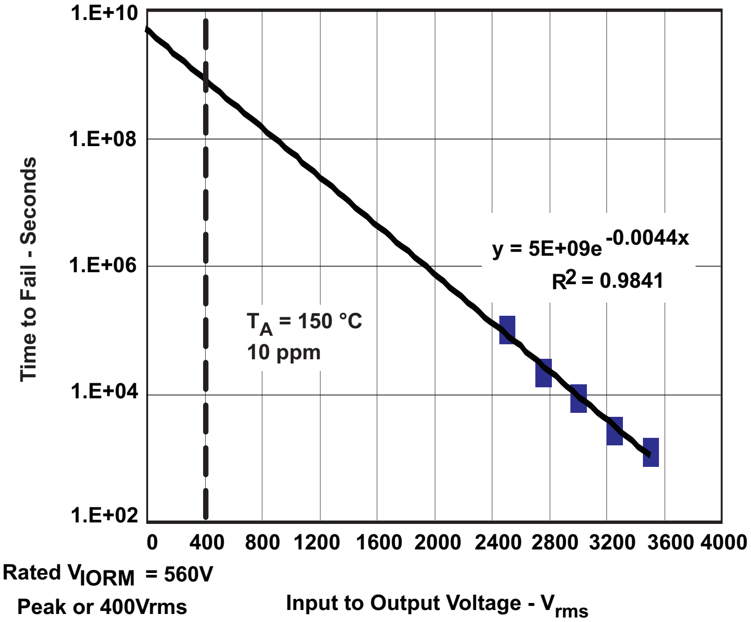
Figure 2. Test Setup for High-Voltage Lifetime

The basic methodology was to apply a stress voltage from the input to the output of the DUT in a two-terminal configuration using a high-voltage source, while maintaining the still-air, ambient-air temperature at 150°C. The start of the test activated a timer; this timer stopped when the current in the circuit exceeded 1 mA, which meant that the dielectric had failed. The TF was noted for each applied test voltage. DUTs were tested independently of each other (one DUT per test) at each test voltage to get statistically valid results.

5 Results

5.1 TDDB E-Model Predictions

The raw data was statistically analyzed using a linearized Weibull (6) plot to determine the worst-case TF; this was extrapolated down to 10-ppm level at each test voltage. The extrapolated TF (10 ppm) is plotted against test voltage in Figure 3.



Rated V_{IORM} = 560V
Peak or 400Vrms
Note: 3E+08 Seconds = 10 years

Figure 3. High-Voltage Lifetime Using TDDB E Model

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(6) See Reference 12. Weibull plots are better suited for analyzing data such as capacitor breakdown.

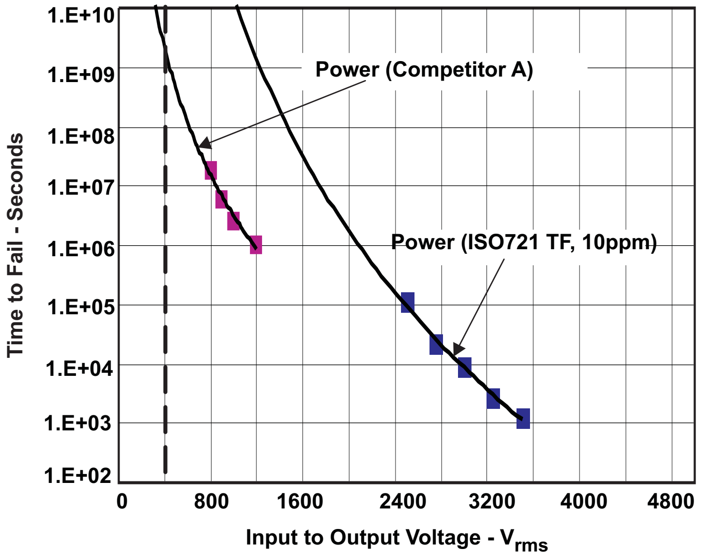
Table 2 summarizes the lifetime predictions at different values of V_{IORM} (Vpeak) using the TDDB E-model illustrated in Figure 3.

Table 2. High-Voltage Lifetime Predictions Based on TDDB E-Model

V_{IORM}, Vpeak	Lifetime per TDDB E-Model (in Years)
200	85
400	46
560	**28**
700	18
800	13

5.2 Model Comparison

Unlike the use of the E-model, competitors often use an arbitrary fit to their data, that is not based on any physical dielectric degradation models. An example is a power fit shown in Figure 4 . The same data used in Figure 3 was plotted here and a best-fit trend-line was generated using a power curve as shown in Figure 4. As can be seen, significantly longer lifetimes can be expected using such an approach. Published competitor data (also at 10-ppm levels) for inductive coupled devices are included for comparison. The competitor data was published using a time scale in years; therefore, in Figure 4, those units were converted from years to seconds for comparison. TI's preference for using the TDDB E-model is based on the fact that this model is conservative and should result in high-confidence predictions compared to any other models or a best data fit methodology.



Note: 3E+08 Seconds = 10 years

Figure 4. High-Voltage Lifetime Based on Best Curve Fit

6 Conclusions

The ISO72x family of products can be safely operated for over 25 years at an operating voltage of 560 V. Results also show that the isolation barrier is robust and can withstand multiple instances of high-voltage spikes of up to 4000 Vpeak or 2828 Vrms, as specified by the V_{IOTM} rating

We currently recommend the ISO7710 from our newest ISO77xx family of digital isolators with improved isolation ratings.

7 References

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2006) to A Revision	**Page**
• Added reference to the ISO7710 device and ISO77xx family of digital isolators in the *Conclusion*	5

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