Interfacing Between LVPECL, VML, CML, and LVDS Levels

Nick Holland — *Serial Gigabit Solutions*

ABSTRACT

This application report introduces the various interface standards used today in modern telecom and datacom systems and describes the methods used to interface between similar and different I/O structures used on Texas Instruments serial gigabit solutions products. The main logic levels discussed in this application report are low-voltage positive/pseudo emitter-coupled logic (LVPECL), current-mode logic (CML), voltage-mode logic (VML) and low-voltage differential signaling (LVDS). This document focuses on these four logic levels, because they are now the most prevalent in today's communications systems. This document deals with the different SERDES devices from Texas Instruments, from input/output structures, various high-speed drivers and receivers, receiver biasing, and termination schemes. Explanations and examples on how to interface different types of drivers and receivers using ac-coupling are also given.

Contents

List of Figures

List of Tables

1 Introduction

As the communications industry is moving to faster data speeds and from parallel- to serial-based technologies, the variety of interfacing standards has led to concerns on how to interface these different logic levels together. The main three priorities for the industry have been to increase performance, decrease power consumption, and reduce cost. Earlier technologies, such as emitter-coupled logic (ECL), used an inconvenient negative power supply rail, which at the time had the advantage of improved noise immunity. Since the implementation of positive-supply technologies such as TLL and CMOS, the older technologies no longer provide a benefit, as a system using them would require several power supplies including the –5.2 V or –4.5 V needed for ECL.

As a result, ECL migrated to positive/pseudo emitter-coupled logic (PECL), which allowed designers to move away from this negative supply rail and simplify board layout. The principle behind PECL was simply to keep the same output swing of 800 mV, but shift it to a positive voltage by using a 5-V rail and ground. Low-voltage positive/pseudo emitter–coupled logic (LVPECL) is the same concept as PECL, but uses a 3.3-V supply rather that the 5-V one. This resulted in a power consumption reduction relative to PECL.

Additionally, as more and more designs use CMOS-based technology, new high-speed drivers have been introduced, such as current mode logic (CML), voltage mode logic (VML), and low-voltage differential signaling (LVDS). This has led to many combinations of switching levels within a system that need to interface with each other.

This application report focuses on the different SERDES devices from Texas Instruments, input/output structures, various high-speed drivers, and biasing and termination schemes. Different types of drivers and receivers can be interfaced, especially if ac-coupling is used. When using ac-coupling, the drivers and receivers are treated separately. AC-coupling is commonly used:

- To interface different technology types
- To interface different signal voltages e.g., 3.3-V driver and 2.5-V receiver
- To interface different ground references between driver and receiver

Note that when ac-coupling is used, the driver and receiver can be treated separately.

2 Switching Levels

The first step in understanding how to interface the various drivers and receivers associated with the logic levels discussed in the application report is to visualize the output voltage swings and biasing voltages. The main voltage levels discussed in this application report are LVPECL, CML, VML, and LVDS.

Table 1 outlines the typical output levels and common-mode voltages for existing Texas Instruments SERDES products.

Table 1. Voltage Parameters by Logic Level

PARAMETER	LVPECL	CML	VML	LVDS
V_{OH}	2.4 V	1.9 V	1.65 V	1.4 V
V_{OL}	1.6 V	1.1 V	0.85 V	1 V
Output voltage (single ended)	800 mV	800 mV	800 mV	400 mV
Common-mode voltage	2 V	1.5 V	1.25 V	1.2 V

An even better method is a visual representation, as shown in Figure 1. The swings shown below are for ac-coupling.

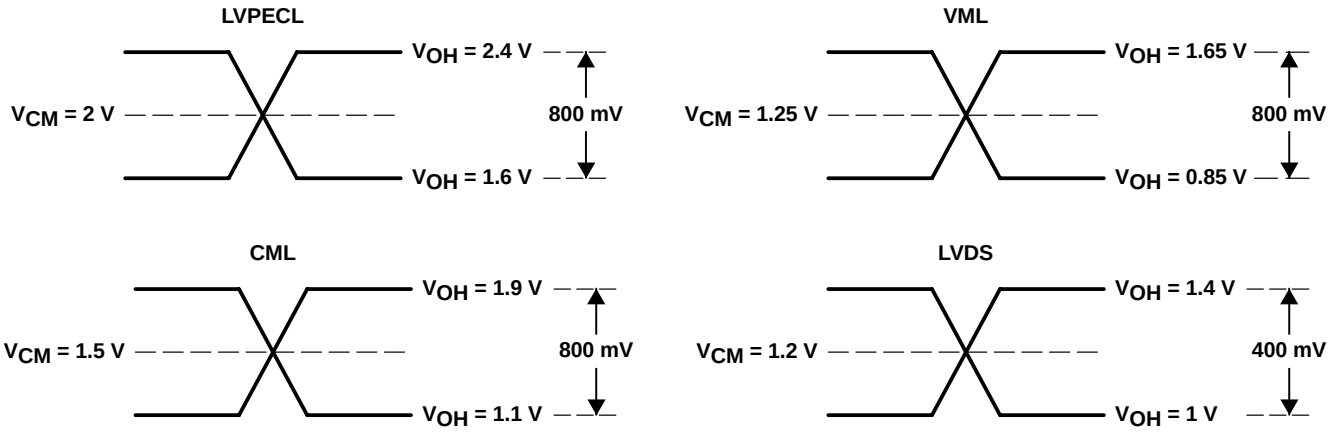

Figure 1. Graphic Voltage Swings by Logic Level

Another vital point is to introduce which Texas Instruments serial gigabit solution SERDES devices have which kind of output drivers. This is listed in Table 2.

Table 2. Logic Level by TI Device

TI PART NUMBER	LVPECL	CML	VML	LVDS
TNETE2201B	X			
TLK1501		X		
TLK2501		X		
TLK2701		X		
TLK2711			X	
TLK3101			X	
TLK1201			X	
TLK2201			X	
TLK2208			X	
TLK31x4			X	
TLK4015		X		
SLK25x1			X	
SLK27x1			X	
SLK2504			X	
SN65LVDS9x				X
SN65LV1021/1212				X
SN65LV1023/1224				X

Now that the switching levels have been introduced along with which Texas Instruments parts include which type of drivers, the next step is to describe how the different input and output stages are designed. This allows the reader to understand how to interface the various logic levels together.

3 Output and Input Stages

As mentioned earlier, it is only relevant to talk about LVPECL, CML, VML and LVDS drivers, because these are the main types of drivers used in CMOS technologies. The section introduces each type of output and input stage.

3.1 LVPECL Interface Structures

LVPECL is derived from ECL and PECL and typically uses 3.3 V and ground supply voltage. The current Texas Instruments serial gigabit solution device that has an integrated LVPECL driver is the TNETE2201 device.

3.1.1 LVPECL Output Stage

The typical output of an LVPECL driver consists of a differential pair with the emitters connected to ground via a current source. This differential pair drives a pair of emitter-followers which provide the current to Output+ and Output–. The LVPECL output stage requires a termination resistance of 50 Ω to the bias voltage of V_{CC} – 2 V. This implies that the emitters of the pair of followers are around V_{CC} – 1.3 V, because there is a 0.7-V drop across the base-emitter junction. The 0.7-V drop across the 50-Ω termination resistors results in a 14-mA flow through the PECL driver. Because the output impedance of the driver is lower than 50 Ω, care must be taken that correct termination is used to reduce voltage reflections that occur due to this mismatch.

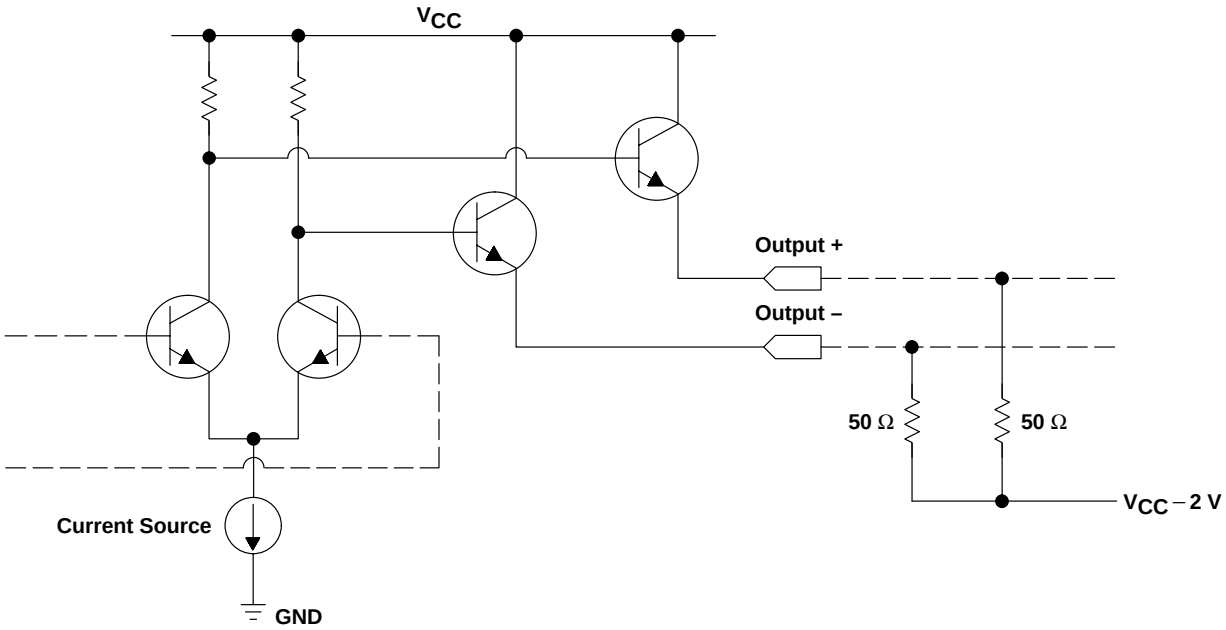

Figure 2. Typical Structure for an LVPECL Output Stage

3.1.2 Input Stage for Devices Using LVPECL Drivers

The TNETE2201 input stage consists of a differential pair which requires its inputs (Input+ and Input–) to be pulled up via resistors to V_{CC} – 1.3 V in order to provide a common-mode voltage of 2 V in the case where V_{CC} is 3.3 V. This is shown more clearly in the interfacing section of this report. If input biasing is not included on-chip, this must be taken care of on the PCB, and the resistors should be placed as close to the device pins as possible.

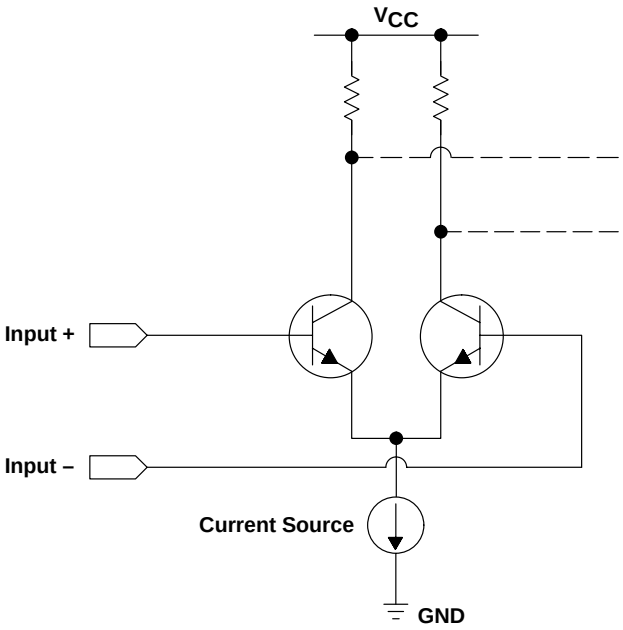

Figure 3. Input Stage for Devices Requiring LVPECL Signaling Levels

3.2 CML Interface Structures

The CML interface drivers provide several design features, including high-speed capabilities, adjustable logic output swing, level adjustment, and adjustable slew rate. Current Texas Instruments serial gigabit solution devices that have an integrated CML driver are the TLK1501, TLK2501, TLK2701, and TLK4015.

3.2.1 CML Output Stage

The above devices have CML drivers that are built from an open-drain differential pair and a voltage-controlled current source using NMOS transistors. The outputs (Output+ and Output–) require pullup resistors to V_{DD} because the NMOS transistor can drive only falling edges efficiently and needs the pullups to help drive rising edges. The voltage-controlled current source is used to vary the amount of current used to drive the load, because the output voltage swing is load dependent. The load resistors and the external reference resistor can then be chosen to optimize output voltage swings.

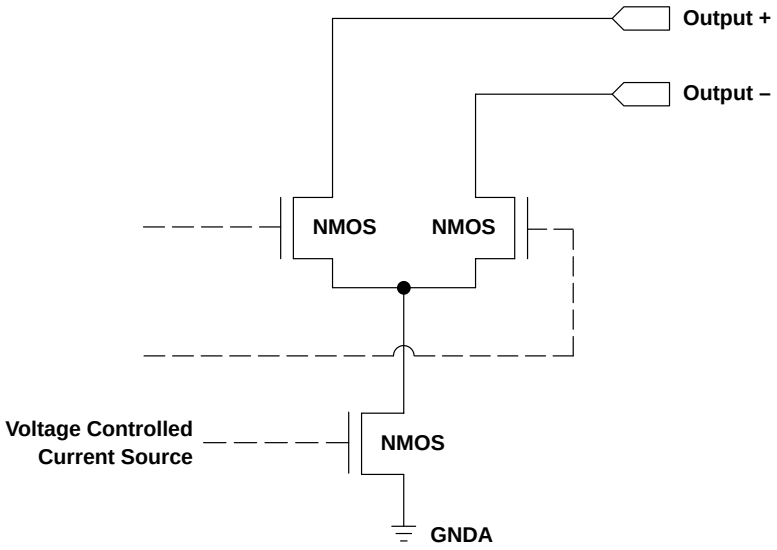

Figure 4. Typical Structure for a CML Output Stage

3.2.2 Input Stage for Devices Requiring CML Signaling Levels

The typical input stage for Texas Instruments devices designed for CML signaling consists of a differential pair using NMOS transistors, and the inputs (Input+ and Input–) require pullup resistors to the common-mode voltage of the receiver. In the case of devices requiring CML voltage levels, the common-mode voltage should be in the range of 1.5 V. Where internal biasing is not included on-chip, this must be taken care of on the PCB, and the resistors should be placed as close to the device pins as possible. The NMOS transistor attached to the drains of the differential pair acts as a latch and basically latches data in the receiver at the rate of the high-speed clock.

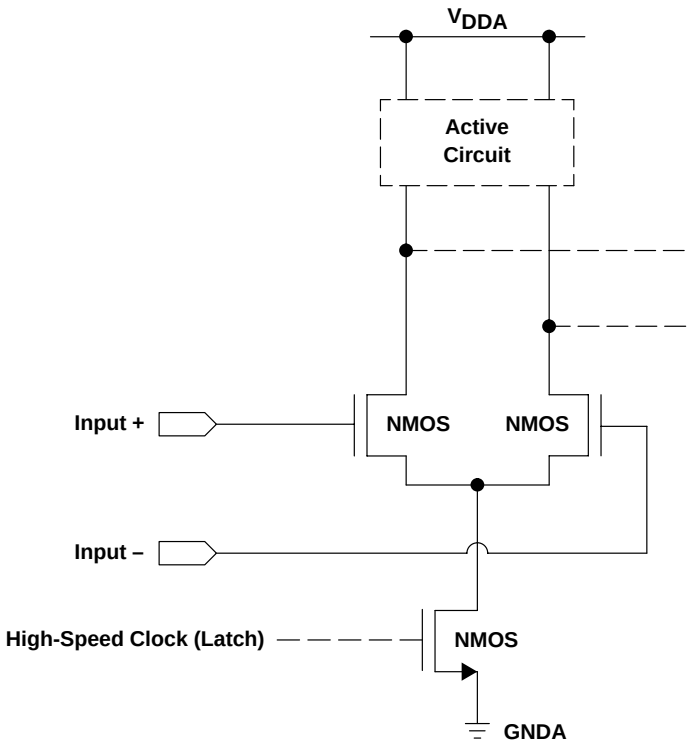

Figure 5. Input Stage for Devices Requiring CML Signaling Levels

3.3 VML Interface Structures

Texas Instruments voltage-mode logic (VML) drivers are voltage-level compatible with LVPECL. Like CML, these drivers are implemented in CMOS, but have the advantage that they do not require external pullup resistors, because of the use of internal NMOS and PMOS transistors to help drive the falling and rising edges. While VML is not yet as widely implemented as the other drivers, it still remains voltage-compatible with LVPECL signaling levels and has been used in many of TI's production devices. Current Texas Instruments serial gigabit solution devices that have an integrated VML driver are the TLK2711, TLK3101, TLK1201, TLK2201, TLK2208, TLK3104SA, TLK3114SA, TLK3104SC, TLK4010(1), SLK2501, SLK2511, SLK2701, SLK2721, and the SLK2504.

3.3.1 VML Output Stage

The above devices have VML drivers that are built as shown in Figure 6. The PMOS and NMOS voltage-controlled voltage sources are used to set V_{OH} and V_{OL} of the driver, and the output transistor simply swings between those values. The output swing of VML interfaces is independent of the load impedance.

(1)Upcoming device.

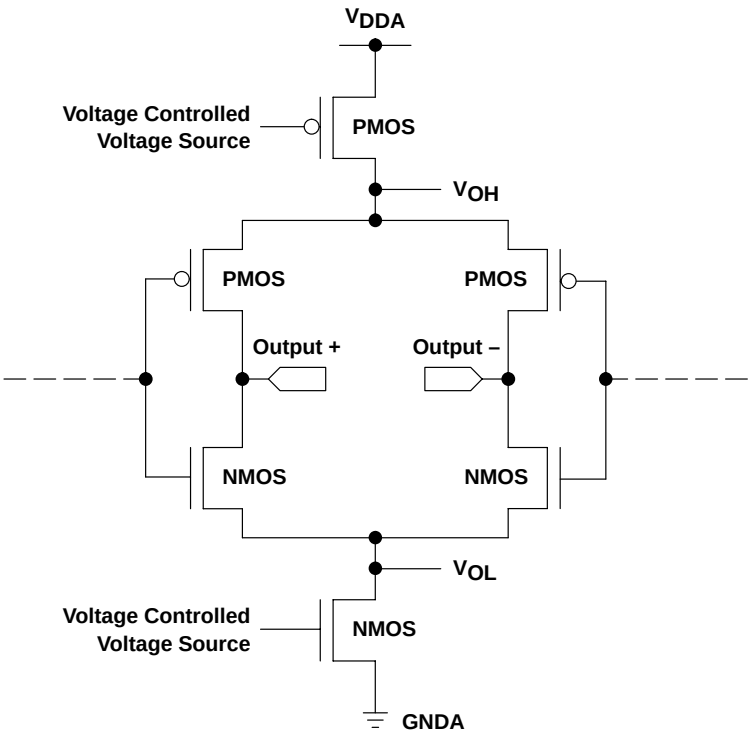

Figure 6. Typical Structure for a VML Output Stage

3.3.2 Input Stage for Devices Requiring VML Signaling Levels

Similar to the CML receiver, the input stage for devices requiring VML signaling levels consists of a differential pair using NMOS transistors and the inputs (Input+ and Input–) need pullup resistors to the common-mode voltage of the receiver. See the CML section (Section 3.2) for further explanation of this type of input structure.

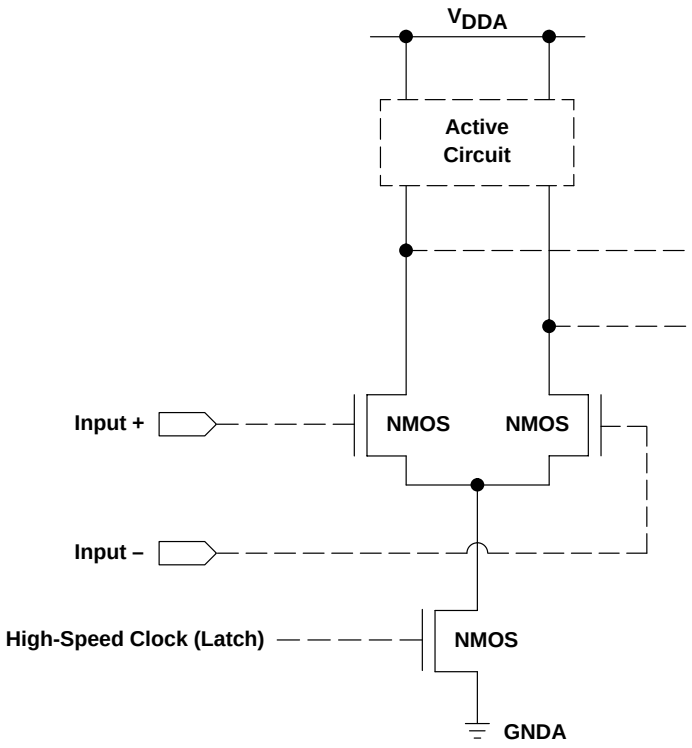

Figure 7. Input Stage for Devices Requiring VML Signaling Levels

3.4 LVDS Interface Structures

The low-voltage differential signal (LVDS) standard is defined by ANSI TIA/EIA-644 and IEEE 1596.3–1996. LVDS has a lower swing and speed than LVPECL, CML, and VML, and therefore typically uses less power. Many LVDS drivers are built with constant current so power consumption does not scale with transmission frequency. Current Texas Instruments serial gigabit solution devices that use these logic levels are SN65LVDS93, SN65LVDS94, SN65LVDS95, SN65LVDS96, SN65LV1021, SN65LV1023, SN65LV1212, and SN65LV1224.

3.4.1 LVDS Output Stage

The LVDS output stage is similar to the VML driver except that Texas Instruments LVDS SERDES output structures use a feedback loop to regulate the common-mode output voltage of the driver. This is shown is Figure 8. A current source attached to the drains of the NMOS transistors is used to control the output current, which is typically 3.5 mA, and provides a 350-mV swing across the typical 100-Ω termination resistor at the receiver.

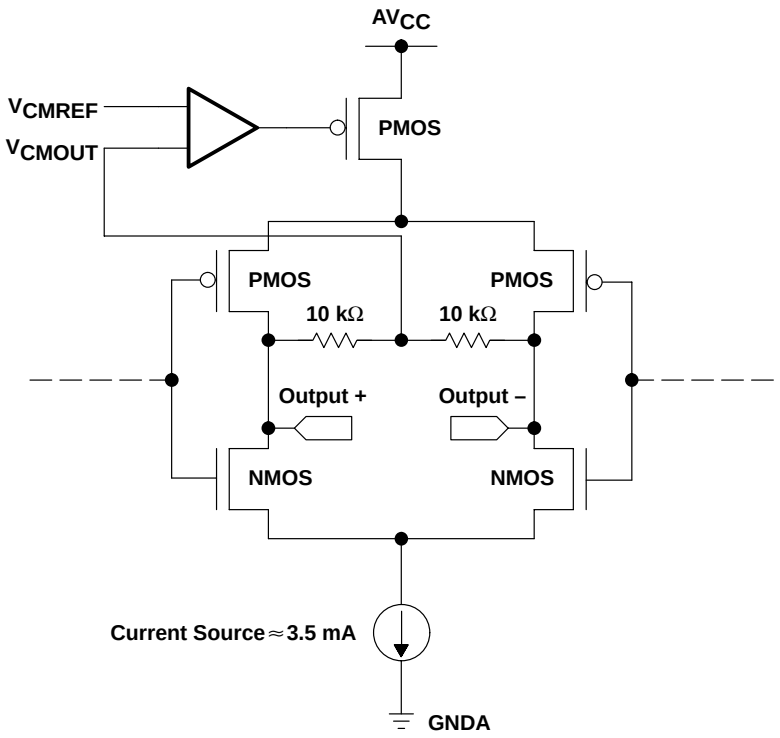

Figure 8. Typical Structure for an LVDS Output Stage

3.4.2 Input Stage for Devices Requiring LVDS Signaling Levels

The typical input stage for TI's LVDS-based SERDES devices consists of a differential pair using NMOS transistors, and the inputs (Input+ and Input–) require a 100-Ω termination resistor across the inputs with a common-mode voltage around 1.2 V. Where internal 100-Ω termination biasing is not included on-chip, this must be taken care of on the PCB, and the resistor should be placed as close to the device pins as possible. The current source attached to the drains of the NMOS transistors simply provides a small amount of current for the differential pair.

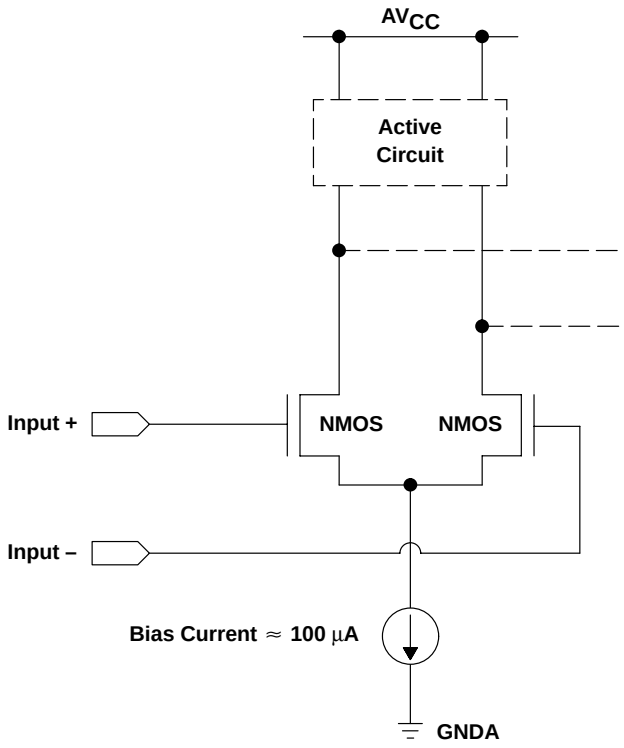

Figure 9. Input Stage for Devices Requiring LVDS Signaling Levels

4 Interfacing Texas Instruments SERDES Devices

This section of the document shows how the various drivers and receivers should be interfaced in terms of termination resistors, termination voltages, dc- and ac-coupling, and shows how different termination schemes can be achieved and what their advantages and disadvantages are. LVPECL, CML, VML and LVDS are the main types of drivers discussed in this report. The assumption here is that all the receivers have high-impedance inputs.

- DC-coupling is typically used where common-mode voltage is not an issue or to avoid impedance discontinuity due to the capacitor impedance.
- AC-coupling is typically used to remove common-mode voltage when common-mode biasing is required or when interfacing different logic types, and assumes a dc-balanced signal pattern.

4.1 LVPECL

4.1.1 LVPECL Driver—DC-Coupled

An LVPECL driver needs a termination of V_{CC} – 2 V when dc-coupled. This implies that for a V_{CC} of 3.3 V the termination voltage should be 1.3 V. The termination resistors R_t should also be the same value as the characteristic impedance Z_O of the transmission line.

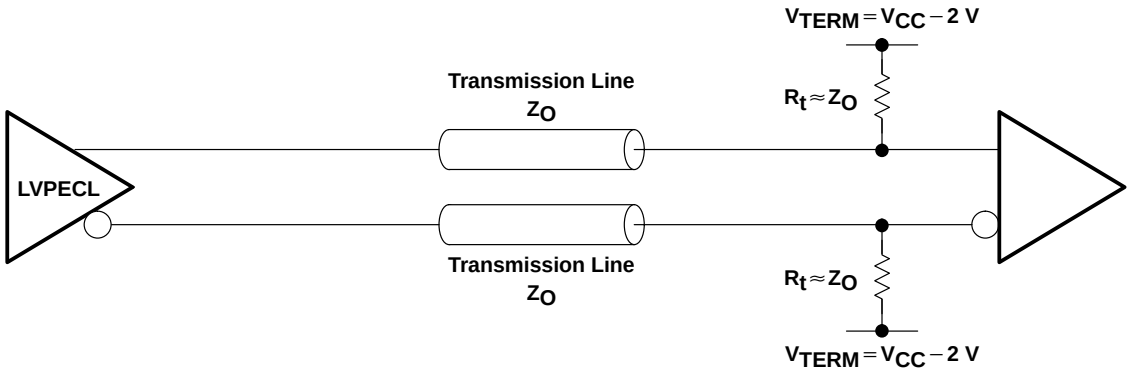

Figure 10. LVPECL Driver for DC-Coupling

4.1.2 LVPECL Driver—AC-Coupled

In the case of ac-coupling, because there is no longer a dc path for falling edges, the LVPECL driver outputs should be grounded via small resistors in the range 140 Ω – 220 Ω in order to provide dc for falling-edge current. On the receiver side, the termination resistors should be at V_{CC} – 1.3 V, because if the receiver requires an LVPECL signaling level, the common-mode voltage is around 2 V for a 3.3-V supply voltage. In the case that the receiver requires a different voltage swing, then the termination resistors R_t should be terminated to the common-mode input voltage of the receiver.

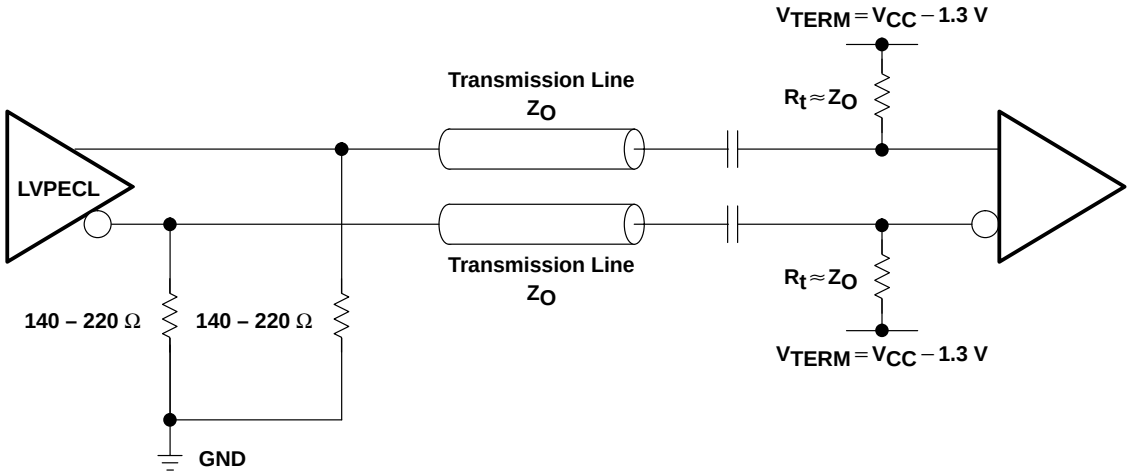

Figure 11. LVPECL Driver for AC-Coupling

4.2 CML

4.2.1 Current Mode Logic (CML) Driver—DC-Coupled

As shown previously, Texas Instruments has CML drivers that use open-source NMOS transistors. In order to drive rising edges, the drivers must have pullup resistors to V_{DD}. These pullup resistors should be equal to Z_O to avoid unwanted reflection due to unmatched lines.

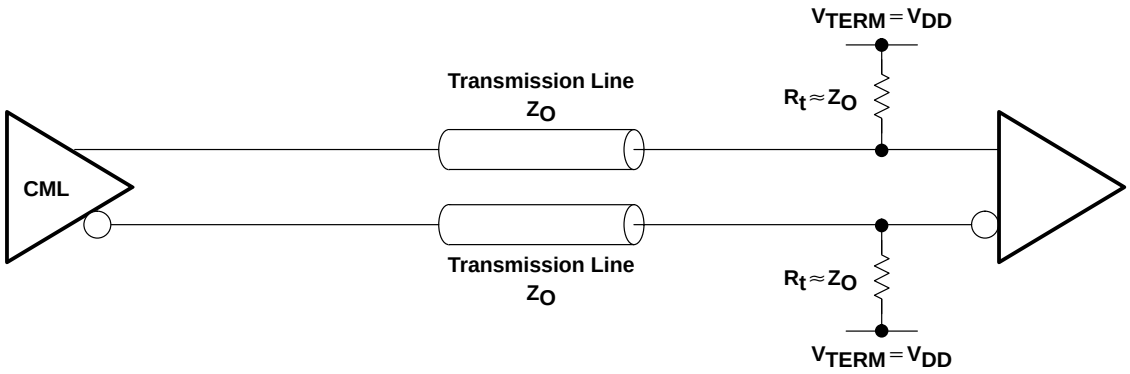

Figure 12. CML Driver for DC-Coupling

The termination scheme is not robust for systems that have impedance discontinuities that could result in multiple reflections. The ac-coupled scheme without the coupling capacitors would provide double termination of the signal and hence and more robust system. A point to note is that through double termination of the line, the signal swing is halved.

4.2.2 Current Mode Logic (CML) Driver—AC-Coupled

In the case of ac-coupling, the CML driver again needs to be pulled to V_{DD} because the rising edge still needs to be driven. On the receiver side, since the capacitor removes the dc component of the incoming signal, the termination resistor should be connected to a voltage that is set to the receiver common-mode input voltage.

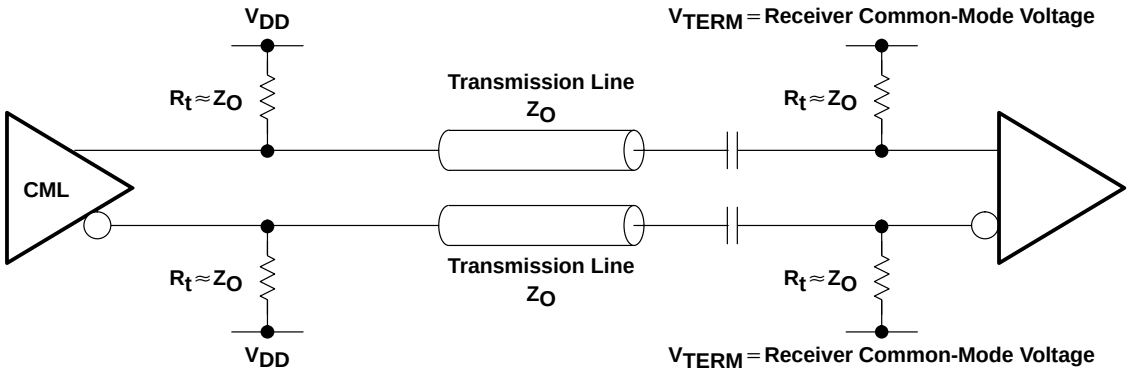

Figure 13. CML Driver for AC-Coupling

4.3 VML

4.3.1 Voltage Mode Logic (VML) Drivers—DC-Coupled

VML drivers have the advantage that they do not need to have pullup or pulldown resistors, because they have additional PMOS and NMOS transistors in their output structures that drive both rising and falling edges. This simplifies board layout; all that is required is a differential termination on the receiver.

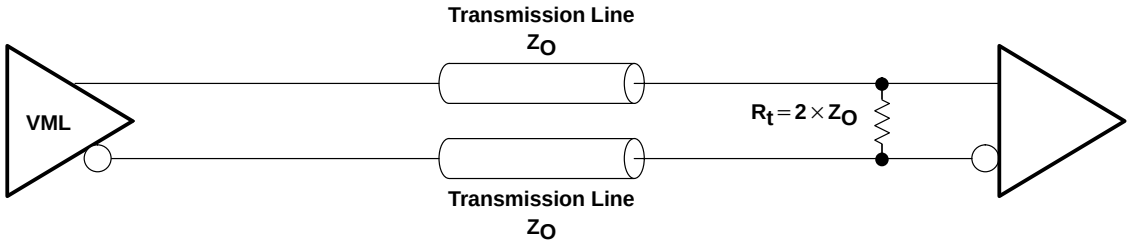

Figure 14. VML Driver for DC-Coupling

This termination configuration is fine if no differential-skew or common-mode noise exists. However, in most situations there is some differential-skew or common-mode noise and therefore the following termination may be more appropriate.

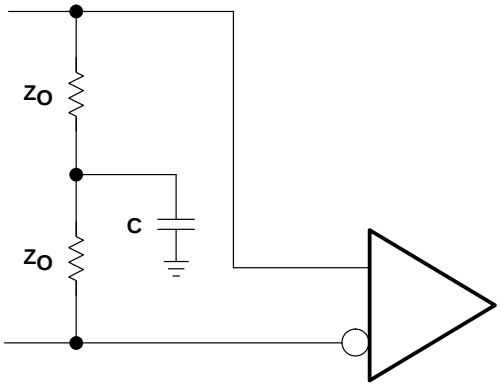

Figure 15. Split Differential Termination With Capacitor

In Figure 15, by using Z_O termination resistors and a common-mode capacitor, this eliminates both differential-skew and common-mode noise.

4.3.2 Voltage Mode Logic (VML) Drivers—AC-Coupled

In the case of ac-coupling, the termination resistors must be connected to a voltage that is set to the common-mode voltage of the receiver. Again, the benefit of VML drivers is that even with ac-coupling, no pullup or pulldown resistors are needed.

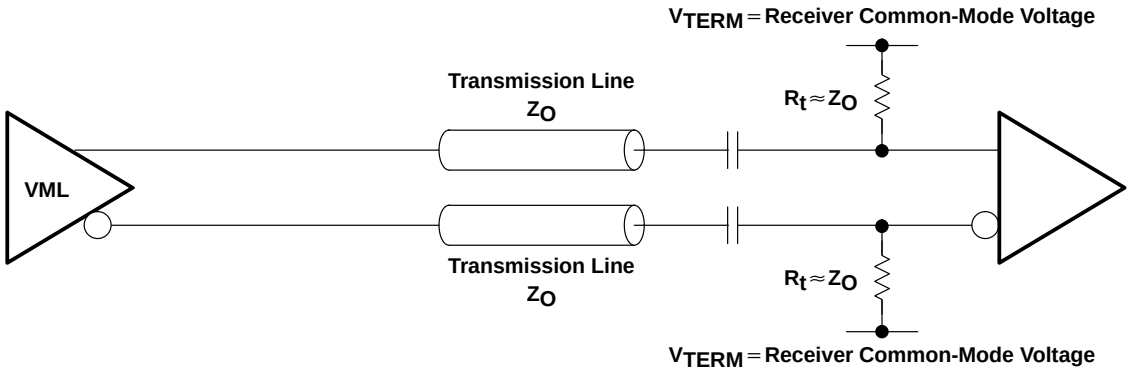

Figure 16. VML Driver for AC-Coupling

4.4 Low-Voltage Differential Signaling (LVDS) Drivers—DC-Coupled

Because LVDS is a form of current driver, the direction of the current across the termination resistor creates the voltage signal at the receiver input. Typically, the differential termination R_t is 100 Ω, but this depends on the value of Z_O.

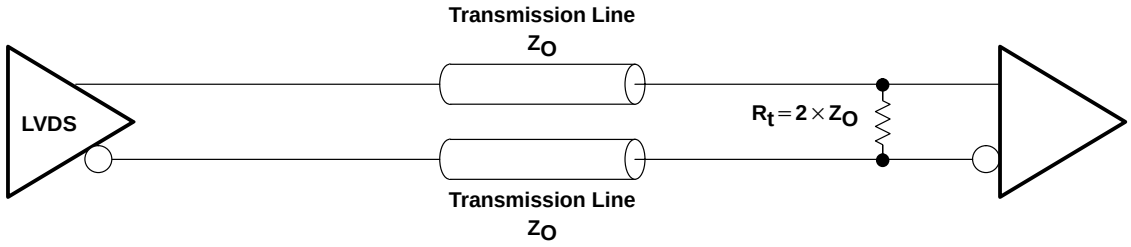

Figure 17. LVDS Driver for DC-Coupling

5 Biasing and Termination Schemes

Different receivers from the family of Texas Instruments SERDES require different types of common-mode voltages and termination configurations.

5.1 Biasing

The easiest way of creating a biasing voltage is using a simple resistor network as shown in Figure 18.

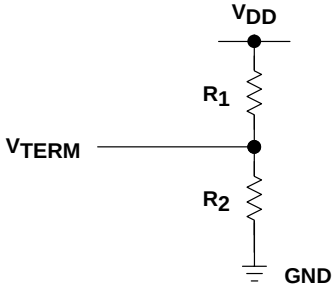

Figure 18. Simple Resistor Network for Biasing Voltages

Example 1.

Take the case of a VML driver and the TLK2501, which has a receiver that requires CML voltage levels. The characteristic impedance of the transmission line is 50 Ω and V_{DD} is 2.5 V. The input common-mode voltage for the TLK2501 could be in the range from 1.5 V to $V_{DD} – V_{ID}/2$. In this case, 2.0 V is chosen as an appropriate value.

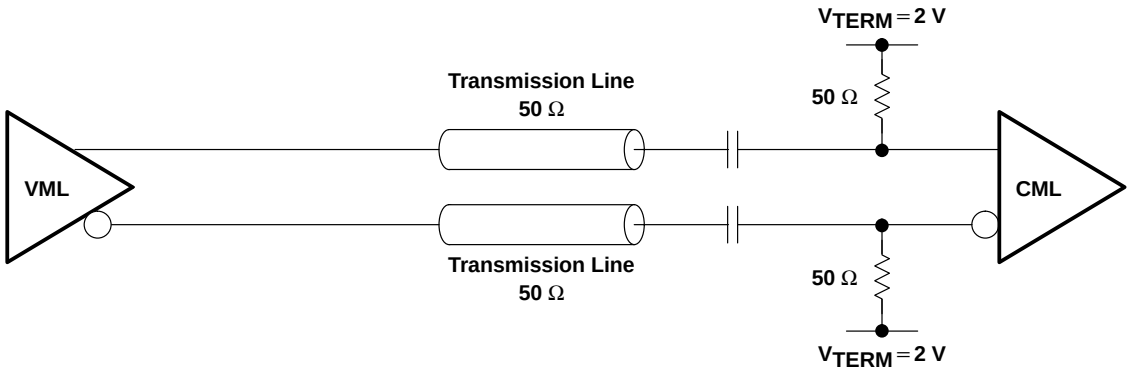

Figure 19. Example With VML Driver and Receiver Requiring CML Voltage Levels

The well-known voltage-divider equation

$$V_{OUT} = V_{IN} \times \frac{R2}{R1 + R2} \quad (1)$$

can be rearranged to show the ratio of resistor values.

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2}{R1 + R2} \quad (2)$$

In the example above, substituting V_{DD} and V_{TERM} numbers into equation 2 gives

$$\frac{R2}{R1 + R2} = 0.8$$

Typical values for R1 and R2 should be in the hundreds of ohms, to provide enough current to keep the biasing point at the required voltage and not to interfere with the termination of the signals.

On the Texas Instruments TLK2501 EVM, R1 and R2 resistor values where chosen as R1 = 200 Ω and R2 = 825 Ω, providing a 2.01-V termination voltage.

There are, of course, more elegant ways of terminating and biasing differential transmission lines. They are discussed in Section 5.2.

5.2 Termination Schemes

There are typically four ways of termination and biasing differential lines. They all have their advantages and disadvantages.

5.2.1 Differential Scheme

This is probably the simplest of all termination and biasing schemes. R1 and R2 are used for a voltage divider. Their values should be in the kilohm range and should set the input at the correct common-mode voltage for the receiver. The differential termination is simply 2 times the characteristic impedance.

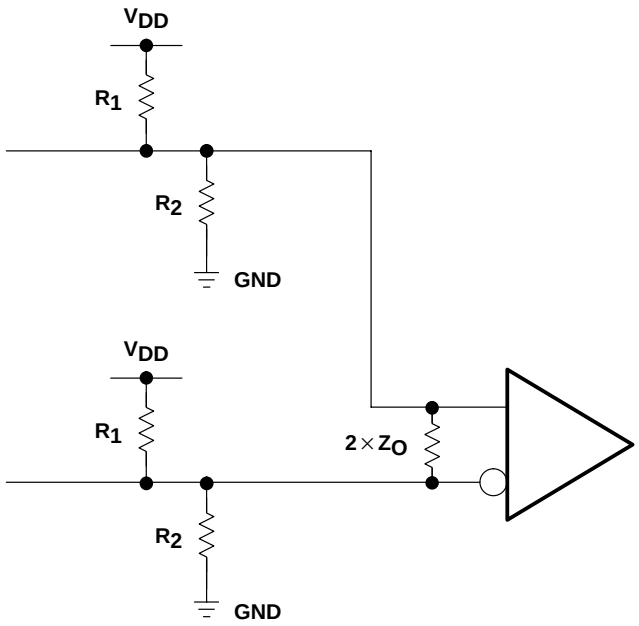

Figure 20. Differential Termination With Biasing

The main disadvantage is the component count and the power consumption though the voltage divider network; however, this can be kept to a low value by choosing high values for R1 and R2.

5.2.2 Differential Scheme With Decoupling Capacitor

The second variation for a termination scheme is similar to the one in Figure 20, but this time the differential termination resistor is split into two 50-Ω (Z_O) resistors in series with a decoupling capacitor to ground.

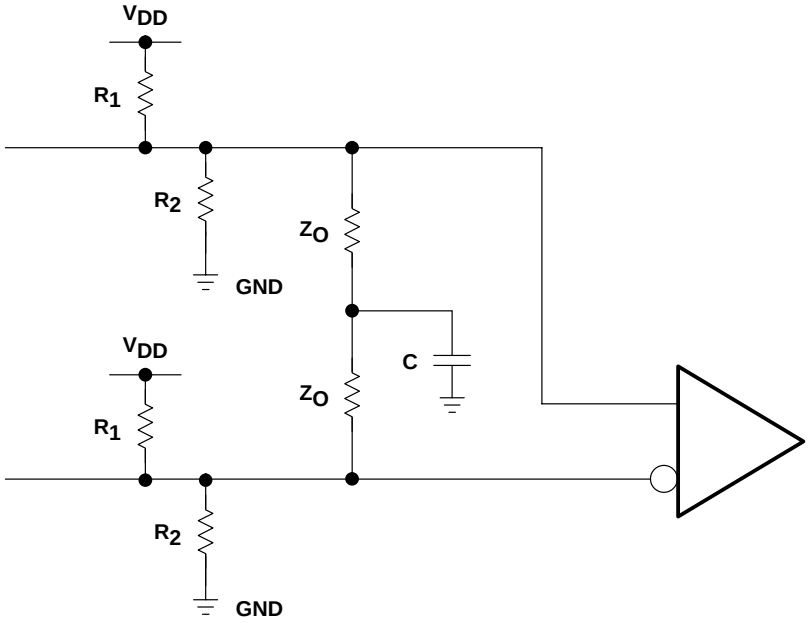

Figure 21. Differential Termination With Biasing and Decoupling Capacitor

As with the differential scheme, the main disadvantages here are the component count and the power consumption though the voltage divider network; however, power consumption can be kept to a low value by choosing high values for R1 and R2. However, the advantage of using the capacitor to ground is that if there is some transmission line skew, i.e., the differential signals do not arrive at the same time due to different line lengths or driver output slew, the capacitor acts as a small-signal short circuit.

5.2.3 Differential Scheme With Reduced Resistor Count

The third variation for a termination scheme combines the termination into the voltage divider network as shown in Figure 22.

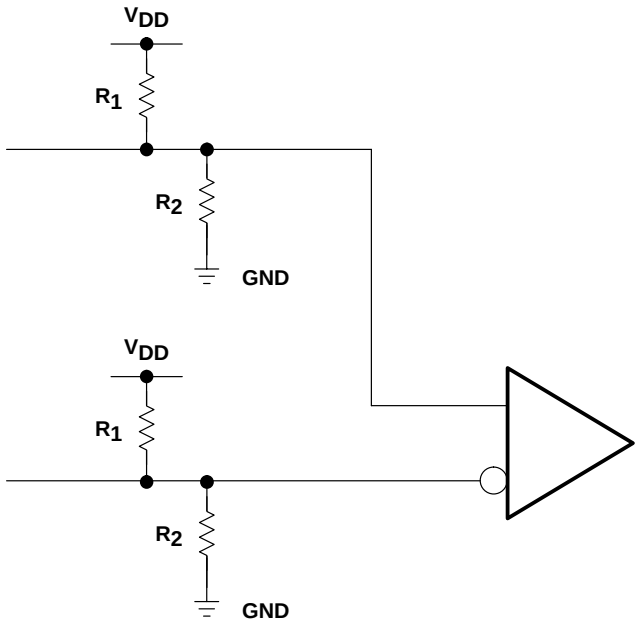

Figure 22. Differential Termination With Reduced Resistor Count

The idea behind this configuration is to make the value of R1 || R2 equal to Z_O of the transmission line, while at the same time providing the correct common-mode input voltage for the receiver.

Example 2.

In this example, we have a VML driver and the TLK2501, which has a receiver that requires CML voltage levels. The characteristic impedance of the transmission line is 50 Ω and V_{DD} is 2.5 V. The input common-mode voltage for the TLK2501 could be in the range 1.5 V to $V_{DD} – V_{ID}/2$. In this case, 2.0 V is chosen as an appropriate value for the biasing voltage.

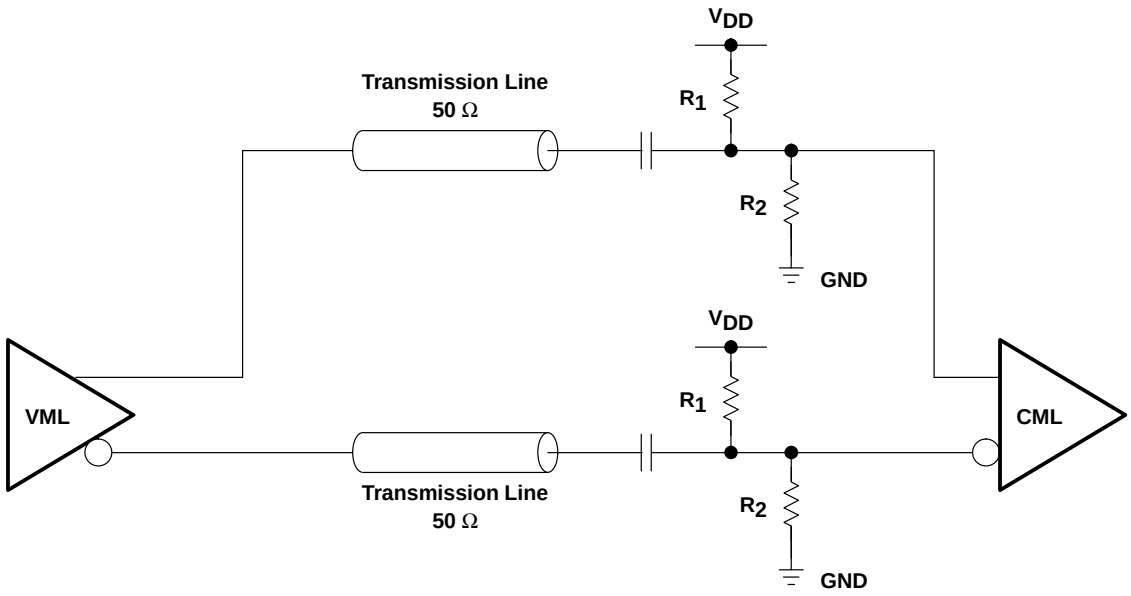

Figure 23. Example With VML Driver and Receiver Requiring CML Voltage Levels

The two main criteria in this kind of termination scheme are:

1. R1 || R2 = Z_O
2. Voltage divider network R1 and R2 set V_{TERM} = 2.0 V

Using the following for parallel resistors (R1 || R2 = 50 Ω):

$$\frac{1}{R1} + \frac{1}{R2} = \frac{1}{Zo} = 50\ \Omega$$

rearranging to:

$$\frac{R1 \times R2}{R1 + R2} = 50\ \Omega$$

rearranging to:

$$(R1 + R2) = \frac{R1 \times R2}{50\ \Omega} \quad (3)$$

Using the voltage divider equation:

$$\frac{R2}{R1 + R2} = \frac{V_{DD}}{V_{TERM}}$$

rearranging to:

$$(R1 + R2) = \frac{R2 \times V_{DD}}{V_{TERM}}$$

rearranging to:

$$(R1 + R2) = 1.25\ R2 \quad (4)$$

Substituting equation 4 into 3:

$$1.25\ R2 = \frac{R1 \times R2}{50\ \Omega} \quad (5)$$

rearranging to:

$$R1 = 1.25 \times 50\ \Omega \qquad R1 = 62.5\ \Omega$$

$$R2 = \frac{R1}{0.2} \qquad R2 = 250\ \Omega$$

Obviously, in this case the values for R1 and R2 are lower than for the previous example, resulting in a lower component count, but increasing waste power consumption.

5.2.4 Differential Scheme With One Biasing Network

The final variation for a termination scheme combines the termination into the voltage divider network as shown in Figure 24.

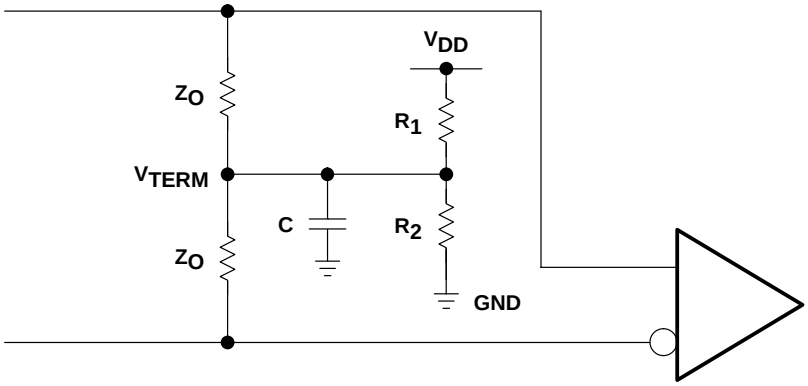

Figure 24. Differential Termination With One Biasing Network

This is a very clean scheme, because only one voltage divider network is used for both signal lines, reducing power consumption. The decoupling capacitor and two termination resistors reduces noise on the receiver due to signal skew.

This is one of the best termination and biasing schemes for parts that do not have internal biasing.

R1 and R2 should be in the kilohm range and the termination resistors should be set to Z_O.

The configuration enables the termination resistors to be placed close to the device, while allowing the biasing circuit to be placed further away form the part. Note that the capacitor needs to be as close to the component as possible.

5.3 Internal Termination and Biasing Summary

Section 5.2 explained the different termination and biasing schemes needed for Texas Instruments' range of SERDES devices. The following table summarizes which devices already have high-speed termination and V_{TERM} biasing on-chip, allowing for a simpler board layout.

TI PART NUMBER	TERMINATION	BIASING
TNETE2201B	–	–
TLK1501	–	–
TLK2501	–	–
TLK2701	–	–
TLK2711	X	X
TLK3101	X	X
TLK1201	–	X
TLK2201	–	X
TLK2208	X	X
TLK31x4	X	X
TLK4015	–	–
SLK25x1	X	X
SLK27x1	X	X
SLK2504	X	X
SN65LVDS9x	–	–
SN65LV1021/1212	–	–
SN65LV1023/1224	–	–

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265