Active Fail-Safe in TI's LVDS Receivers

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ABSTRACT

Differential line receivers commonly have fail-safe circuits to prevent the receiver from switching on input noise. Many innovative LVDS fail-safe solutions require either external components, with subsequent reduction in signal quality, or integrated solutions with limited application. This paper addresses an innovative integrated fail-safe incorporated into the SN65LVDS32B receiver (hereafter referred to as the LVDS32B) and similar parts that solves the limitations seen in present solutions. A detailed theory of operation is presented, supported by laboratory work demonstrating Active Fail-Safe performance.

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1 Introduction

Differential data line receivers can switch on noise in the absence of an input signal. This can occur when the bus driver is turned off or the interconnecting cable is damaged or disconnected. Generally, this problem is solved with an external resistor network applying a steady-state bias voltage to the undriven input pins. In addition to the cost of external components, this lowers the input-signal magnitude and reduces the differential-noise margin.

The fail-safe function attempts to drive the output of the data receiver to a known state under floating or disconnected bus conditions. However, the fail-safe features of many existing differential receivers are limited to open-circuit conditions or restricted to only certain operating conditions. The LVDS32B Active Fail-Safe (TI Patent Pending) function is not restricted to the limitations seen in existing solutions. This paper explains some of the existing fail-safe solutions, the differences between present fail-safe solutions, and the advantages seen by using Active Fail-Safe.

2 What Is Active Fail-Safe?

A fail-safe circuit provides a known receiver output when a valid input signal is not present. Receivers without fail-safe will oscillate in response to input differential noise. As previously mentioned, one technique to solve this problem is to bias the bus externally as shown in Figure 1. This maintains a dc offset in the absence of a valid signal. However, the presence of a bias network can unbalance the driver output loop currents. This can distort the output signal and possibly reduce the input signal amplitude to the receiver. When this happens, the possibility of switching on input noise is increased. Therefore, it is desirable to provide a fail-safe function with minimal impact on the input signal during normal operation.

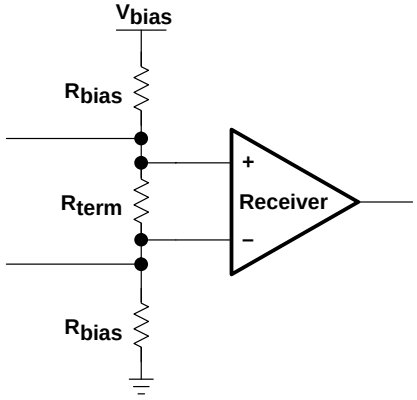

Figure 1. External Bias Network

Existing integrated fail-safe implementations rely on bias currents integrated internally into the receiver. As illustrated in Figure 2, the bias sources provide a current through the termination resistor. This ensures that a dc voltage is maintained across the termination resistor when a valid input signal is not present. The receiver in Figure 2 uses a pullup and a pulldown current source to maintain a dc bias across the termination resistor. Other integrated solutions, such as in the non-B version of the LVDS32, use a pullup on both input pins to bias each node up to V_{CC}. Logic detects this and drives the output to a known state.

The small bias currents used by existing integrated fail-safe solutions do not appreciably affect the input-signal magnitude. However, one disadvantage of the existing solutions is that the fail-safe bias currents are unable to generate the required differential with an external common-mode voltage applied. Increasing the bias currents to improve this would result in additional bus loading during normal operation. Additionally, the offset created when pulling the two differential signals apart increases the input-signal magnitude required by the receiver to switch. This offset also contributes to pulse skew, which is the difference between the time needed for the receiver to switch from low to high and the time to switch from high to low.

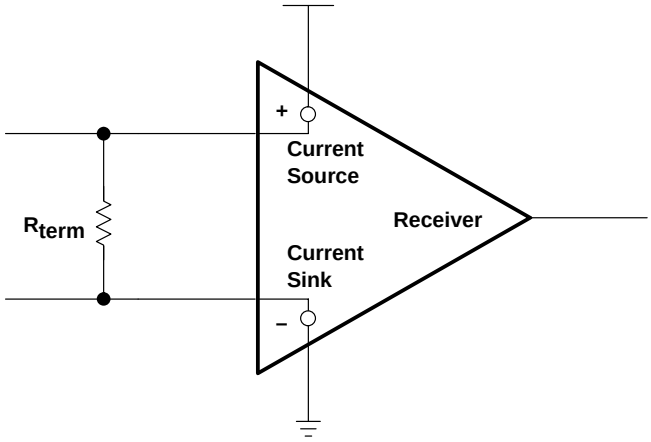

Figure 2. Integrated Fail-Safe With Bias Currents

Fail-safe as implemented on the LVDS32B relies not on bias circuits but a window-comparator circuit to monitor the differential voltage at the receiver input pins. The window comparator senses when the input differential is less than 80 mV and drives the output to a logic high state. Because Active Fail-Safe requires no external resistor bias network or internal bias current to generate an offset, it neither affects the receiver input threshold nor adds any significant bus loading. The window comparator operates over the entire input common-mode range of the receiver. Therefore, Active Fail-Safe operates even when an external, common-mode voltage is applied.

2.1 Active Fail-Safe Operation

Figure 3 shows one of the LVDS32B receiver channels with Active Fail-Safe. It consists of a main receiver that can respond to a high-speed input differential signal. Also connected to the input pair are two fail-safe receivers that form a window comparator. The window comparator has a much slower response than the main receiver and detects when the input differential falls below 80 mV. A 600-ns, fail-safe timer filters the window comparator outputs. When $\overline{\text{FAILSAFE}}$ is asserted, the fail-safe logic drives the main receiver output to a logic high.

During normal operation, the main receiver tracks the input signal. It switches when the input signal changes polarity and exceeds 50 mV of hysteresis. Each time the main receiver switches, the fail-safe timer resets and begins timing from zero.

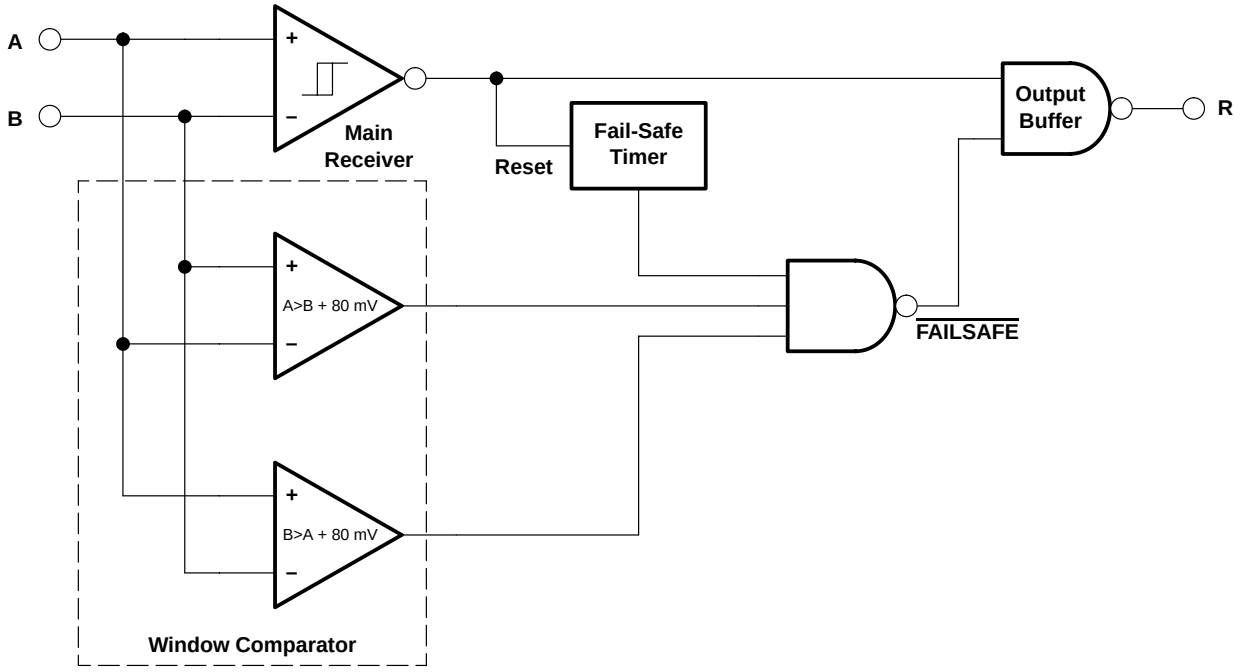

Figure 3. Receiver With Active Fail-Safe

The window comparator monitors both inputs on a continuous basis to detect a loss of input signal. If the two inputs are within 80 mV of each other, the window comparator outputs are driven high. The window-comparator outputs are then gated with the fail-safe timer. If the timer is allowed to reach its maximum value and the window comparator still detects a low differential input, the receiver output is driven to a logic high state.

Under normal conditions and when the timer expires, the input differential signal is greater than 100 mV and, as illustrated in Figure 4, $\overline{\text{FAILSAFE}}$ is not asserted. Here, the input signal begins with A greater than B by 400 mV. The input then switches polarity and B is greater than A by 100 mV. When the input switches, the output of the receiver is driven low (upper trace of Figure 4) and the fail-safe timer begins timing. After approximately 600 ns, the timer output is set high and enables the window comparator to drive the $\overline{\text{FAILSAFE}}$ node. Since the difference between inputs is 100 mV (greater than the fail-safe threshold), $\overline{\text{FAILSAFE}}$ is not asserted, and output node R remains at logic low tracking the input signal.

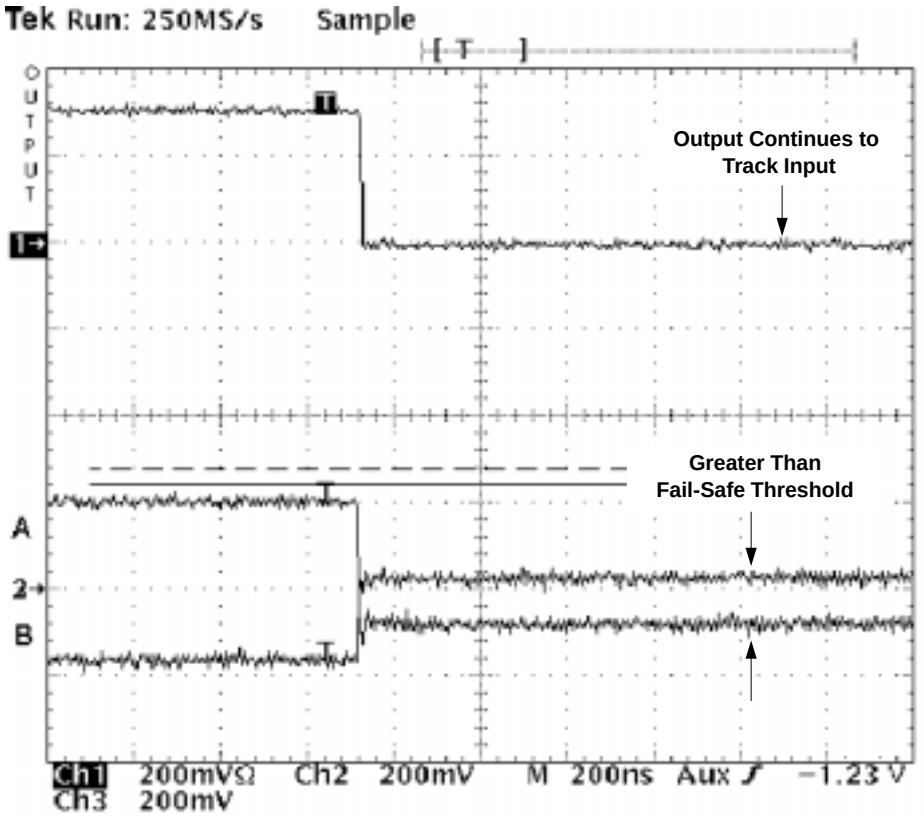

Figure 4. Receiver Operation With Valid Inputs

If the fail-safe timer expires and the input differential is less than 80 mV, $\overline{\text{FAILSAFE}}$ is asserted and output node R of the receiver is driven to logic high. Figure 5 illustrates this condition. The input signal begins with A greater than B by 400 mV. The input then switches polarity with B greater than A by approximately 50 mV. When the input switches, the receiver output is driven low and the fail-safe timer is reset and begins timing. When the timer expires, since B is greater than A by only 50 mV, $\overline{\text{FAILSAFE}}$ is asserted. Figure 5 illustrates the receiver output R being driven high 600 ns after the switch even though B is greater than A (normally a low output condition). This figure demonstrates how Active Fail-Safe functions when a valid input signal is lost.

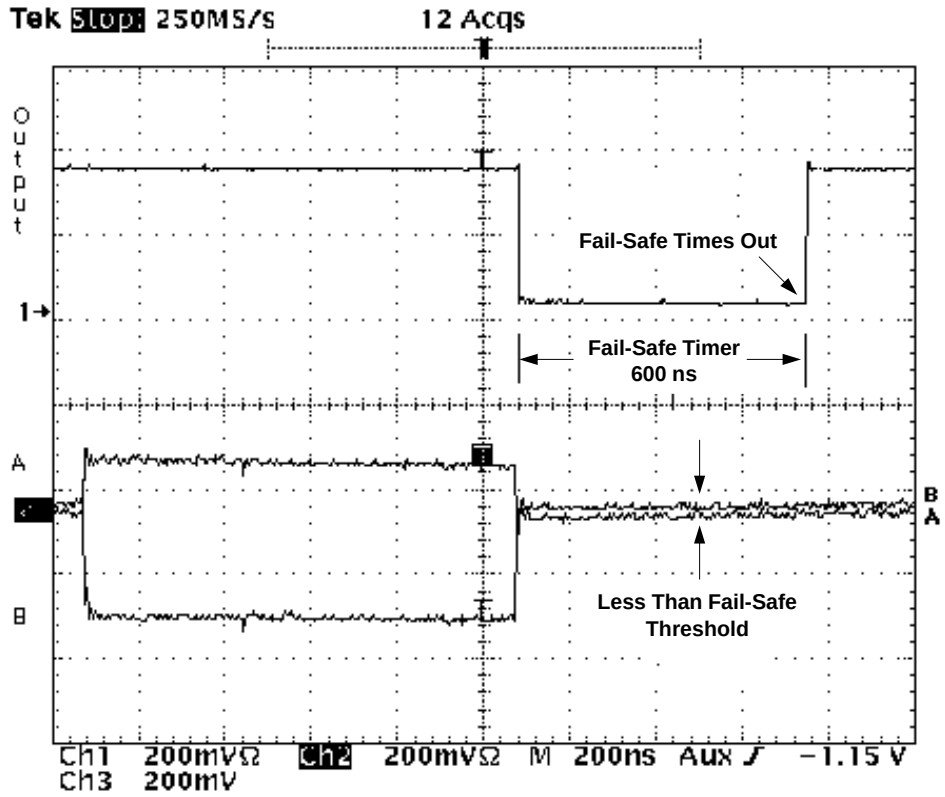

Figure 5. Receiver Operation With Invalid Inputs

After the fail-safe function has been asserted, the window comparator and logic continue to drive the output to a logic high as long as the inputs remain within 80 mV of each other. If a valid differential signal is restored at the input, one window-comparator output is driven low and the fail-safe signal is driven high. The receiver then resumes tracking the input signal. Figure 6 illustrates this, starting with B greater than A by 50 mV and $\overline{\text{FAILSAFE}}$ asserted (fail-safe signal drives the output to logic high). The input signal then increases in magnitude where B is greater than A by 400 mV. $\overline{\text{FAILSAFE}}$ then is deasserted and the receiver begins tracking the input signal and drives the output node R to a low state.

If the main receiver does not switch when the input is restored, the fail-safe timer does not reset. Thus, if the input signal subsequently is reduced in amplitude with no reversal of polarity, fail-safe will immediately resume control of the receiver output. If the application of the valid signal results in the main receiver switching, the fail-safe timer is reset and any subsequent signal loss will not be detected until the timer is allowed to reach its maximum value.

Note that Active Fail-Safe relies on the main receiver hysteresis (50 mV) to keep $\overline{\text{FAILSAFE}}$ asserted. If external noise is large enough to cause the main receiver to switch, the fail-safe timer is reset and the fail-safe function is disabled. $\overline{\text{FAILSAFE}}$ will not be reasserted until the input noise is less than the receiver hysteresis for the entire fail-safe timer period.

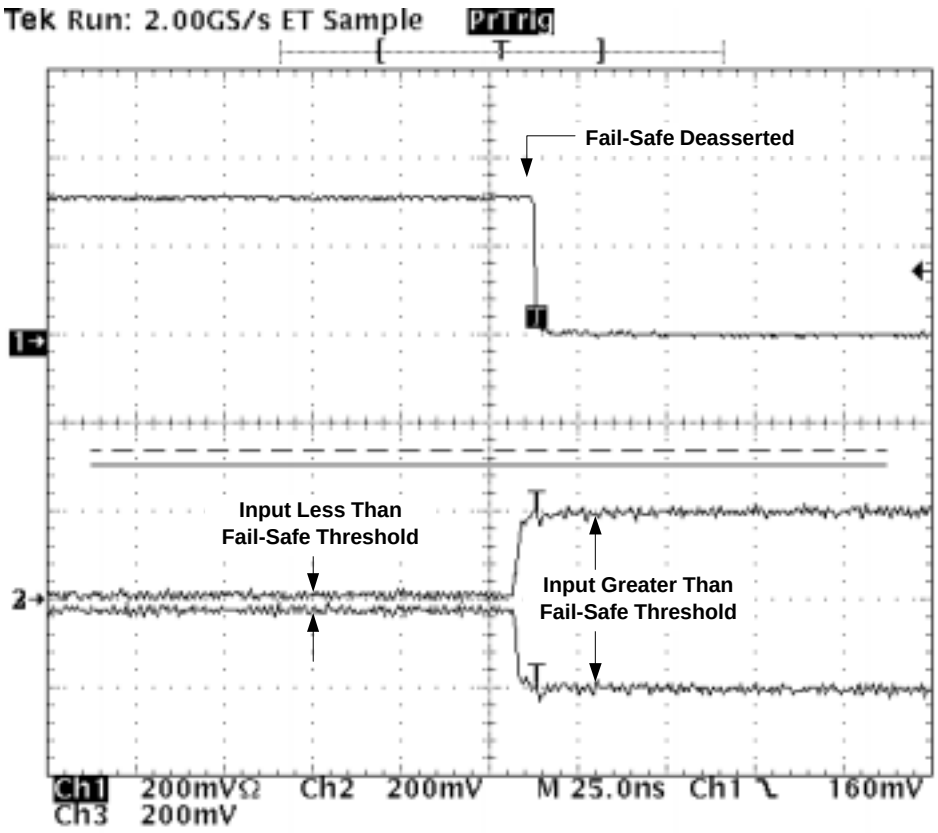

Figure 6. Restoration of Valid Input Signal

2.2 Active Fail-Safe Supported Conditions

Active Fail-Safe guarantees the output is driven to the fail-safe state when the input pins are shorted (from a crushed cable), left open (an unused receiver), or connected together through a termination resistor when the line driver is disabled or removed.

Following is a detailed summary of the supported fail-safe conditions:

Open Input Pins – In a multipoint or multidrop configuration, unused nodes can be disconnected from the bus. It is also possible to have multichannel receivers with a portion of the channels used and unused channels left open. If receiver inputs are left floating, both pins are pulled internally to the same potential. Active Fail-Safe detects this condition and drives the receiver output R to a logic high.

Idle bus – If the receiver is connected to an idle bus with the driver in the high impedance state (turned off) the receiver input pins are pulled to nearly the same voltage via the termination resistor. Normally this would be near the receiver's differential threshold and any external noise would cause the receiver to switch. Active Fail-Safe detects the low differential input and provides a known output state.

Shorted Inputs Pins – Line-fault conditions (a crushed cable) can result in shorted inputs. Active Fail-Safe detects the input short and drives the output high.

Active Fail-Safe functions over the entire receiver input common-mode range which is important with bus voltage biases, ground offsets or common-mode noise present.

Figure 7 illustrates the case with both receiver inputs shorted together. Since $\overline{\text{FAILSAFE}}$ is asserted, the output is high. Both pins are held initially at ground potential. Common-mode voltage spikes are then coupled onto both inputs. The output remains at logic high demonstrating Active Fail-Safe functions over the entire input common-mode range.

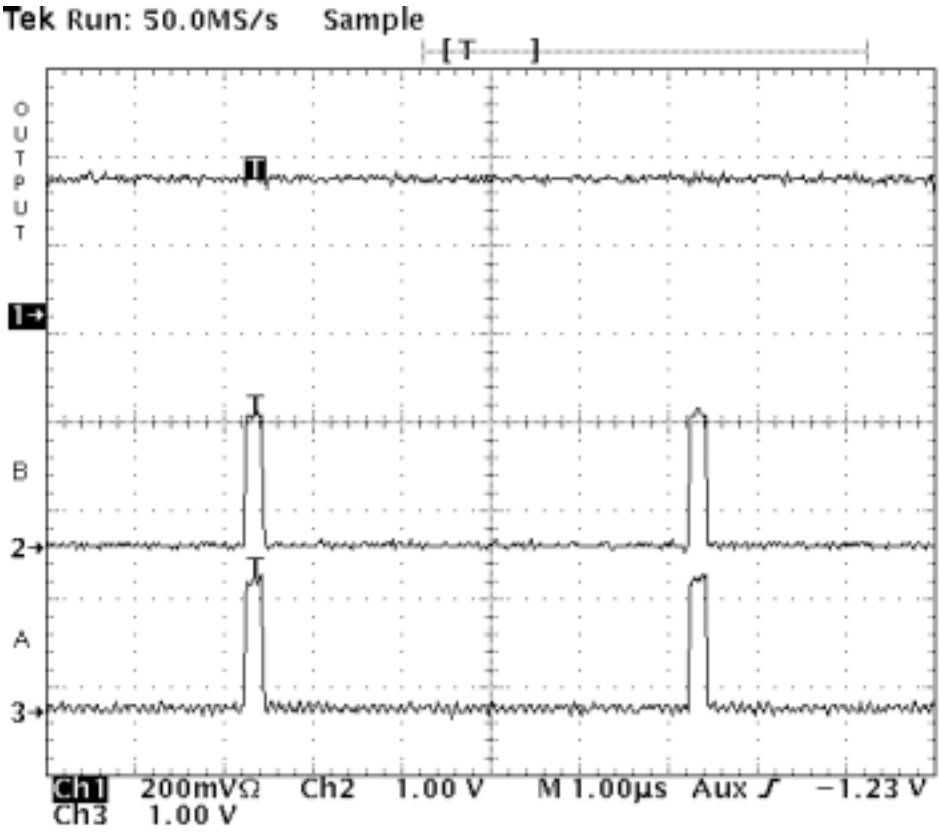

Figure 7. Common-Mode Fluctuations on Disconnected Line

3 Conclusion

This paper discusses an innovative type of fail-safe that overcomes the limitations seen in other fail-safe solutions. Active Fail-Safe presents minimal bus loading and therefore does not degrade the signal quality of the driver output as an external bias network would. Active Fail-Safe requires no internal offset in the signal path and therefore does not increase the input differential required for the receiver to switch, as do some integrated fail-safe solutions. Active Fail-Safe operates over the entire input common-mode range and assures a known state in the presence of common-mode noise, dc bias voltages, or system ground offsets.

The SN65LVDS32B Active Fail-Safe discussed in this paper in also available in the following TI devices:

- SN65LVDT32B
- SN65LVDS3486B
- SN65LVDT3486B
- SN65LVDS9637B
- SN65LVDT9637B
- SN65LVDS33
- SN65LVDS34
- SN65LVDT33
- SN65LVDT34

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