

LVDS Multidrop Connections

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ABSTRACT

This application report describes design considerations for low-voltage differential swing (LVDS) multidrop connections. The report describes the maximum number of receivers possible versus signaling rate, signal quality, line length, output jitter, and common-mode voltage range when multidrop testing on a single LVDS line driver transmitting to numerous daisy-chained LVDS receivers.

The LVDS receivers are wired to simulate a wire-wrapped or printed circuit backplane environment. The receivers are tested to monitor system response for different signaling rates and a varied number of receivers.

Contents

1	Introduction	3
2	Maximum Number of Receivers	3
2.1	Best Case Analysis	3
2.1.1	DC Electrical Models	3
2.1.2	Driver Analysis	4
2.1.3	Common-Mode Load	5
2.1.4	Differential Load	5
2.1.5	Receiver Input Leakage	5
2.2	Worst Case Analysis	6
2.2.1	TIA/EIA-644 Requirements	6
2.2.2	TI LVDS Characteristics	7
3	Maximum Signaling Rate Obstacles	7
3.1	Driver Output Loading	8
3.2	Intersymbol Interference	8
3.3	Skew in Parallel Buses	9
3.4	Termination	9
3.5	Allowable Jitter	10
3.6	External Noise Coupling	11
3.7	Common-Mode Voltage Range	11
4	Bench Verification	11
4.1	The Multidrop Setup	11
4.2	Equipment Setup	14
5	Measurement Results	16
5.1	Output Jitter From Receiver 36 With Different Cable Lengths	16
5.2	Output Jitter From a Single Point-to-Point Receiver	17
5.3	Output Jitter of Varied Load Conditions	18
5.4	Percent Output Jitter From Every Fourth Load	22
6	Conclusion	23

6.1 Receiver Number vs Cable Length	23
6.2 Receiver Number vs Signaling Rate	26
6.3 Receiver Number vs Common-Mode Voltage Range	29
7 References	30

List of Figures

1 Common Mode and Differential LVDS Bus Model	3
2 Differential Line Driver Model	4
3 Simplified LVDS Driver Model	4
4 Common Mode and Differential Driver Models	4
5 SN65LVDS31 Simplified Driver Model	5
6 SN65LVDS31 Common Mode and Differential Driver Models	5
7 Simplified SN65LVDS32 Receiver Model	6
8 SN65LVDS32 Common Mode and Differential Driver Models	6
9 Spec-Compliant 20 Receiver Model	7
10 Loading Effects at a Receiver Input	8
11 Data Error Pattern	9
12 Typical Eye Pattern	10
13 Multidrop System With TI LVDS Evaluation Modules	12
14 Berg Sticks Connected to One Receiver Channel on the EVM	13
15 Multidrop Bank of 36 Receivers	14
16 Test Setup With Instrumentation	15
17 Output Jitter From Receiver 36 With Different Cable Lengths	16
18 Output Jitter vs Signaling Rate at Different Cable Lengths	17
19 Output Jitter From a Single Point-to-Point Receiver	18
20 Output Jitter of a Nine Receiver Load Bank	19
21 Output Jitter of an Eighteen Receiver Load Bank	19
22 Output Jitter of a Twenty-Seven Receiver Load Bank	20
23 Output Jitter With a 1 m Cable and a Varied Number of Receivers	20
24 Output Jitter With a 3 m Cable and a Varied Number of Receivers	21
25 Output Jitter With a 10 m Cable and a Varied Number of Receivers	21
26 Output Jitter With a 30 m Cable and a Varied Number of Receivers	22
27 Percent Output Jitter From Every Fourth Load	23
28 Percent Output Jitter From Each Multidrop Load	24
29 Percent Output Jitter From a 35 Drop 21 ns Load	25
30 Output Jitter From an 18-Receiver 17.1 ns Load	25
31 Output Jitter From a 13-Receiver 12.3 ns Load	27
32 Output Jitter From a 15-Receiver 14.3 ns Load	27
33 Output Jitter From an 11-Receiver 10.4 ns Load	28
34 Load Propagation Delay vs Signaling Rate	29
35 Receiver Number vs Common-Mode Voltage Range	30

1 Introduction

The most commonly used data transmission system, or topology, is known as the *point-to-point* application. The term *point-to-point* is used to describe a unidirectional system that consists of a single line driver connected to a single line receiver, that transmits data from *point A* to *point B* using one *speaker* and one *listener*. The term *multidrop*, defines a topology where one driver transmits data to more than one receiver. The *multidrop* application is the equivalent of sending data from *point A* to *point B1*, *point B2*, *point B3*, etc., since with this application, one *speaker* may have a *whole room full of listeners*.

In data transmission circuits, the output voltage transition time of a line driver is often the limiting factor in determining a maximum signal rate. This is usually due to an output stage not being fast enough to provide a *decent* pulse, however data rate limitations are also related to noise margin, crosstalk, and radiated and conducted emissions. Many conventional line drivers have a single-ended output with a long, slow voltage swing of several volts. A signaling rate may be further constrained by the increase in power dissipation as the signaling rate increases.

2 Maximum Number of Receivers

Connecting multiple LVDS receivers to a single LVDS driver works well, but at some point, increasing the number of receivers overloads a single driver, and the system fails. The maximum number of receivers possible is examined in the following discussion with *best case* and *worst case* modeling.

2.1 Best Case Analysis

2.1.1 DC Electrical Models

The effect that multiple receivers have on a driver is calculated by examining the output model of an LVDS driver and the input model of an LVDS receiver. The common mode and differential models shown in Figure 1 represent an LVDS bus consisting of an LVDS driver, the interconnection, and the LVDS receiver.

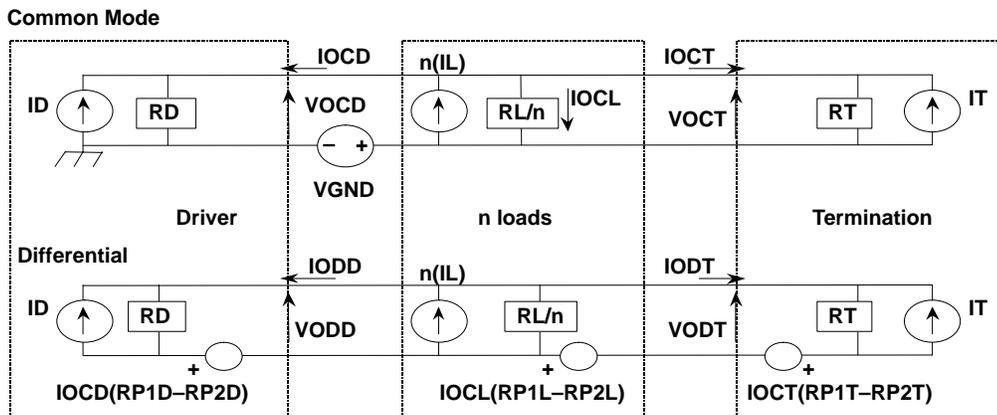


Figure 1. Common Mode and Differential LVDS Bus Model

2.1.2 Driver Analysis

Figure 2 displays an LVDS driver model from Annex C of the TIA/EIA-644 standard. The model is complex, but useful in developing a simplified differential line driver model for the examination of driver response to output load increases. For this purpose, the simple model of an SN65LVDS31 line driver is developed in Figure 3.

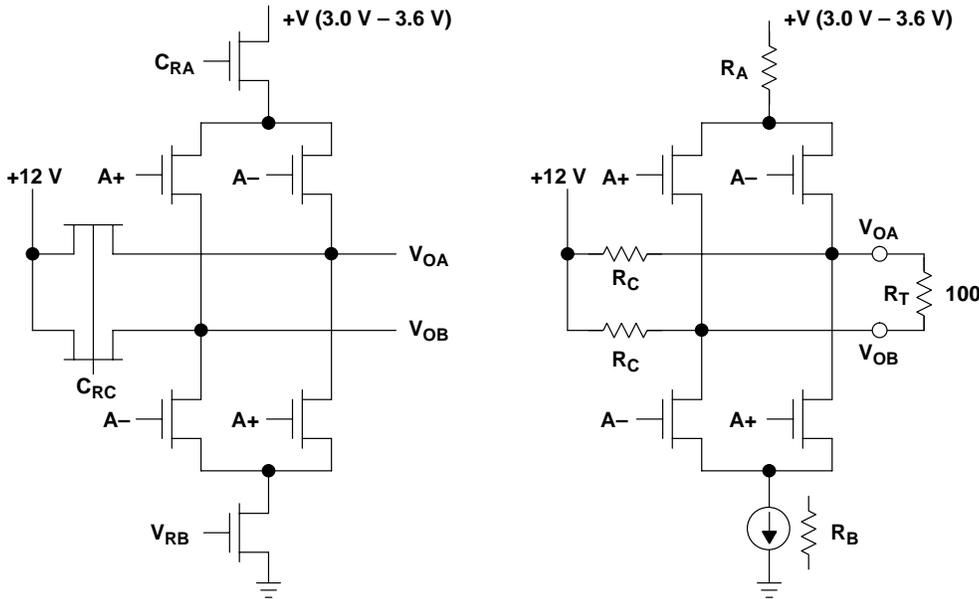


Figure 2. Differential Line Driver Model

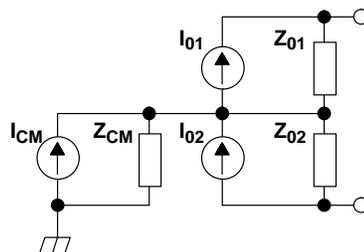


Figure 3. Simplified LVDS Driver Model

Output differential drive and common-mode offset models are derived from the simplified model of Figure 3 and modeled individually in Figure 4.

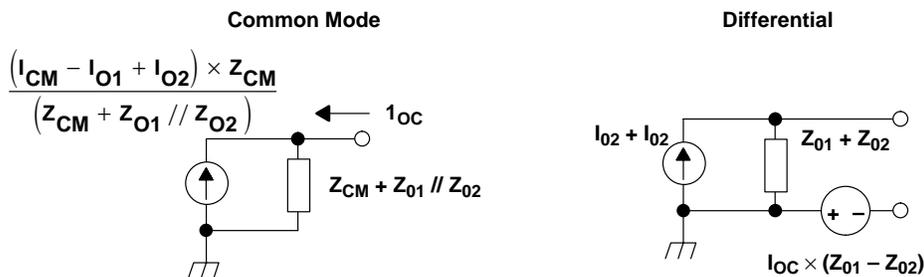


Figure 4. Common Mode and Differential Driver Models

Values are assigned to each source and impedance by using data sheet specifications and IBIS models for the SN65LVDS31. These values are obtained from a straight line approximation of the actual IBIS model and are shown in Figure 5.

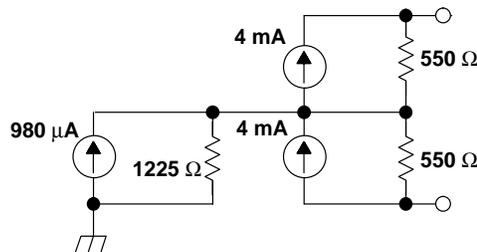


Figure 5. SN65LVDS31 Simplified Driver Model

Using the derived values in this model, individual common mode and differential models are developed in Figure 6.

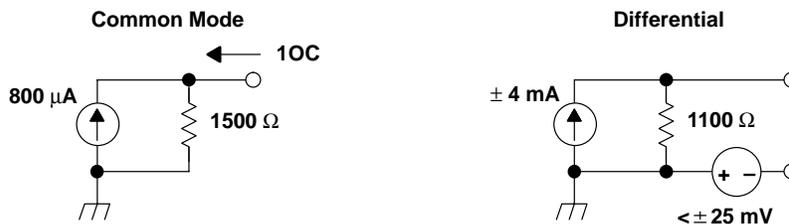


Figure 6. SN65LVDS31 Common Mode and Differential Driver Models

2.1.3 Common-Mode Load

The model for the common-mode output of the SN65LVDS31 shows the driver consists of a small current source and a 1500-Ω load develops a 1.2-Vdc common-mode voltage. The current source is capable of maintaining the 1.2 Vdc within the limits of the 800-μA source, but loads beyond this limit causes the common-mode output to shift.

2.1.4 Differential Load

The nominal driver output is modeled differentially as a 4-mA source with an output impedance of 1100-Ω load; the resulting (nominal) current is 3.66 mA at the termination resistor, producing a differential voltage (V_{od}) of 366 mV across the inputs of the receiver. The LVDS standard specifies a minimum differential voltage of 250 mV, which occurs if the termination resistance decreases to 67 Ω. The differential model also contains an offset voltage modeled as a 25-mV voltage source resulting from a mismatch of the individual outputs. This mismatch can cause the output voltage levels to change differentially by 50 mV as the current source varies. The open circuit differential-output voltage of the driver without the 100-Ω termination resistor does not remain at 4.4 Vdc, but ramps up to V_{cc} .

2.1.5 Receiver Input Leakage

The SN65LVDS32 simplified receiver model in Figure 7 and the common-mode and differential models of the receiver in Figure 8 are developed with the same derivation technique as the SN65LVDS31 driver.

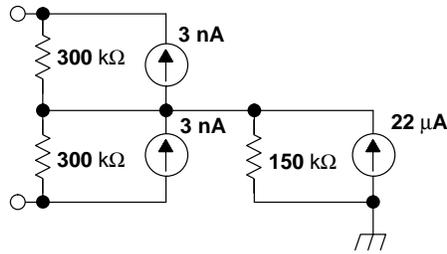


Figure 7. Simplified SN65LVDS32 Receiver Model



Figure 8. SN65LVDS32 Common Mode and Differential Driver Models

The receiver for the SN65LVDS32 models has an extremely high input impedance when compared to the 100-Ω termination resistor. The common-mode model has very little impact on the overall system when compared to the driver. The same is true of the differential model which is the equivalent of a 6-μA source compared to the 4-mA source of the drivers. It would take a large number of receivers (over 100) before the effects would interfere with the performance of an overall system.

2.2 Worst Case Analysis

2.2.1 TIA/EIA-644 Requirements

Although both devices modeled above meet the requirements of TIA/EIA-644, there are LVDS specifications that need to be addressed.

When the standard was developed, it was specifically intended for lower signaling rates and point-to-point applications, and LVDS signal *edges* running in high-speed applications like multipoint or multidrop were clearly not envisioned. As a result, parameters that would ultimately be affected by these new applications are not completely defined in the standard.

Two of these *undefined* parameters are the common-mode currents in an LVDS driver and receiver. The standard does define a common-mode voltage range via the ground potential difference voltage (V_{gpd}) of ± 1 Vdc, however the maximum allowable common-mode current between a driver and receiver(s) is yet to be defined.

Another parameter that does not lend itself to multipoint or multidrop applications is the leakage current out of (or into) each receiver pin, which is modeled for the SN65LVDS32 in Figure 7 as a 3-nA current source. The standard states that leakage current *shall not exceed* 20 μA. The direction for the current is not specified. Therefore the specification is met if one receiver pin has a leakage current of -20 μA, and the other pin 20 μA.

NOTE: Current leakage can occur with another manufacturer’s parts if the failsafe configuration of the receiver is based upon biasing one terminal high and the other terminal low.

Theoretically then, a resulting 40- μ A *loop* current is now working against the differential output voltage (V_{od}) of the driver. The nominal output of the driver model is 366 mV (4 mA across an equivalent resistance of 91.5 Ω) and the minimum allowable V_{od} for a driver is 247 mV, therefore a 40- μ A loop current leaves an operating margin of approximately 116 mV.

Utilizing this margin, 31 receivers (116 mV/3.66 mV per receiver) can be connected to the driver before dropping below the minimum V_{od} ; however, any desired margin lowers this number accordingly. For example, if a 50-mV noise margin and 50-mV ground potential difference margin are desired, the maximum number of receivers drops to 5. This condition, modeled with 20 theoretical LVDS receivers, is illustrated in Figure 9.

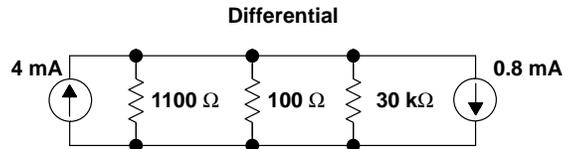


Figure 9. Spec-Compliant 20 Receiver Model

The 20 receivers establish a 0.8-mA current working against the differential voltage generated by the driver. The 20 resistors in parallel develop an equivalent system impedance of approximately 90 Ω , which results in a 288-mV difference voltage across the 100- Ω termination resistor, leaving little room for a system performance margin.

NOTE: The LVDS receiver is theoretical, and the values are used to demonstrate what could happen based upon the present LVDS standard. The LVDS committee reviewing the standard should address these issues.

2.2.2 TI LVDS Characteristics

Most LVDS receivers, including the SN65LVDS32, have both inputs pulled up through 300 k Ω resistors. Since both inputs are pulled up internally, the resulting loop current is the *difference* between the input leakage currents of each pin, and not the sum of the two currents as demonstrated in the example above, where nonTI parts are modeled.

Other manufacturers employ a configuration that results in a differential *loop* current very near the 40- μ A allowable limit. Although the devices meet the LVDS specification and work in point-to-point applications, they would not perform well in the multidrop application with a large number of drops.

3 Maximum Signaling Rate Obstacles

Many factors come into play when sending digital signals over copper wire at megabits-per-second rates. Signaling rates and bandwidth have increased dramatically in the last few years, and cable and connector manufacturers are struggling to keep pace with newer and faster silicon. While many of the factors affecting maximum signaling rate are nothing new, the problems they pose are a concern whether the signaling rate is kilobits-per-second or megabytes-per-second.

3.1 Driver Output Loading

The LVDS line driver converts a single-ended logic signal (LVTTTL) to the differential output levels and common-mode voltage specified in the LVDS standard. The voltage levels are required to drive the transmission line and termination resistor at the receiver input, but as transmission line length increases, so does its effect on the driver. The dc resistance of a CAT5 cable is specified (TIA/EIA-568-A) not to exceed 9.38 Ω/100 meters, which equates to a decrease of 35 mV in the V_{od} of an LVDS driver with a 100-m cable. However, the standard recommends a maximum distance for LVDS transmission of up to 30 m, which places the V_{od} loss in the range of 10 mV.

Cables also attenuate an ac signal (TIA/EIA-568A). The permissible attenuation allowed for a CAT5 cable may be derived with the following equation;

$$Attenuation(f) = 1.967\sqrt{f} + 0.023 \times f + \frac{0.050}{\sqrt{f}}$$

Where f is the applied frequency

Another consideration is a cable's characteristic impedance (Z_0). The TIA/EIA-644 LVDS specifies the use of 90-Ω to 132-Ω transmission lines (other values may be used in nonstandard applications). Since the output impedance of an LVDS driver is significantly greater than Z_0 , reflections are created as signals propagate from the device, creating a trade-off between driver power dissipation and output impedance matching the driver with the cable.

3.2 Intersymbol Interference

Maximum signaling rate is also affected by intersymbol interference (ISI). While this discussion is not restricted to the multidrop application, the effect may be more pronounced in a multidrop system due to the increased capacitive loading of multiple receivers on a transmission line. Capacitive loading induced ISI causes errors that are pattern (or data) dependent. The influence of ISI on a driver's output signal is shown in Figures 10 and 11.

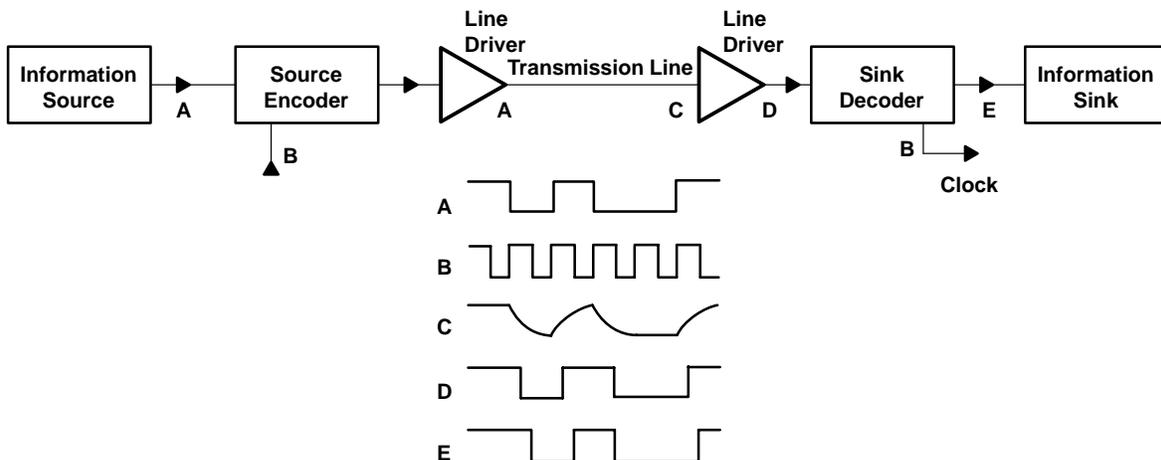


Figure 10. Loading Effects at a Receiver Input

Capacitive loading may not be as apparent at lower signaling rates because a signal has time to make the transition and settle to a steady-state level before the next transition occurs. At higher signaling rates, as shown in Figure 11, a signal may not have sufficient time to make a transition detectable by a receiver, resulting in data errors.

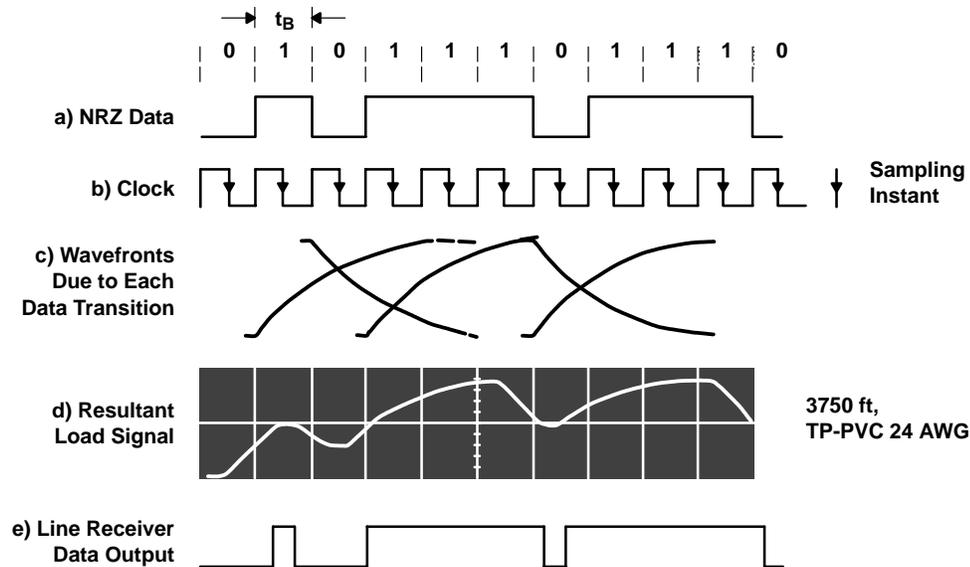


Figure 11. Data Error Pattern

3.3 Skew in Parallel Buses

The output of a SN65LVDS31 driver changes state in about 500 ps. The interconnection to a receiver greater than a few centimeters can be closely modeled as a resistive load and a time delay. Systems that use multiple LVDS drivers to form a parallel bus need the same time delay for all channels, as differences will cause a timing skew and possible data errors between channels. For example, consider a parallel bus system with a 400 Mbps signaling rate, a timing budget of 650 ps for the rising edge, 650 ps for the falling edge, and 1200 ps for the steady state level. If the propagation delay of the cable is 5 ns/meter, a 20 cm difference in cable length between two channels will cause a skew of 1 ns, or 40% of the timing budget. This problem becomes more manageable as many cable manufacturers now specify multiple twisted pair cables with a maximum skew between pairs, often listed as a difference in propagation delay between pairs of conductors per unit length of cable.

3.4 Termination

The transmission line between driver and receiver is terminated at the receiver input, with a resistance approximately equal to the line's characteristic impedance, for two reasons. First, an LVDS driver is a current mode device and the differential voltage is generated at the receiver inputs across this termination resistor. Secondly, almost all transmission systems require some type of termination to minimize reflections back into the line. Higher frequency components (fundamental and harmonic) reflect back to the source if termination resistance does not closely match the characteristic impedance of a transmission line. While allowable reflection in a system depends upon its design and tolerable noise margin, matching the nominal characteristic impedance of the cable to $\pm 10\%$ of the termination resistor value is generally sufficient. The TIA/EIA-644 specifies termination within the range of 90 Ω to 132 Ω , or a nominal value of 100 Ω across the inputs of an LVDS receiver.

A termination resistor is placed across the inputs of the last receiver in a multidrop application, which means that ideally, balanced driver current flows through the entire transmission line. Although other receivers connected to the line do not draw significant current, the connectors and short lines to each of the additional receivers create *stubs* on the transmission line. Each of these stubs is modeled as a small lumped capacitance attached to the line, creating a mismatch at that point on a transmission line. It is difficult to maintain the characteristic impedance of a line after the first stub, and the small mismatch increases with each successive *drop* along the line. The overall effect results in a degraded signal quality, slower signal transitions, and an increase in intermodulation products. It is therefore evident that a maximum possible signaling rate decreases as system noise and signal jitter increases with each additional drop.

3.5 Allowable Jitter

The required quality of a signal leaving a receiver is ultimately dictated by the quality of the downstream equipment in a system. Signal quality is not a major concern if the downstream equipment is high-end decoding equipment with error correction and calibration capabilities. However, if downstream equipment is low end, then the quality of the receiver output may need to be extremely *clean*.

The most common method of quantifying signal quality is by measuring jitter in the eye-pattern of a receiver's output. An eye-pattern includes all the effects of systemic and random distortion and reveals the time during which a signal may be considered valid. A typical eye-pattern is shown in Figure 12.

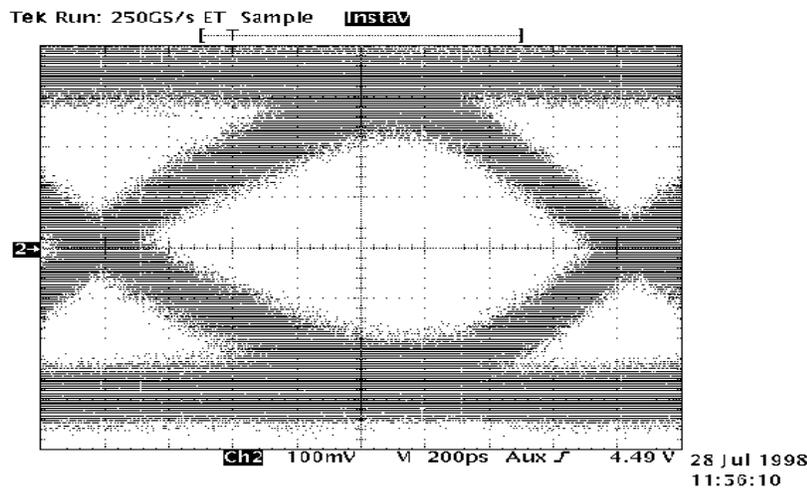


Figure 12. Typical Eye Pattern

The jitter values obtained from eye-pattern measurements are often reported as *percent jitter*, the percentage of time that jitter takes out of each bit.

$$\text{Percent Jitter} = \frac{\text{Absolute Jitter}}{\text{Time Unit Interval}} \times 100$$

The time unit interval (UI) is the reciprocal of the signaling rate, therefore percent jitter represents the portion of UI during which a logic state should be considered indeterminate.

3.6 External Noise Coupling

One of the benefits of LVDS is the superior noise immunity of the balanced differential interface between driver and receivers. This benefit outweighs the fact that two wires and connector pins are required for data transmission. The effects of noisy environments and interference from other equipment are minimized because transient noise and spikes are coupled onto both conductors at the receiver input. The receiver responds to the *difference* in signal levels across the input and this transience is present on both input conductors, it is essentially ignored and has minimal impact on system performance. While differential signaling has this advantage over single-ended signaling, both techniques are still susceptible to the other external noise sources.

3.7 Common-Mode Voltage Range

Another obstacle of concern is ground potential differential voltage (V_{gpd}), which occasionally occurs when the driver and receiver are in different locations with separate power supplies. When the ground reference of the driver's and receiver's power supplies is not common, a dc offset between the driver and receiver may develop. The LVDS standard addresses this problem by requiring that any dc offset stay within a ± 1 -V_{dc} range, a 3.3-V LVDS system may require that a dedicated ground line or *water-pipe* ground be used between the driver's and receiver's power supplies.

4 Bench Verification

Now that the major obstacles limiting signaling rate have been addressed, the LVDS multidrop system is examined on the bench.

4.1 The Multidrop Setup

A basic multidrop system consists of one LVDS driver connected to multiple LVDS receivers. TI's LVDS evaluation module (EVM) is shown in Figure 13.

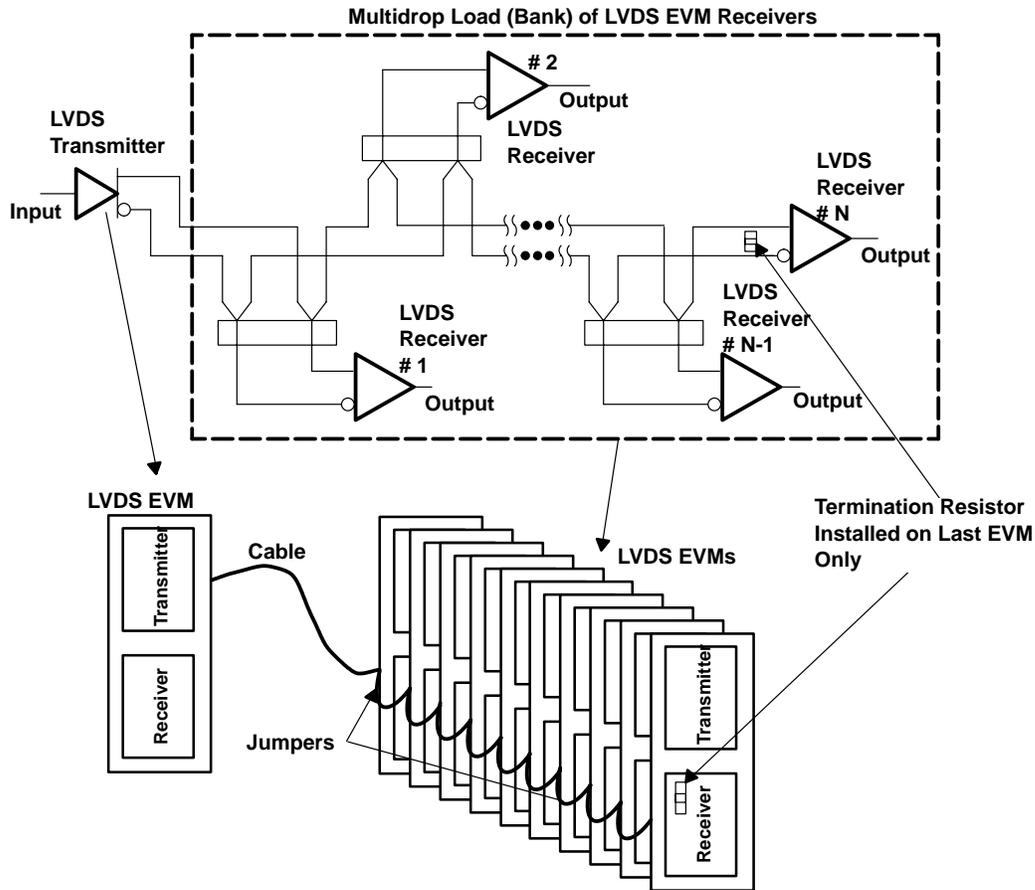


Figure 13. Multidrop System With TI LVDS Evaluation Modules

The EVM is constructed with SMA connectors on one receiver channel. The remaining channel connections lead to empty solder pads on the edge of the board. Two-wire terminal posts (*Berg Sticks*[™]) are soldered to two of the receiver's edge pads. These posts facilitate the two-wire connection to an adjacent EVM receiver channel, providing for a *daisy-chain* of 36-receiver channels. Figure 14 is a closeup of the *Berg Sticks* installed on one EVM.

Berg Sticks is a trademark of Berg Electronics.

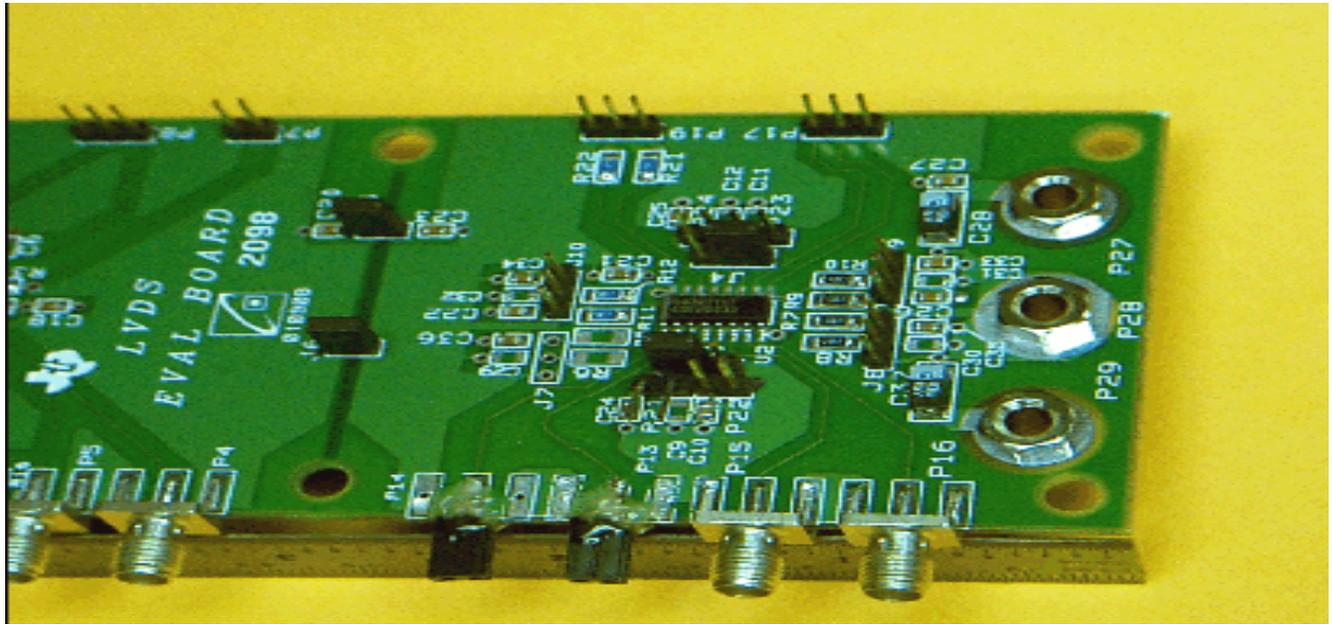


Figure 14. Berg Sticks Connected to One Receiver Channel on the EVM

The 36 EVMs are bolted together with threaded rod, slid through the banana jack connectors of each EVM, then fitted with flat washers and nuts on both sides of each EVM. This creates the equally spaced multidrop bank of 36 receivers shown in Figure 15. Power (V_{CC} and ground) is then applied to the bank by connecting a dedicated supply to the metal rods. Thirty-five 7.62 cm (3") length twisted pair wires are used as jumpers from one receiver connection to the next. A 100- Ω termination resistor is installed between the inputs of the last (farthest) EVM. Another EVM is set up as the *driver*, mounted and powered separately from the *load bank* of receivers.

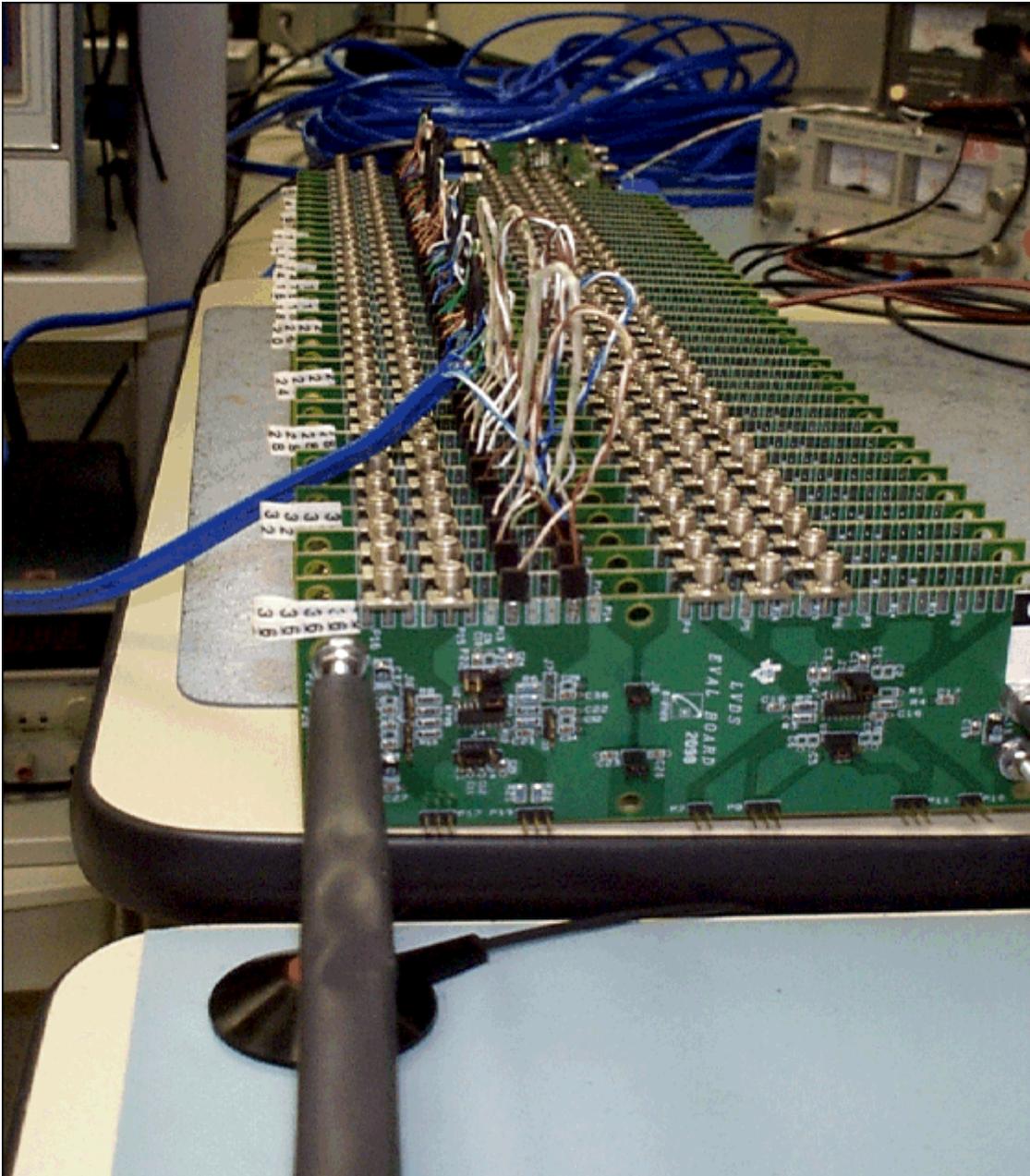


Figure 15. Multidrop Bank of 36 Receivers

4.2 Equipment Setup

The Tektronix HFS-9003 signal generator in Figure 16 (top shelf on the left), employed as the signal source for the multidrop system is adjusted as follows:

- Pattern: NRZ, pseudo-random binary sequence (PRBS)
- Input high level: 2.7 Vdc
- Input low level: 0.0 Vdc
- Slew rate: 800 ps

The Tektronix HFS-9003 signal generator is capable of generating a pseudo-random binary sequence (PRBS) data pattern at signaling rates up to 630 Mbps, with data patterns not repeated in the same sequence for $2^{16}-1$ (64K) bits. The setup is monitored with the Tektronix 784D oscilloscope on the right side of the photo, and powered with the two small Hewlett Packard power supplies on the bench behind the load bank. One of these supplies the driver, while the other supplies the load bank, with both set to 3.3 Vdc.

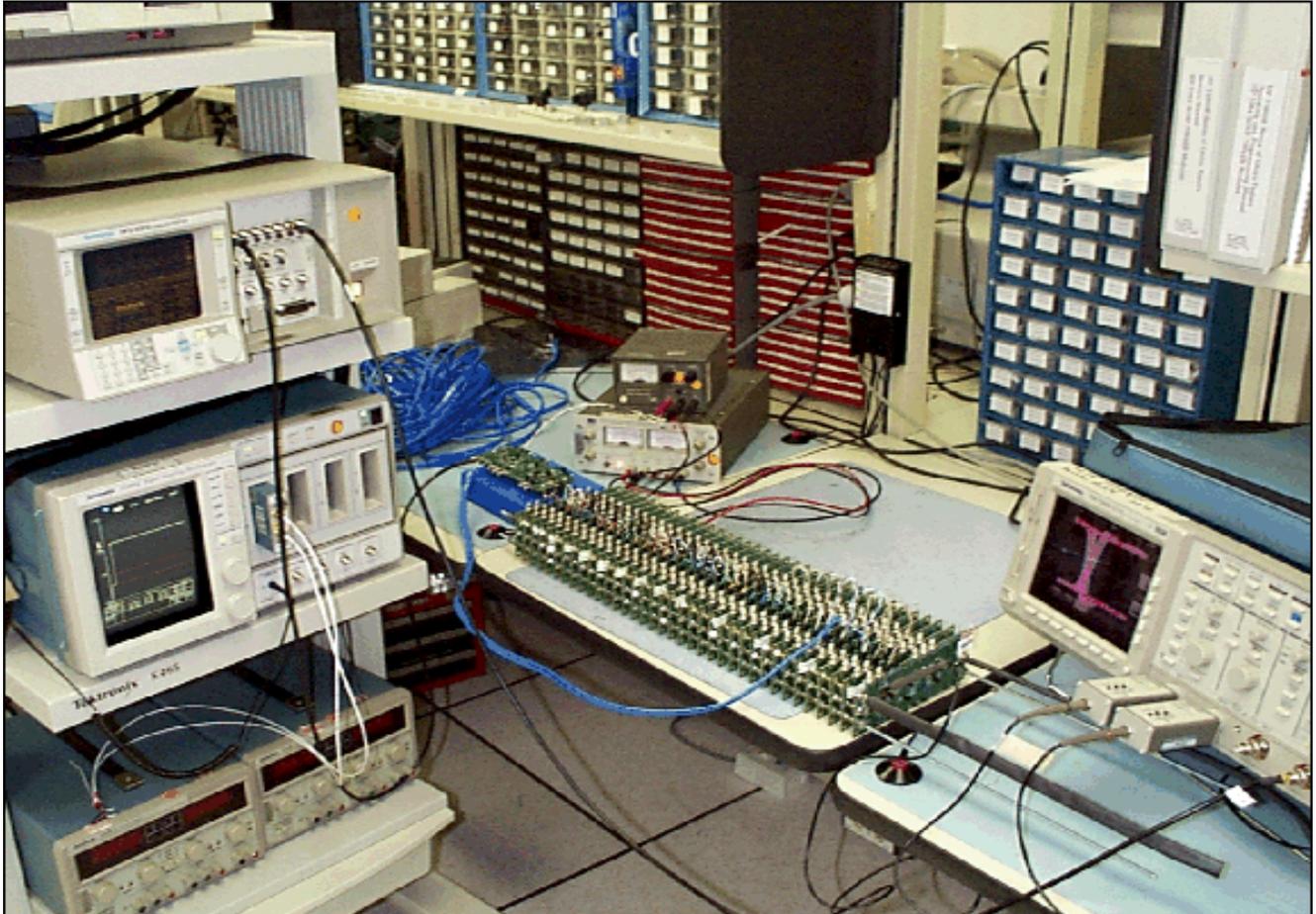


Figure 16. Test Setup With Instrumentation

At high data rates, the influence of equipment used to measure a signal of concern should be minimized, therefore probe heads should behave like a low-capacitance, high-impedance load with high bandwidth. For this test, the Tektronix 784D oscilloscope and Tektronix P6247 differential probes are used, since both scope and probe have a bandwidth of 1 GHz and a capacitive load of less than 1 pF. For signals in the range of 400 Mbps and above, an even higher bandwidth is recommended (as a rule of thumb, the fifth harmonic, i.e. 2 GHz, should be able to be detected), but at this time, no faster differential probe head is available.

The problems associated with the triggering jitter are eliminated by using a separate output channel from the HFS-9003, as the trigger source for the TDS784D oscilloscope.

The transmission cable is a Belden MediaTwist™ (CAT5) cable containing four unshielded twisted pair (UTP) conductors. The jumpers used to connect each receiver together are constructed by cutting nine 7,62 cm (3") pieces of MediaTwist, removing the four pieces of twisted pair from each piece, then stripping about a half inch of insulation from both ends of each twisted pair.

5 Measurement Results

Four series of tests are completed in order to determine the receiver number vs cable length and the receiver number vs signaling rate:

- Output Jitter vs Signaling at Different Cable Lengths
- Output Jitter From a Single Point-to-Point Receiver
- Output Jitter of Varied Load Conditions
- Output Jitter Percent From Every Fourth Load

5.1 Output Jitter From Receiver 36 With Different Cable Lengths

The first series of signal length (Mbps) measurements are taken between the driver and the 36th receiver load bank. The measurements are performed using varied lengths of cable to examine the system response to all 36 of the EVM receivers.

- Insert the 100 m cable connectors into the driver EVM Berg-Stick connectors.
- Insert the 100 m cable connectors into the first driver EVM Berg-Stick connectors (Receiver 1).
- Record data from the 36th EVM receiver for each signaling rate (Mbps) Figure 17.
- Shorten the cable (90 m, 80 m through 1 m) between the driver and the receiver load bank.
- Repeat the series of signal length (Mbps) measurements for each cable length and record the data.

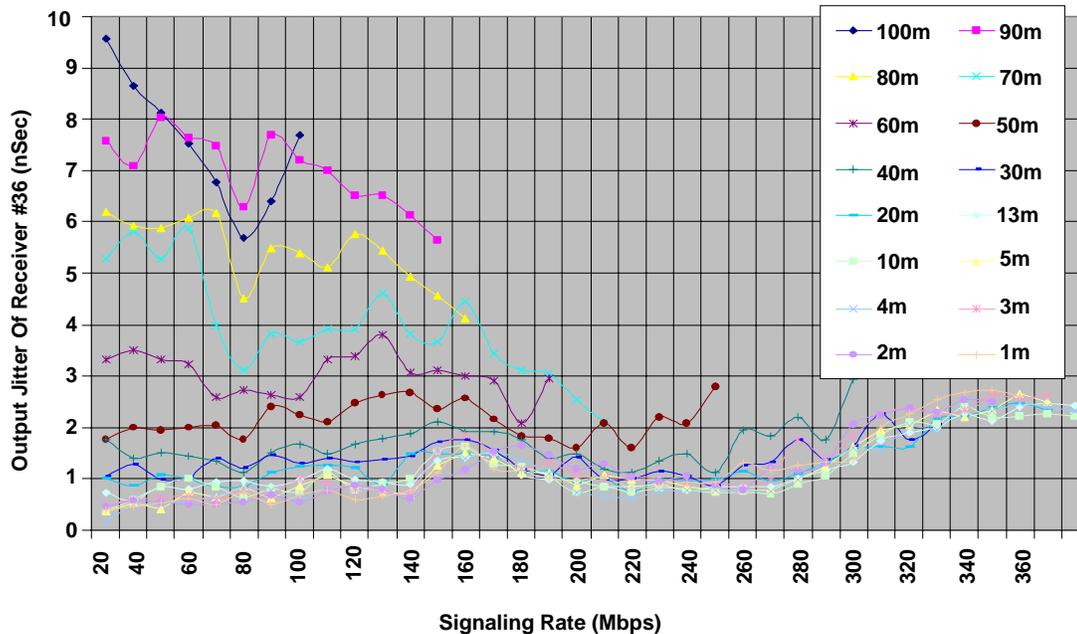


Figure 17. Output Jitter From Receiver 36 With Different Cable Lengths

MediaTwist is a trademark of Belden Wire and Cable Company.

The results of the tests are presented in Figure 17 and clearly show that output jitter is proportional to cable length, but the data format is not in the *conventional* format for percent jitter. In Figure 18 the same data is replotted as percent jitter.

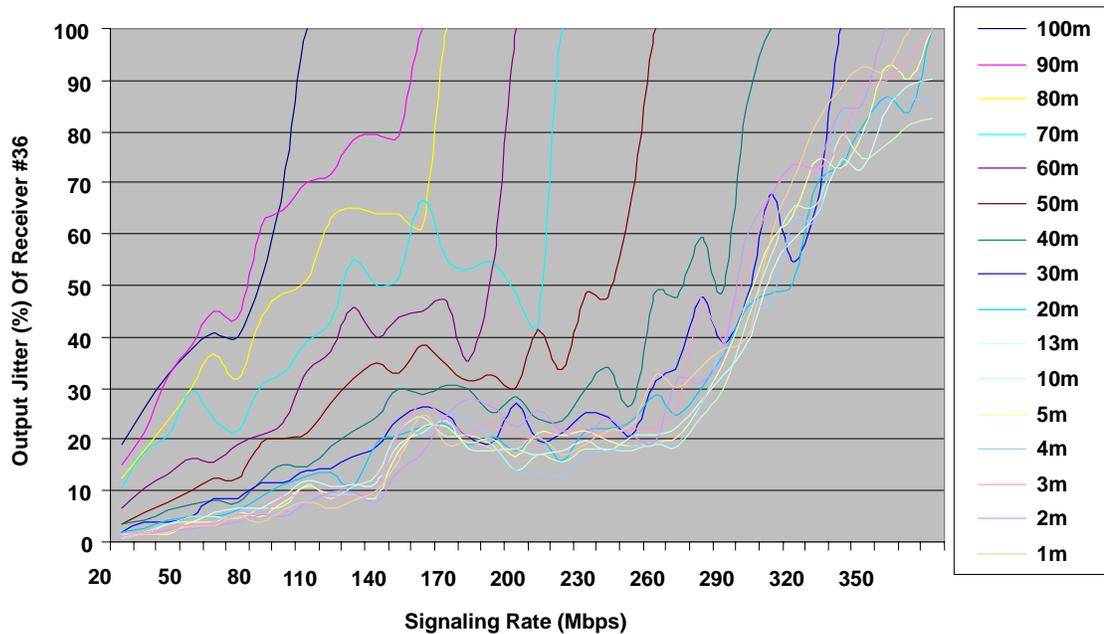


Figure 18. Output Jitter vs Signaling Rate at Different Cable Lengths

5.2 Output Jitter From a Single Point-to-Point Receiver

The second series of signal length (Mbps) measurements are taken between the driver and the 36th EVM receiver only. The measurements are performed using varied lengths of cable to examine the system response to the 36th EVM receiver only.

- Remove the jumper wires between the 35th and 36th EVM receivers.
- Insert the 30 m cable connectors into the driver EVM Berg-Stick connectors.
- Insert the 30 m cable connectors into the 36th EVM receiver Berg-Stick connectors.
- Record data from the 36th EVM receiver for each signaling rate (Mbps) Figure 19.
- Shorten the cable (10 m, 3 m, and 1 m) between the driver and the 36th EVM receiver.
- Repeat the series of signal length (Mbps) measurements for each cable length and record the data.

The results of the tests are presented in Figure 18.

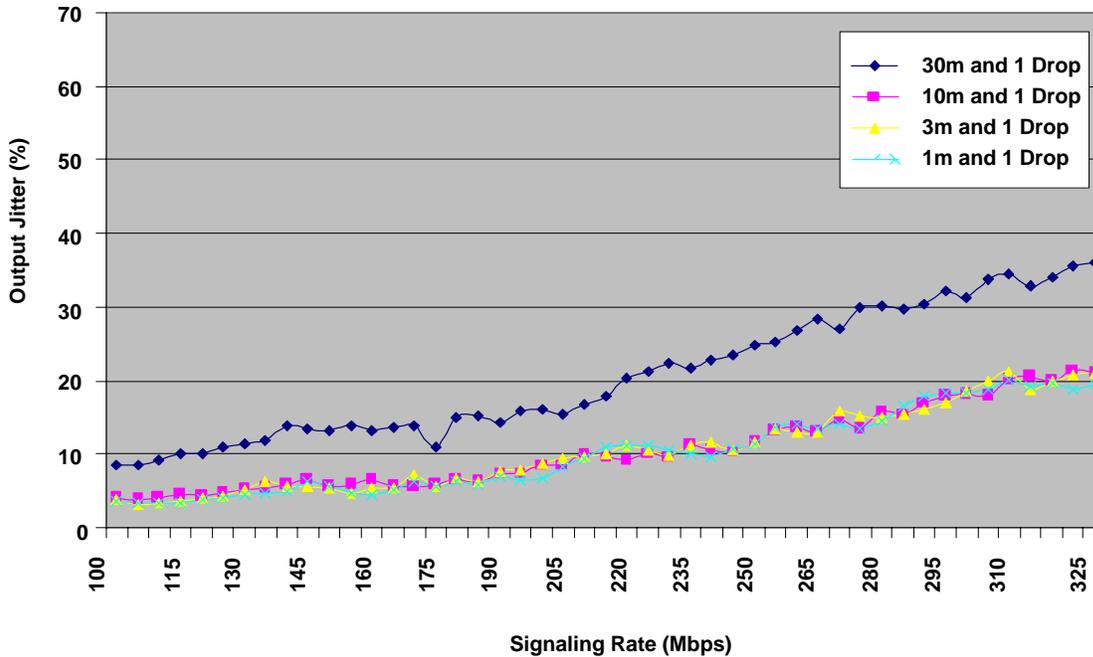


Figure 19. Output Jitter From a Single Point-to-Point Receiver

5.3 Output Jitter of Varied Load Conditions

The third series of signal length (Mbps) measurements are taken between the driver and varied EVM receiver load drops. The measurements are performed using varied lengths of cable to examine the system response to the varied EVM receiver load drops.

- Remove the jumper wire between the ninth and tenth EVM receivers.
- Insert the 30 m cable connectors into the driver EVM Berg-Stick connectors.
- Insert the 30 m cable connectors into the ninth EVM receiver Berg-Stick connectors.
- Record data from the ninth EVM receiver for each signaling rate (Mbps) Figure 20.
- Shorten the cable (10 m, 3 m, and 1 m) between the driver and the ninth EVM receiver.
- Repeat the series of signal length (Mbps) measurements for each cable length and record the data.
- Remove the jumper wire between the 18th and 19th EVM receivers.
- Insert the 30 m cable connectors into the driver EVM Berg-Stick connectors.
- Insert the 30 m cable connectors into the 18th EVM receiver Berg-Stick connectors.
- Record data from the 18th EVM receiver for each signaling rate (Mbps) Figure 21.
- Shorten the cable (10 m, 3 m, and 1 m) between the driver and the 18th EVM receiver.
- Repeat the series of signal length (Mbps) measurements for each cable length and record the data.
- Remove the jumper wire between the 27th and 28th EVM receivers.
- Insert the 30 m cable connectors into the driver EVM Berg-Stick connectors.

- Insert the 30 m cable connectors into the 27th EVM receiver Berg-Stick connectors.
- Record data from the 27th EVM receiver for each signaling rate (Mbps) Figure 22.
- Shorten the cable (10 m, 3 m, and 1 m) between the driver and the 27th EVM receiver.
- Repeat the series of signal length (Mbps) measurements for each cable length and record the data.

The results of the tests are presented in Figures 20, 21, and 22.

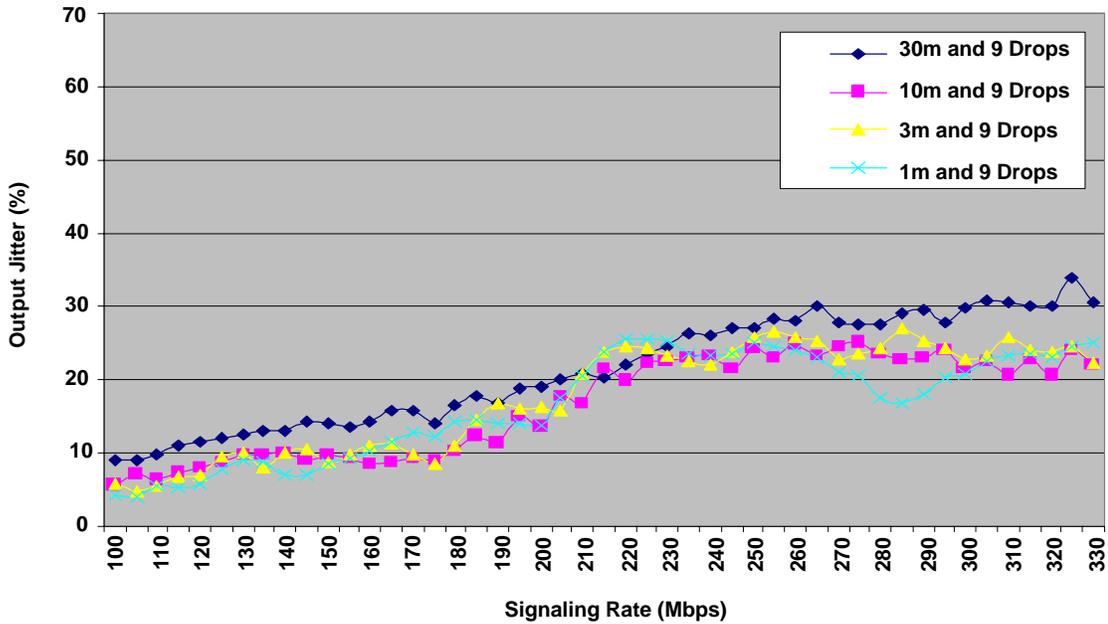


Figure 20. Output Jitter of a Nine Receiver Load Bank

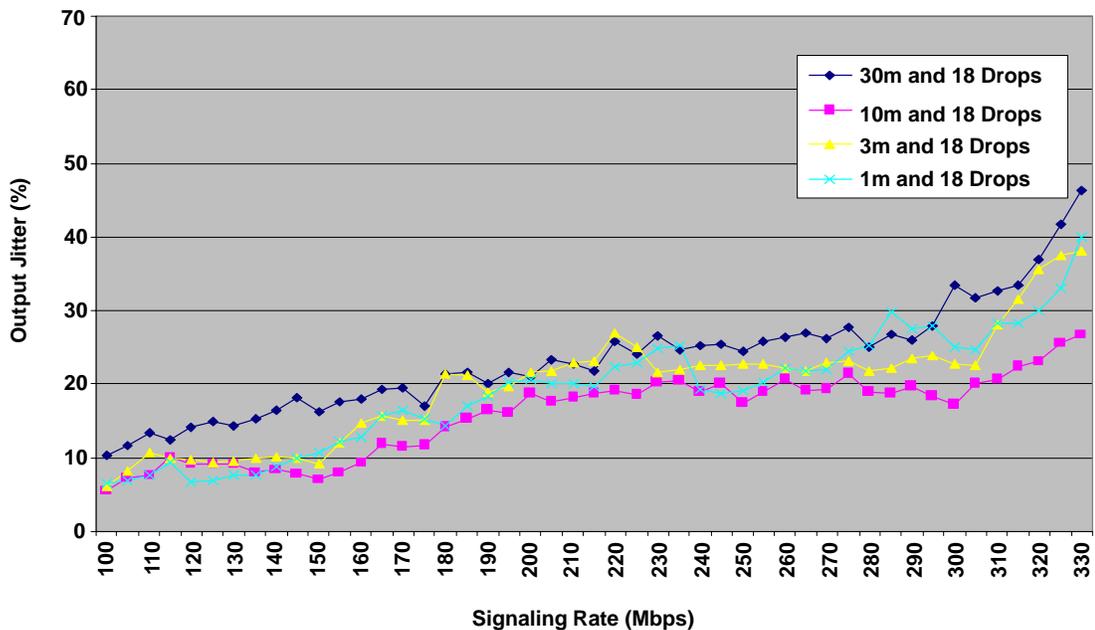


Figure 21. Output Jitter of an Eighteen Receiver Load Bank

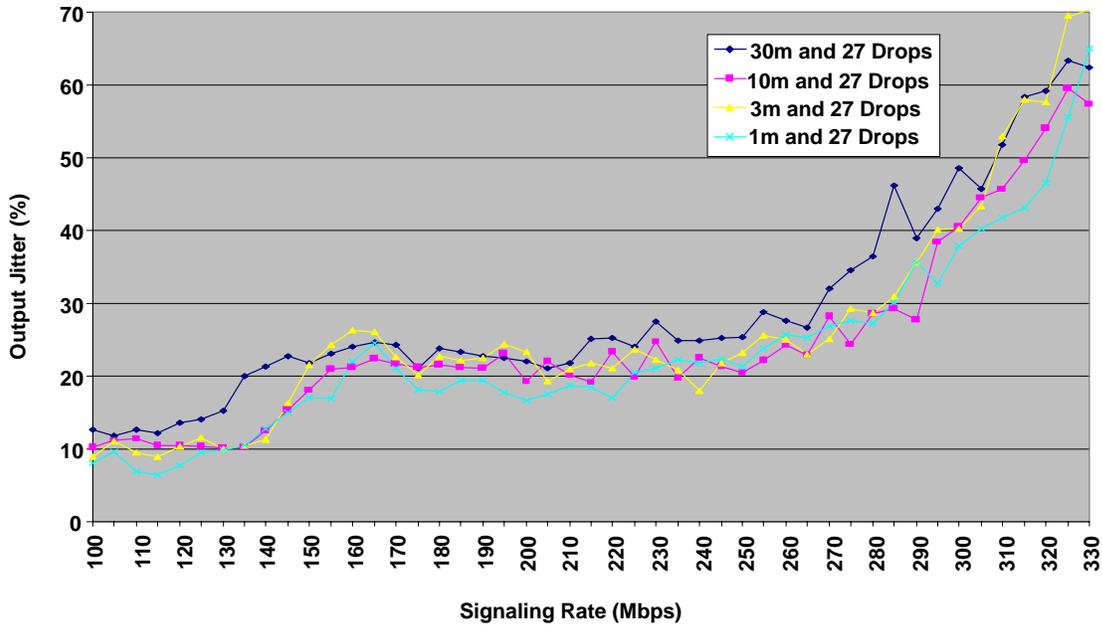


Figure 22. Output Jitter of a Twenty-Seven Receiver Load Bank

Combine the jitter data test results from all three series of tests (Figures 18 through 22). Examine the effect of an increasing number of loads at a fixed cable length Figures 23 through 26.

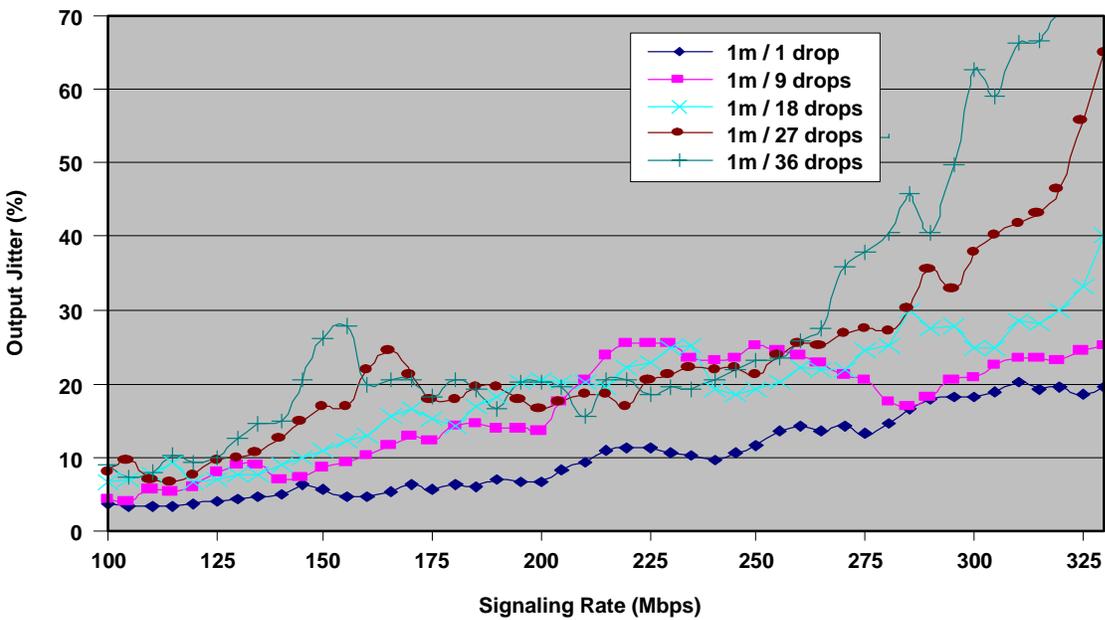


Figure 23. Output Jitter With a 1 m Cable and a Varied Number of Receivers

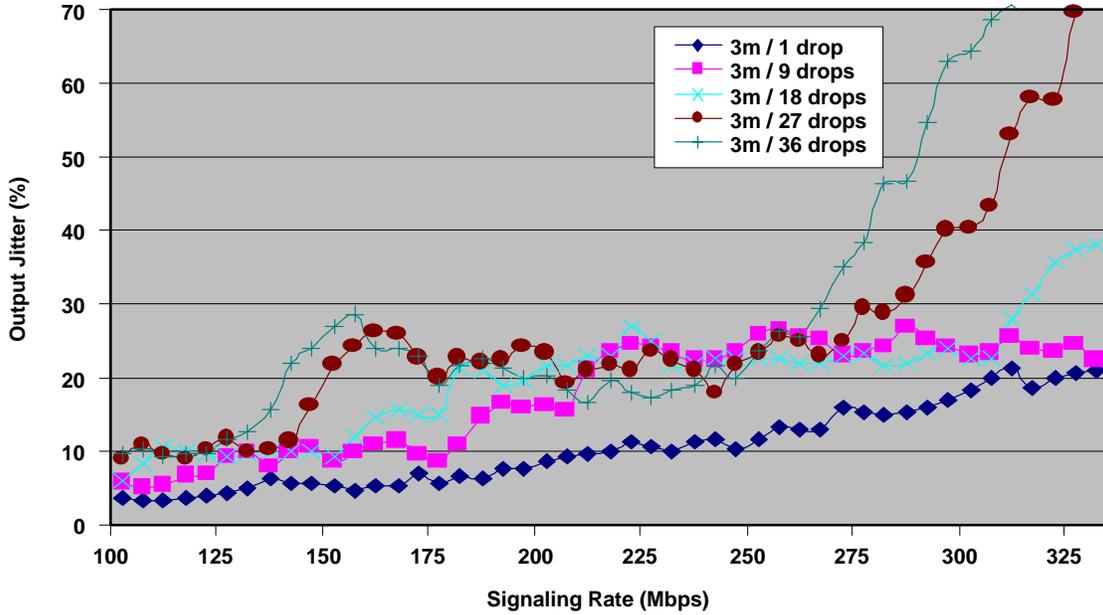


Figure 24. Output Jitter With a 3 m Cable and a Varied Number of Receivers

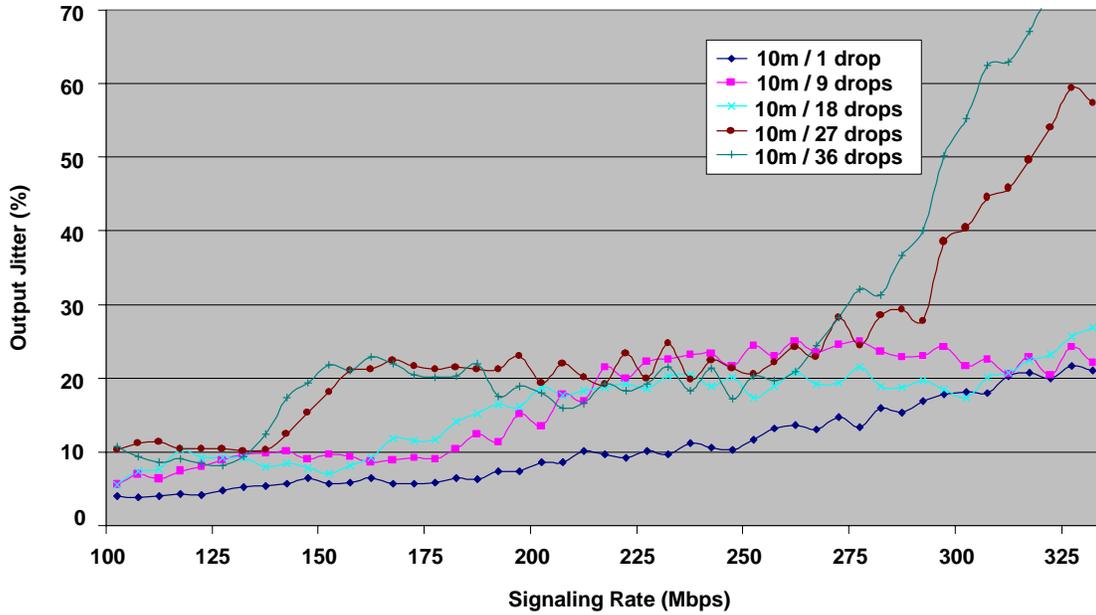


Figure 25. Output Jitter With a 10 m Cable and a Varied Number of Receivers

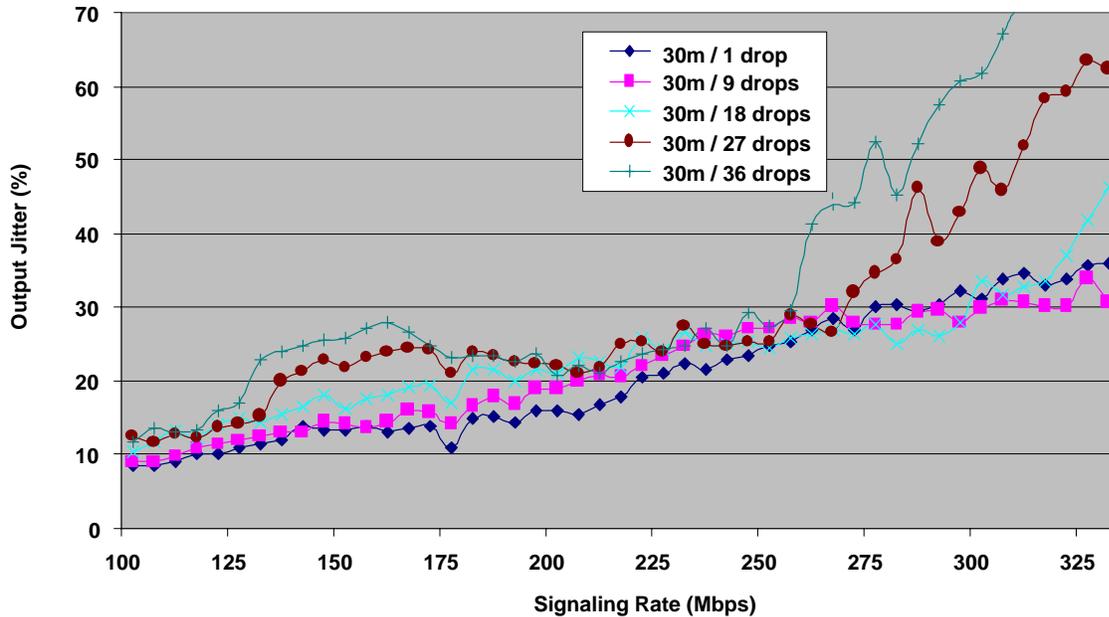


Figure 26. Output Jitter With a 30 m Cable and a Varied Number of Receivers

5.4 Percent Output Jitter From Every Fourth Load

The fourth series of signal length (Mbps) measurements are taken first between the driver and the first EVM receiver only, then from every fourth EVM receiver in the 36 EVM receiver load bank. The measurements are performed using a 15,24 cm (6") cable. The HFS-9003 is adjusted for a signaling rate of 50 Mps, then incremented in 50 Mps steps to 300 Mps, measuring the output jitter at each increment.

- Remove the jumper wires between the first and second EVM receivers.
- Insert the six-inch cable connectors into the driver EVM Berg-Stick connectors.
- Insert the six-inch cable connectors into the first EVM receiver Berg-Stick connectors.
- Adjust the HFS-9003 signaling rate to 50 Mps
- Record data from the first EVM receiver for each signaling rate (Mbps) Figure 27.
- Adjust the HFS-9003 signaling rate in increments of 50 Mps, up to 300 Mps, and measure the output jitter at each increment.
- Connect the jumper wires between the first and second EVM receivers.
- Continue testing every fourth EVM receiver load in the 36 EVM receiver load bank.

The results of the tests are presented in Figure 27.

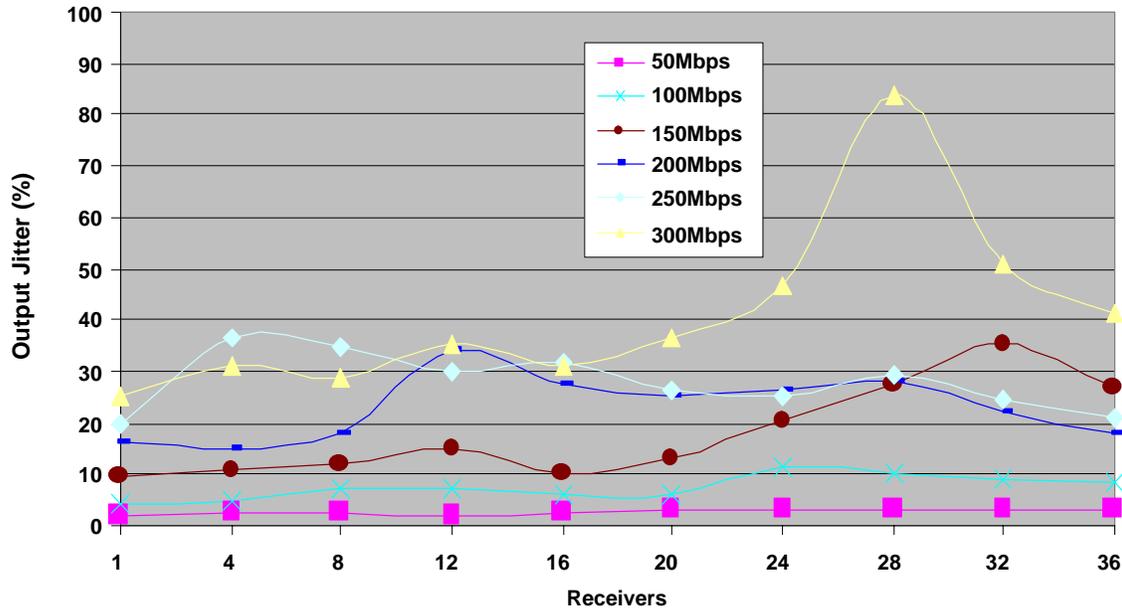


Figure 27. Percent Output Jitter From Every Fourth Load

6 Conclusion

This report provides basic design guidelines and recommendations for determining operating margins, distance between the transmitter and the receivers, and the optimal signaling rates to the number of LVDS receivers.

6.1 Receiver Number vs Cable Length

While the effect of increased cable length is apparent in Figure 18, performance of the shorter length cables (30 m) indicates that load number impacts a system as much as cable length. This is obvious when the multidrop system plots in Figure 18 are compared with the single point system plots in Figure 19. The point at which each plot crosses the 20% jitter line in Figure 20 through Figure 22 clearly demonstrates this increased loading effect.

Not as obvious in Figure 20 through Figure 22 is that the longer cables in these plots appear to both delay and attenuate reflected signals more than the shorter cables. It appears that although cable length increases jitter, length seems to reduce the high and low peaks of the output jitter caused by jumpers and stubs in the load bank. Figure 23 through Figure 26 display this unexpected characteristic with a decrease in the dramatic fluctuations of the 1 m and 3 m plots, on the 10 m and 30 m plots. The longer cables effectively smooth out the minimum and maximum peaking evident in the shorter lengths, however overall performance of the system still degrades rapidly with increased cable length.

Figure 27 illustrates the fact that data taken at the last receiver (EVM #36), does not represent the worst case jitter in the load bank. It appears that the stub lengths and connectors along the load contribute noise and jitter to the system, but the fact that the slope is negative between loads 32 and 36 implies that the termination at the last load attenuates jitter. The positive slope of the first four loads (except at 200 Mbps) indicates that the cable and driver also attenuate system jitter generated along the load bank. These effects are amplified in the higher signaling rates.

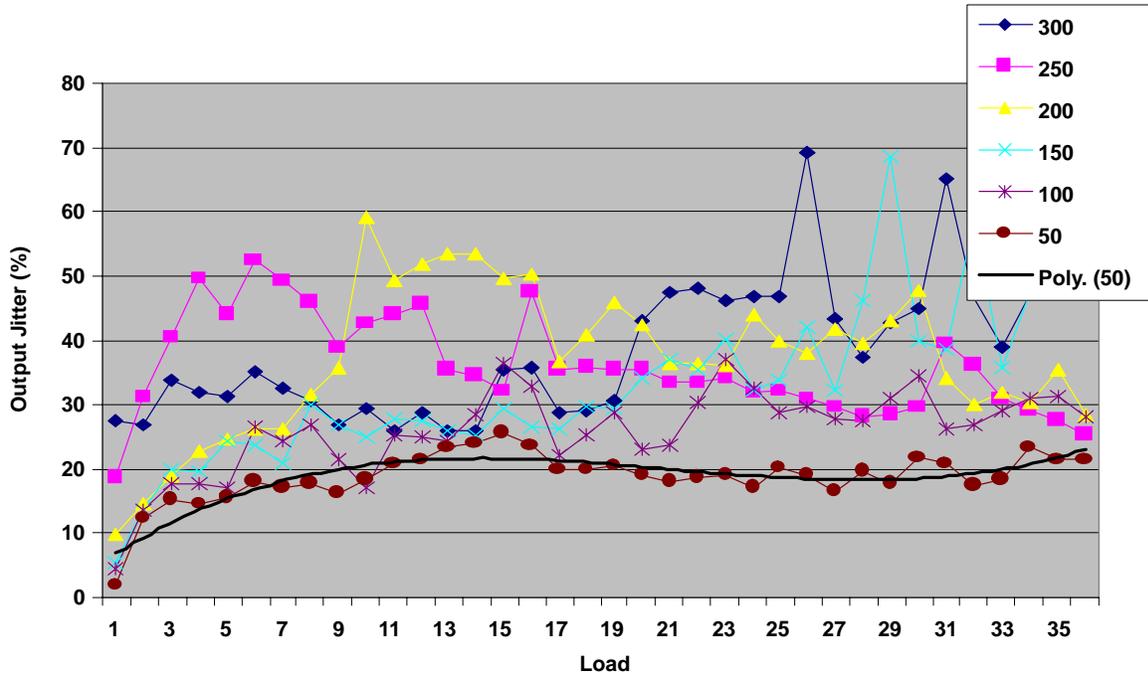


Figure 28. Percent Output Jitter From Each Multidrop Load

An examination of possible attenuation by the transmission cable and driver with a 1 m cable is recorded in Figure 28 as the output jitter from each load. These results again present a positive slope at the beginning of the load bank and a negative slope at the end. While a gradual noise increase is expected with an increase in cable length, clearly this extra noise is being generated by the stub and connectors along the load bank.

It is also apparent that jitter levels shift along the load bank as the signaling rate is changed, establishing a *characteristic wave* of the load bank. The number of loads and the propagation delays introduced by the cables between receivers directly influence this wave, which in the test setup are the 7,62 cm (3") jumpers between EVMs. Based on these results, measurements of the propagation delay are made across the entire load bank. The fundamental and harmonic signaling rates related to this delay are examined.

A delay of 20.9 ns is measured from the output of the first receiver (#1) to the output of the last receiver (now #35 since the receiver output pins on one of the loads was damaged during the previous test). This 20.9 ns delay equates to a characteristic signaling rate of 47 Mbps (1/21 ns), and a third harmonic of 141 Mbps. If a standing wave is being generated along the load bank, then this wave should shift along the load bank as the signaling rate is changed.

Increasing the signaling rate in quarter-wave increments of 12 Mbps, the next series of tests are performed with an initial signaling rate of the third harmonic. The second test is performed with the signaling rate increased to 155 Mbps, then increased again to 167 Mbps, and finally 179 Mbps. The results are plotted with third order poly nominal trend lines in Figure 29, employed to examine the wave more clearly.

Next, the load bank is reconfigured to approximate the same characteristic wave using half the number of receivers (#19 – #36) and doubling the line length between EVMs from 7,62 cm (3") to 15,24 cm (6"), using a 1 m cable from the driver to EVM #19. This should create a load bank of 18 receivers with a propagation delay somewhere near the original.

The delay between the output of the first load (#19) and the last load (#36) is 17.2 ns, corresponding to a characteristic rate of 58 Mbps. As done previously, the third harmonic with quarter wavelength increases in the signaling rate are now applied to the driver, with results plotted in Figure 30.

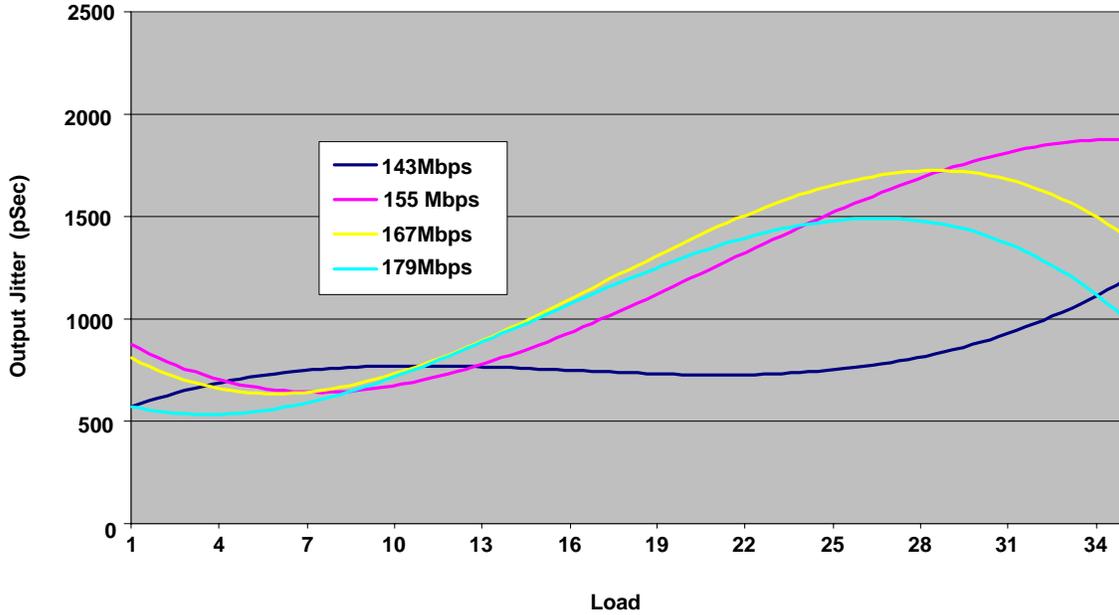


Figure 29. Percent Output Jitter From a 35 Drop 21 ns Load

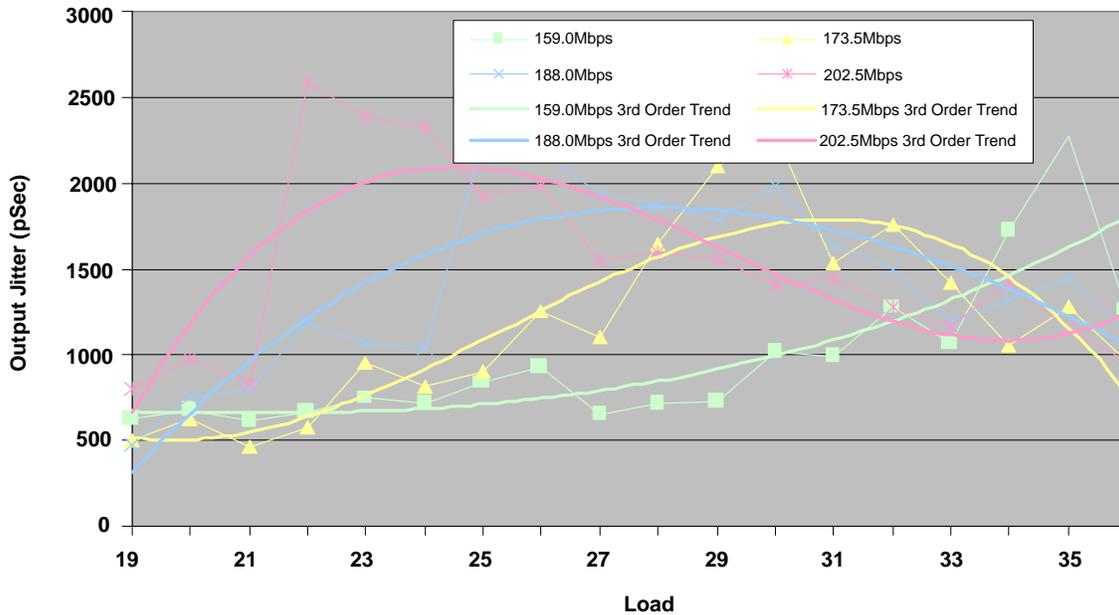


Figure 30. Output Jitter From an 18-Receiver 17.1 ns Load

The wave, generated by reflections from connectors and stubs present on each EVM, shifts along the load bank as a function of the signaling rate. The output jitter of the first load *is* not the worst case, and the output jitter from the last load *may* not be the worst case in a system.

A closer examination of another source of jitter is made at the termination resistor, across the inputs of the last receiver in the load. As expected, the rise and fall times of the signal are much faster with this 18-receiver load bank than with the 36-receiver load bank. To analyze this apparent signal decay more closely, the short 7,62 cm (3") jumpers are reinstalled across the 35-receiver loads and a 500- Ω series resistor is added in series with the bank on a short cable from the driver. The 100- Ω termination resistor is removed to effectively measure the time constant of the signal decay.

The HFS-9003 is adjusted for a 1 V_{p-p} 1-kHz pulse and applied to the driver input. The decay time of the signal is measured across the receiver inputs of the last load; this decay time divided by the 500- Ω resistance results in a total value of 640 pF for the entire bank. This breaks down to just over 18 pF (640/35) for each EVM and jumper, and it increases to 20 pF with the long 15,24 cm (6") jumpers installed.

Increased capacitance causes slower rise and fall times, therefore the time that edges are within a receiver threshold window increases. With this effect, jitter at the input of a receiver is presented for a longer period of time, then the receiver itself increases this jitter again as a near-linear function of signaling rate (approximately 1 ps of jitter per Mbps).

6.2 Receiver Number vs Signaling Rate

Guidelines for determining the maximum allowable signaling rate that can be used with a particular number of receivers can now be established. It has already been determined that one load (EVM and jumper) adds approximately 1 ns of propagation delay and 20 pF of capacitance. Therefore, a plot of propagation delay (# of loads) versus the signaling rate that results in an output jitter of 15% becomes a practical design tool. More propagation delay measurements are needed to complete this graph.

The next series of measurements made on a 13-receiver load (#24 through #36) with 15,24 cm (6") jumpers, yields a propagation delay of 12.3 ns. Based on the previous results, signaling rates approximately twice the fundamental period, result in jitter levels near 15%, signaling rates of 162 Mbps ($2 \times 1/12.3$ ns) and 142.5 Mbps ($1.75 \times 1/21.3$ ns) for the quarter wavelength shift are used with results plotted in Figure 31.

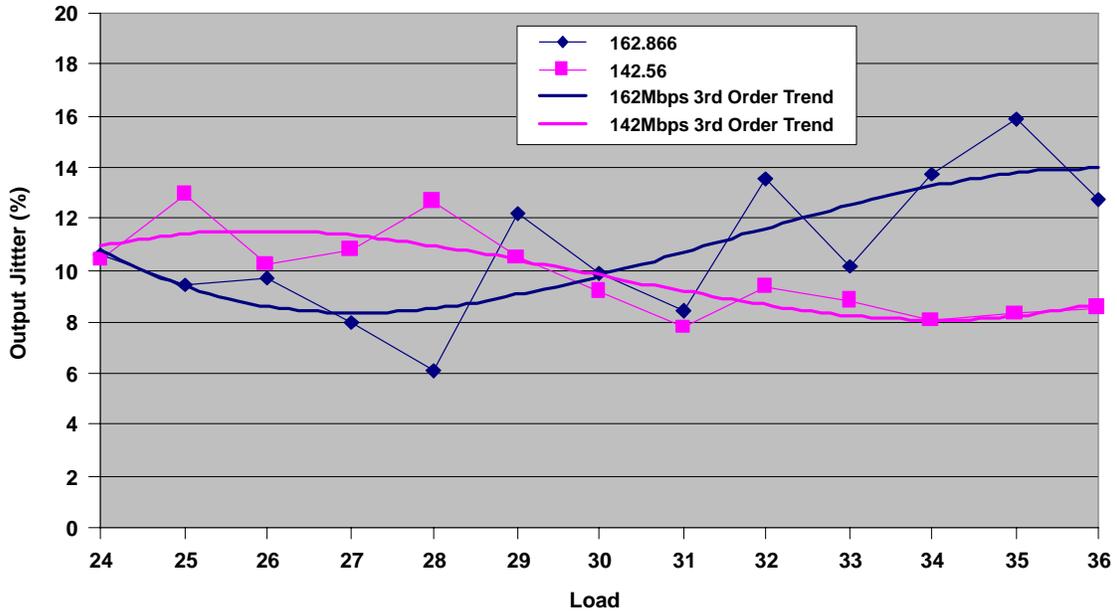


Figure 31. Output Jitter From a 13-Receiver 12.3 ns Load

The 2x signaling rate yields a peak jitter of 16%. The load bank is increased to 15 receivers and a 14.3 ns load delay is measured. Signaling rates of 140 Mbps ($2 \times 1/14.3$ ns), 157 Mbps ($2.24 \times 1/14.3$ ns), and 175 Mbps ($2.5 \times 1/14.3$ ns) are used for this test. The resulting 2.25x quarter-wave shifted rate of 157 Mbps nearly reaching the 15% jitter mark is shown in Figure 32.

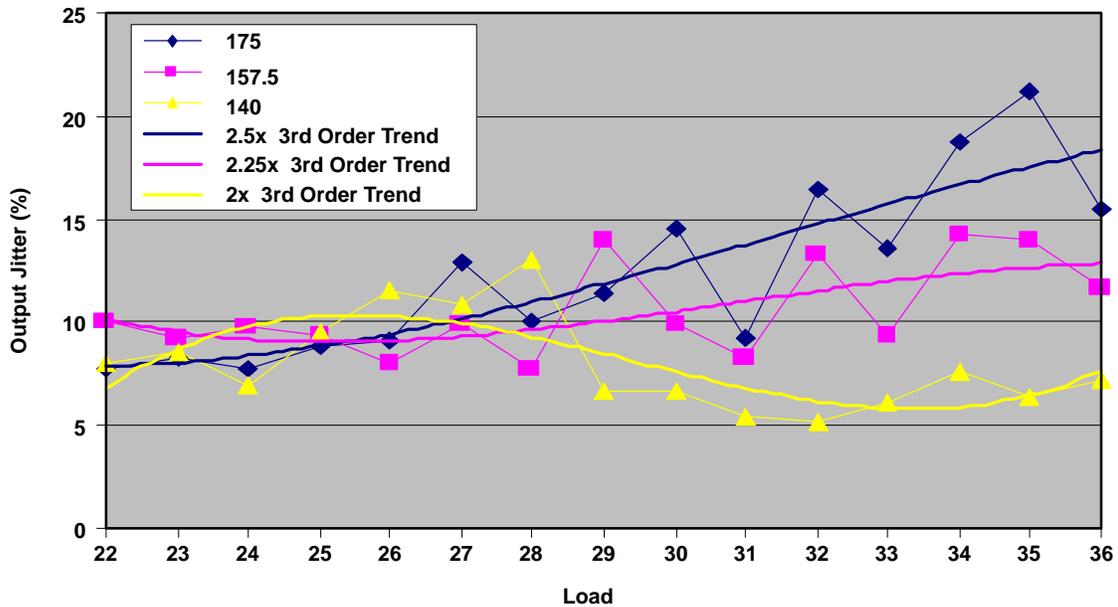


Figure 32. Output Jitter From a 15-Receiver 14.3 ns Load

Remove four jumpers from the load bank to create an 11-drop, 10.4 ns load. When the value of the 2x ($2 \times 1/10.4$ ns = 192 Mbps) was recorded, the results were already above 15% jitter. Tests were then made with 1.75x (168 Mbps) and 1.5x (149Mbps) signaling rates. The results are shown in Figure 33.

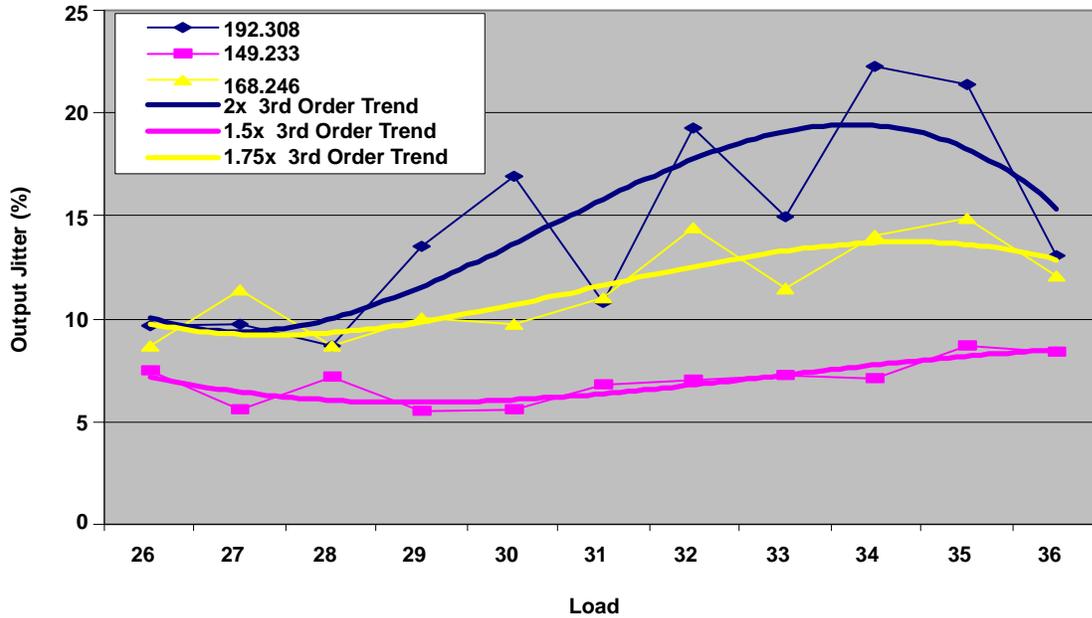


Figure 33. Output Jitter From an 11-Receiver 10.4 ns Load

Tests are repeated with loads of 30, 11, 6, and 3 receivers, and the measurements are combined with earlier results for the plot in Figure 32. The graph confirms expectations of a linear relationship between propagation delay and a 15% jitter signaling rate. (This graph could be titled *Load Capacitance vs Signaling Rate.*)

The data in Figure 34 may be useful in multidrop system development, if the same constraints utilized in the test setup are maintained. Stub lengths are 4 cm or less and the single drop capacitance is approximately 20 pF if the 15,24 cm (6") cable length between loads is used. The transmission cable from the driver to the receiver bank is 1 m, however, this can be relaxed up to 10 m since there is very little performance difference in cables from 1 m to 10 m length (Figures 18 through 22).

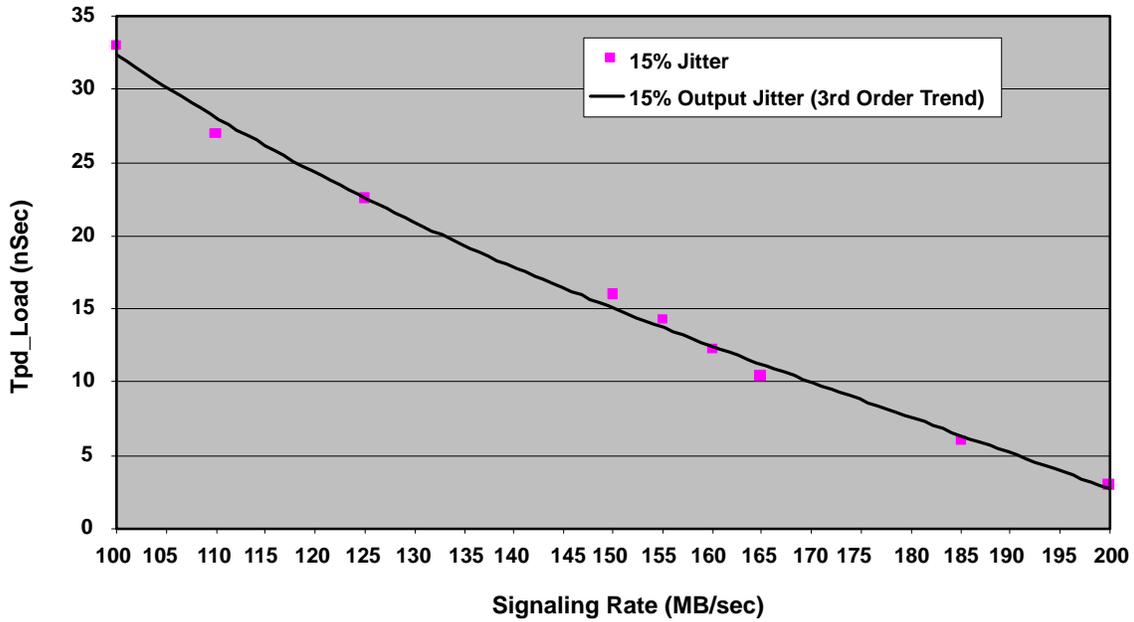


Figure 34. Load Propagation Delay vs Signaling Rate

6.3 Receiver Number vs Common-Mode Voltage Range

Earlier this report mentions that the common-mode output current (I_{oc}) of an LVDS receiver is not specified in the LVDS standard, and that as a result the ground potential difference voltage, (V_{gpd}) may be affected as receivers are added to the output of a single driver. Testing for this condition, a third power supply (Tekronix Model PS280) is added to the test setup for monitoring any change in V_{gpd} . The positive lead of the power supply is connected to the ground of the LVDS31 line driver's V_{CC} supply, and the negative lead is connected to the ground of the load bank's V_{CC} supply. With all jumpers removed from the load bank, the cable from the driver is then attached to load #36, a single receiver. The signaling rate on the HFS-9003 is set to 100 Mbps, and the output of the receiver is monitored while this common-mode voltage is gradually increased.

The test is repeated with the addition of each load until all 36 receivers are connected to the single driver, then the polarity connections on the PS280 power supply are reversed and the tests repeated.

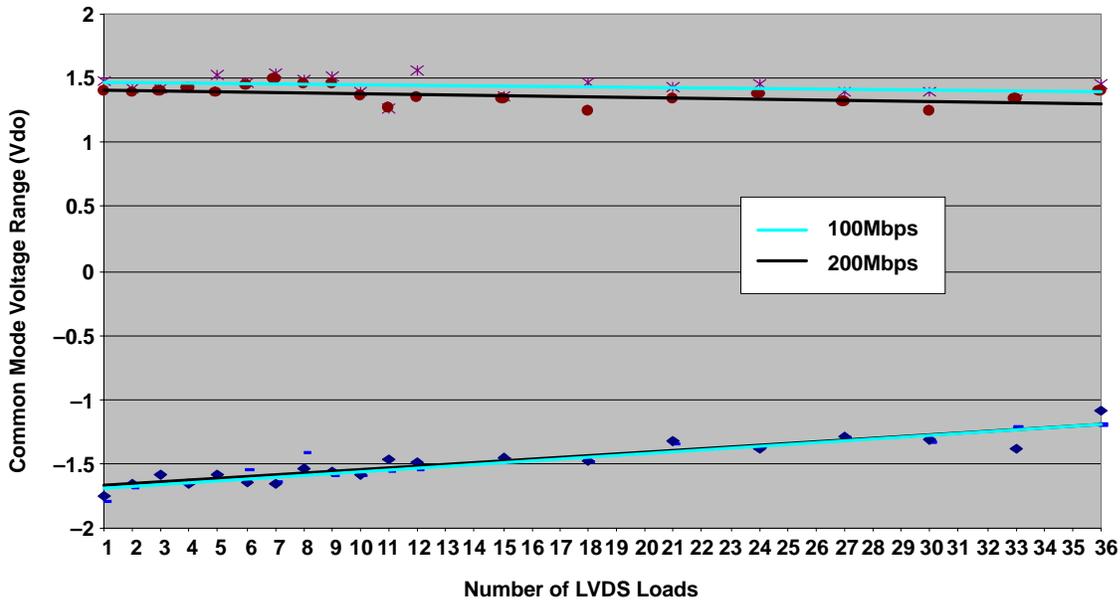


Figure 35. Receiver Number vs Common-Mode Voltage Range

The results presented in Figure 35 confirm that common-mode voltage is impacted by signaling rate. This is due to the gain rolloff of the receiver, and is documented and reported in several point-to-point applications. Also evident in Figure 35 is the increased common-mode loading of the receivers linearly loading the 1.2-V common-mode voltage source of the driver, as predicted earlier in the common-mode model discussion.

Clearly the common-mode voltage range decreases as additional receivers are added to the output of a single LVDS driver, and as the signaling rate increases.

7 References

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3. Design note, *Low Voltage Differential Signaling (LVDS) Design Notes* (Literature Number SLLA014)
4. Application report, *Printed Circuit Board Layout for Improved Electromagnetic Compatibility* (Literature Number SDZAE06)
5. Application report, *What a Designer Should Know* (Literature Number SDZAE03)
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8. Seminar manual, *Linear Design Seminar* (Literature Number SLYDE05)
9. Paper, *Communicate*, Issue June 1998
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11. *Commercial Building Telecommunications Cabling Standard (ANSI/TIA/EIA–568–A)*
12. IEEE 1596.3–1995, *Draft Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interfaces (SCI) Draft 1.3*

Appendix A Glossary

Signaling Rate: $1/T$, where T is the time allocated for one data bit. Therefore, in a transmission system with a 400 Mbps signaling rate, the width of one data bit is 2.5 ns. LVDS, as standardized in TIA/EIA-644, specifies a maximum signaling rate of 655 Mbps, where one bit has a duration of 1.5267 ns. In practice, a maximum signaling rate is determined by the quality of interconnection between line drivers and receivers, since transmission line length and line characteristics ultimately determine the maximum unusable signaling rate. However, the TIA/EIA-644 standard deals with the electrical characteristics of data interchange only, therefore mechanical specifications, bus structure, protocol, and timing are left to the referencing standard.

Data Rate: The number of data bits per second transmitted from driver to receiver. There are nondata bits, such as start bits, stop bits, parity bits, etc., used by many systems, but they are not, strictly speaking, actual data bits. If a transmission system is unformatted, and only data bits are transmitted, then the data rate is equal to the signaling rate.

Jitter: The time frame during which the logic state transition of a signal occurs. The jitter may be given either as an absolute number or as a percentage with reference to the time unit interval (UI). This UI or *bit length* equals the reciprocal value of the signaling rate, and the time during which a logic state is valid is just the UI minus the jitter. Percent jitter (the jitter time divided by the UI times 100) is more commonly used and represents the portion of UI during which a logic state should be considered indeterminate.

Eye-Pattern: A useful tool for measuring overall signal quality at the end of a transmission line. It includes all of the effects of systemic and random distortion, and displays the time during which the signal may be considered valid. A typical eye-pattern is illustrated in Figure 12 with its significant attributes identified.

Several characteristics of an eye-pattern indicate the signal quality of a transmission circuit. The height or *opening* of the eye above or below the receiver threshold level at the sampling instant is the noise margin of the system. The spread of the transitions across the receiver thresholds measures the peak-to-peak jitter of the data signal. The signal rise and fall times can be measured relative to the 0% and 100% levels provided by the series of low and high levels.

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