# TPL0102 Evaluation Module

Features

- TPL0102: 2-channel, 256-Tap, Linear Taper DPOT with Non-Volatile Memory and I2C Interface.
- Simple Evaluation Module (EVM) for user configuration and evaluation.
- Dual Footprint Option (Board Pre-Populated with TPL0102-100RUCR MicroQFN Package)
- Interface to Host Via Connector J14
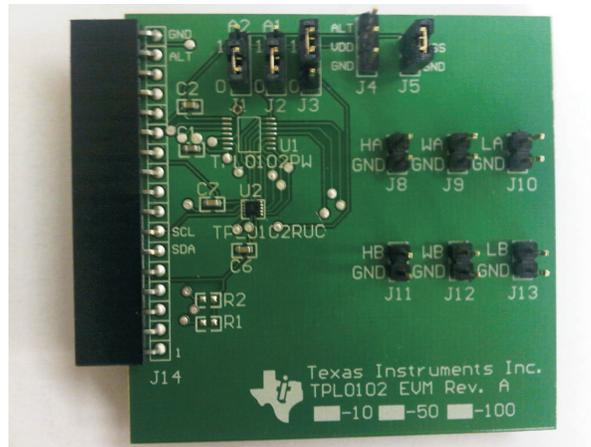
General Description

This EVM is designed to evaluate the operation and performance of the TPL0102, which is a two channel, linear-taper digital potentiometer with 256 wiper positions. Each potentiometer can be used as a three-terminal potentiometer or as a two-terminal rheostat.

Description of Connectors and Jumpers

| Label	Description
J1, J2, J3	A2, A1, A0 inputs. Insert header cap in upper position to set to '1' or in lower position to set to '0'
J4	VDD and GND Terminal.
J5	VSS Terminal. Insert header cap to connect VSS to GND.
J8	HA Terminal
J9	WA Terminal
J10	LA Terminal
J11	HB Terminal
J12	WB Terminal
J13	LB Terminal
J14	Connector to interface with I²C Host

Setup Procedure

1. Insert header caps in J1, J2, J3 to set A2, A1, A0 respectively. The board is shipped with the following settings: A2=0, A1=0, A0=1.
2. Connect the I²C bus of the host processor to the board via connector J14 (pins marked SCL, SDA). Also connect the GND pin on J14 to GND of the host processor.
3. Apply the positive supply voltage (VDD) to center pin of J4. Apply GND to lowest pin of J4.
4. Apply the negative supply voltage (VSS) to J5. The board is shipped with a header cap that connects VSS to GND.
5. Write to the TPL0102 data registers per protocol in the datasheet (Lit# SLIS134).
6. Measure resistance between H, W, L terminals as appropriate on headers J8-J13.

TPL0102 EVM Schematic

TPL0102 Evaluation Module
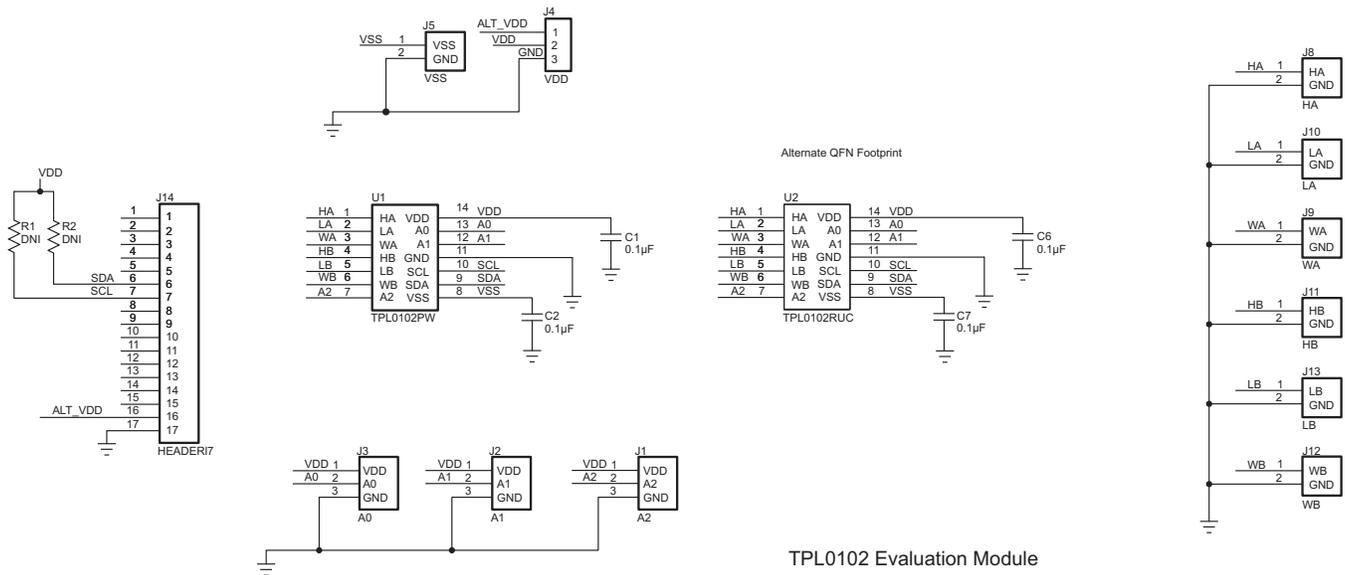
TPL0102 EVM Component Placement
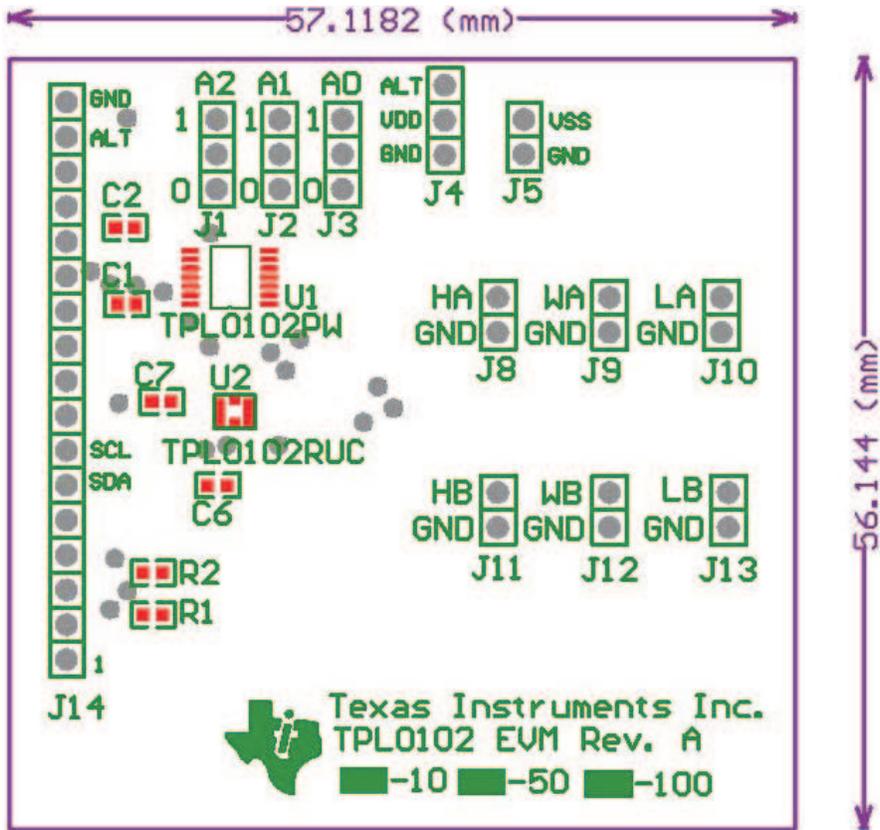
TPL0102 EVM Layout (Top Layer)
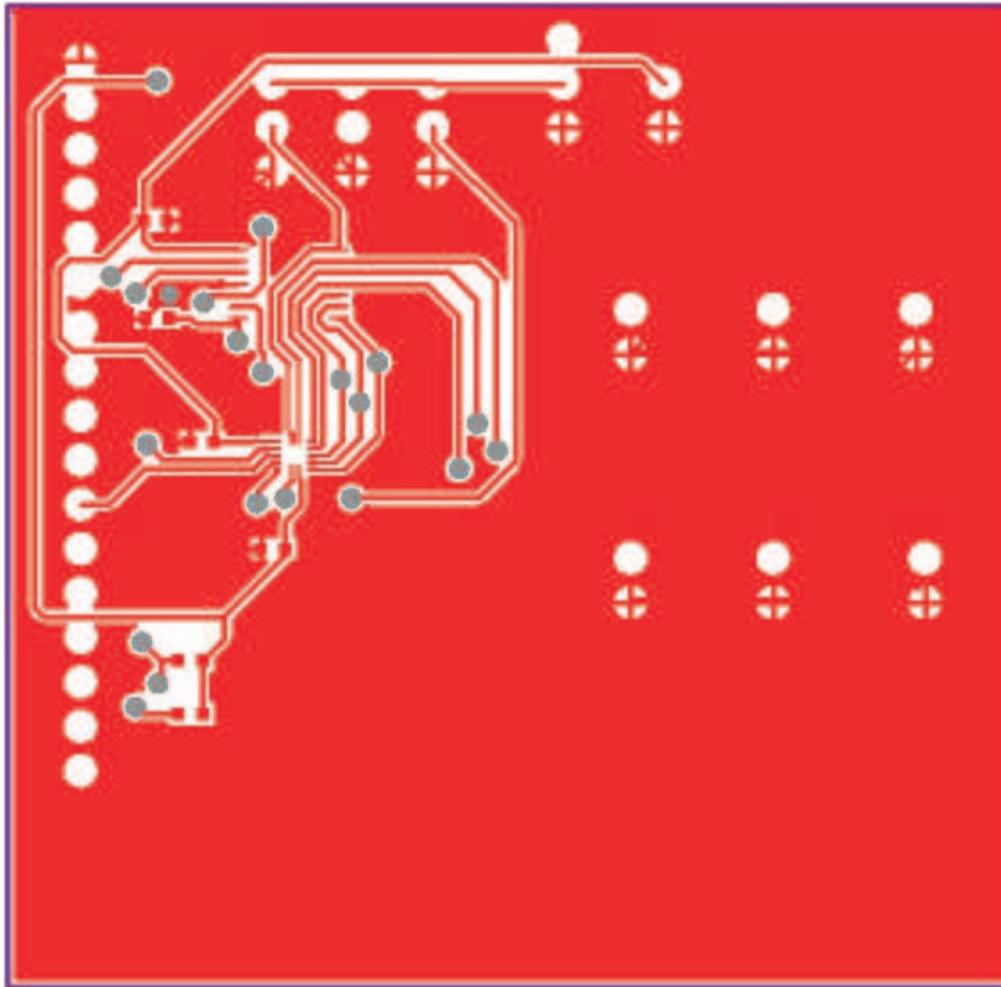
TPL0102 EVM Layout (Bottom Layer)

IMPORTANT NOTICE