Application Report
SLIA094A–January 2020–Revised March 2020

DRV5013-Q1 Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for DRV5013-Q1 (SOT-23 (3), TO-92 (3) package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 shows the device functional block diagram for reference.

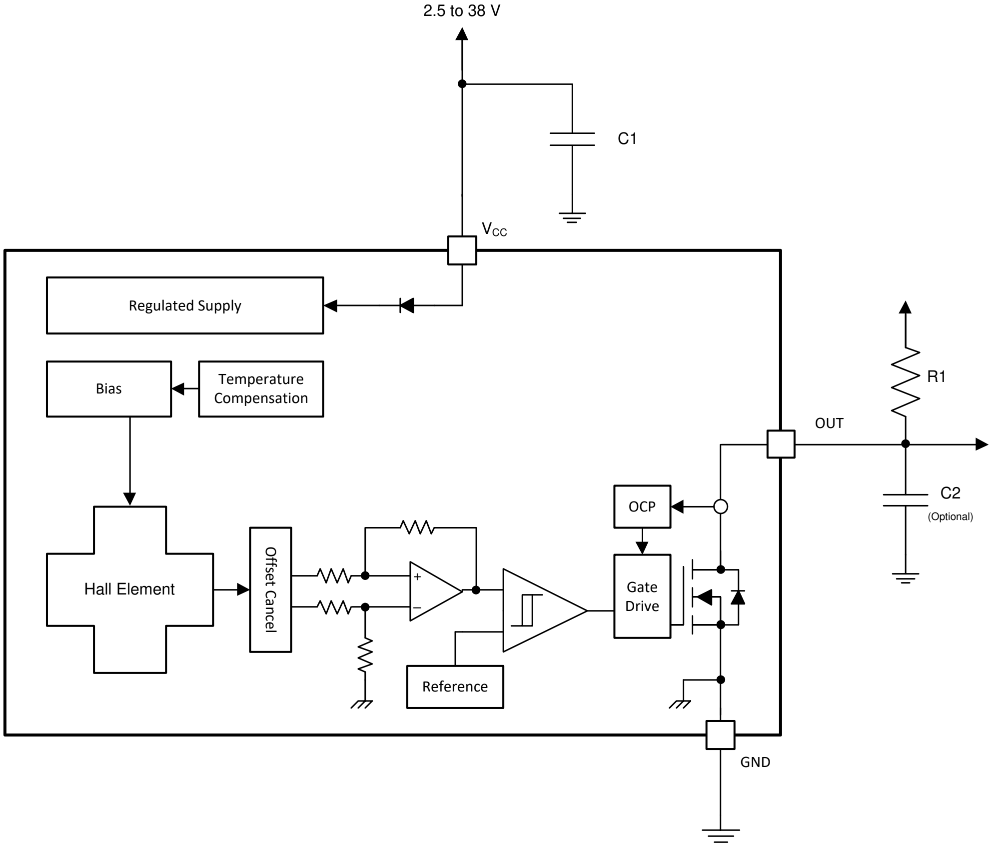

Figure 1. Functional Block Diagram

DRV5013-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for DRV5013-Q1 based on two different industry-wide used reliability standards:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 3 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1. SOT23-3, Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	6
Die FIT Rate	4
Package FIT Rate	2

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 50 mW
- Climate type: World-wide Table 8
- Package factor lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. TO-92, Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	19
Die FIT Rate	3
Package FIT Rate	16

The failure rate and mission profile information in Table 2 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 50 mW
- Climate type: World-wide Table 8
- TO-92 Package factor lambda B Table 18
- Thermal mismatch Pi alpha = 1.0
- EOS FIT rate assumed: 0 FIT

Table 3. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 3 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for DRV5013-Q1 in Table 4 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 4. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output operation out of specification	40%
No Output	50%
Pin to Pin short any two pin	10%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the . The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 6)
- Pin open-circuited (see Table 8)
- Pin short-circuited to an adjacent pin (see Table 10)

Table 6 through Table 13 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 5.

Table 5. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 2 and Figure 3 show the pin diagrams. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the datasheet.

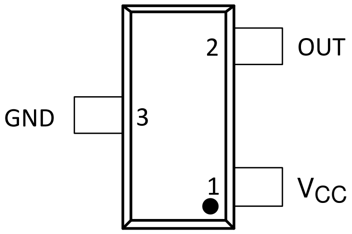

Figure 2. SOT-23 Pin Diagram

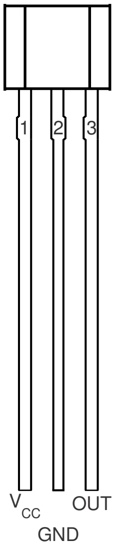

Figure 3. TO-92 Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Device is powered within published absolute maximum operating conditions.

Table 6. SOT23, Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCC	1	Supply shorted to Ground. System will source high current as a result. Thermal damage may result.	B
OUT	2	DRV5013-Q1 will not be damaged. Output will be pulled down by short to GND.	C
GND	3	Normal mode of operation	D

Table 7. TO-92, Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCC	1	Supply shorted to Ground. System will source high current as a result. Thermal damage may result.	B
OUT	3	DRV5013-Q1 will not be damaged. Output will be pulled down by short to GND.	C
GND	2	Normal mode of operation	D

Table 8. SOT23, Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCC	1	The DRV5013-Q1 won't be damaged. There will be no power supply current, and no functionality.	B
OUT	2	The DRV5013-Q1 won't be damaged. Power supply current will be the normal but the output is not connected to any load	C
GND	3	The DRV5013-Q1 won't be damaged. There will be no power supply current, and no functionality.	B

Table 9. TO-92, Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCC	1	The DRV5013-Q1 won't be damaged. There will be no power supply current, and no functionality.	B
OUT	3	The DRV5013-Q1 won't be damaged. Power supply current will be the normal but the output is not connected to any load	C
GND	2	The DRV5013-Q1 won't be damaged. There will be no power supply current, and no functionality.	B

Table 10. SOT23, Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VCC	1	OUT	The DRV5013-Q1 will not be damaged. The output will sink about 30mA (limited by the overcurrent protection feature). The output signal will be stuck-high and non-functional. Note that the MCU in the system might then see VCC on its input which may be an overvoltage.	B

Table 11. TO-92, Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VCC	1	GND	The DRV5013-Q1 will not be damaged. The system power supply will source high current due to this short and may current limit. Thermal damage may be a concern.	B
GND	2	OUT	The DRV5013-Q1 will not be damaged. The output will be stuck low and non-functional.	B

Table 12. SOT23, Pin FMA for Device Pins Short-Circuited to VCC

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCC	1	Normal mode of operation	D
OUT	2	The DRV5013-Q1 will not be damaged. The output will sink about 30mA (limited by the overcurrent protection feature). The output signal will be stuck-high and non-functional. Note that the MCU in the system might then see VCC on its input which may be an overvoltage.	B
GND	3	Supply shorted to Ground. System will source high current as a result and may current limit. Thermal damage may result.	B

Table 13. TO-92, Pin FMA for Device Pins Short-Circuited to VCC

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCC	1	Normal mode of operation	D
OUT	3	The DRV5013-Q1 will not be damaged. The output will sink about 30mA (limited by the overcurrent protection feature). The output signal will be stuck-high and non-functional. Note that the MCU in the system might then see VCC on its input which may be an overvoltage.	B
GND	2	Supply shorted to Ground. System will source high current as a result and may current limit. Thermal damage may result.	B

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2020) to A Revision	**Page**
• Changed to latest report format, including FIT Rate, FMD, and Pin FMA	1

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