Texas Instruments

DEM-DAI1808

User's Guide

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DEM-DAI1808

User's Guide

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Description

The DEM-DAI1808 is an evaluation board for the PCM1808, a 96-kHz, 24-bit PCM audio analog-to-digital converter (ADC), with digital audio transmitter, optical and coaxial interface, onboard multiple clock generator, –6-dB amplifier with LPF, and switches or jumpers for mode or clock control.

Related documentation includes the DIT4096 96-kHz Digital Audio Transmitter data sheet (literature number SBOS225) and the PLL1707, PLL1708 3.3-V Dual PLL Multiclock Generator data sheet (literature number SLES065)

The DEM-DAI1808 operates under 5-V and ±15-V analog power supplies, with 1-Vrms or 2-Vrms unbalanced analog signal input.

Topic **Page**

1.1 Block Diagram

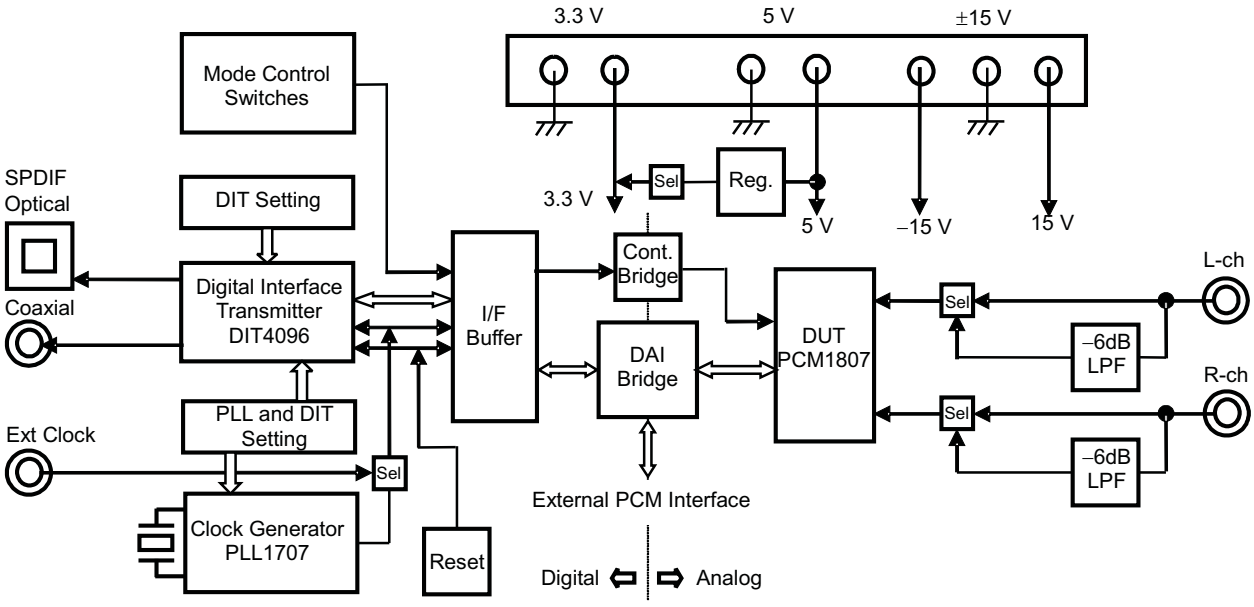


Figure 1-1. DEM-DAI1808 Block Diagram

1.2 Basic Connection and Operation

1.2.1 Basic Connections and Configurations

- Connect the 5-V and ±15-V power supplies to V_{CC}, $\pm AV_{CC}$, and GND on CN051–CN055. The ±15-V power supplies only are required for 2-Vrms input.
- Connect the SPDIF output to CN003 (coaxial) or U001 (optical).
- Select the system clock source from 256/512 fs or 384 fs generated by on-board clock generator (PLL1707), or external clock input connector (CN001) using JP001, and ensure the presence of system clock on it.
- Set the interface mode (master or slave) using SW002 M/S for board and SW004 MD1/0 for PCM1808.
- Set the interface format (LJ-24 or I^2S-24) using SW002 FMT0 for board and SW004 FMT for PCM1808.
- Select the combination of sampling frequency (16 kHz to 96 kHz) and system clock rate (256 fs, 384 fs, 512 fs), using SW002 CLK1/0, SR, FS2/1 for board and SW004 for PCM1808.
- Set the channel status for DIT4096 if required. (It is not required for PCM1808 evaluation.)

1.2.2 Configuration Controls

1.2.2.1 System Clock Source Selection

The system clock (master clock) source for the evaluation module (EVM) including the PCM1808, which is associated with sampling frequency, can be selectable by the JP001 setting as follows.

Table 1-1. System Clock Source Selection

JP001	DESCRIPTION
256	Internal, 256/512 times of sampling frequency (default)
384	Internal, 384 times of sampling frequency
EXT	External, TTL interface level, up to 25 MHz

1.2.2.2 Master/Slave (M/S) Interface Mode Selection

The audio interface mode of the PCM1808 and EVM can be selectable as follows.

In slave mode, audio interface clock, BCK, and LRCK are generated in the DIT4096 and supplied to the PCM1808 through a buffer. In master mode, they are generated in the PCM1808 and supplied to the DIT4096.

Mode control to the PCM1808 can be performed by the SW004 setting.

Table 1-2. Master/Slave Interface Mode Selection

SW002, M/S(1)	SW004, MD1/0(1)		DESCRIPTION
	MD1	MD0	
OFF (High)	ON (Low)	ON (Low)	Slave mode
ON (Low)	ON (Low)	OFF (High)	Master mode, 512 fs (default)
ON (Low)	OFF (High)	ON (Low)	Master mode, 384 fs
ON (Low)	OFF (High)	OFF (High)	Master mode, 256 fs

(1) Other inconsistent combinations between SW002 M/S and SW004 MD1/0 selection are not available.

1.2.2.3 Interface Format Selection

The audio interface format of the PCM1808 and EVM can be changed as follows.

Table 1-3. Interface Format Selection

SW002, FMT0[1]	SW004, FMT[1]	DESCRIPTION
OFF (High)	ON (Low)	I^2S 24 bits (default)
ON (Low)	OFF (High)	Left-justified 24 bits

(1) Other inconsistent combinations between SW002 FMT0 and SW004 FMT selection are not available.

1.2.2.4 Sampling Frequency and System Clock Frequency Selection

The sampling frequency and the system clock frequency for the PCM1808 and EVM can be selectable as shown in Table 1-4 and Table 1-5 by setting JP001, SW002, and SW004. Sampling frequencies of 16 kHz to 96 kHz and system clock rates of 256 fs, 384 fs, and 512 fs are available for the EVM. The settings of JP001, CLK1/0 of SW002, and MD1/0 of SW004 (see Table 1-4) determine the system clock rate. The settings of SR and FS2/1 of SW002 (see Table 1-5) determine the sampling clock and system clock frequencies. The possible combinations of sampling clock and system clock frequencies appear in the right-most column of Table 1-5.

Table 1-4. System Clock Rate Selection

JP001[1]	SW002[2]		SW004[3]		SYSTEM CLOCK RATE
	CLK1	CLK0	MD1	MD0	
–	ON/Low	ON/Low	–	–	Reserved
256	ON/Low	OFF/High	OFF/High	OFF/High	256 fs
384	OFF/High	ON/Low	OFF/High	ON/Low	384 fs
256	OFF/High	OFF/High	ON/Low	OFF/High	512 fs (default)

(1) Other inconsistent combinations between SW002 CLK1/0 and SW004 MD1/0 selection are not available.
(2) Select the DIT4096 master clock rate.
(3) Select the PCM1808 system clock rate if master-mode operation of the PCM1808 is required. If slave-mode operation of the PCM1808 is required, the combination of MD1 = ON/Low and MD0 = ON/Low is available for all three rates: 256 fs, 384 fs, and 512 fs.

Table 1-5. Sampling Frequency and System Clock Frequency Selection

SW002[1]			FREQUENCIES SAMPLING CLOCK (kHz)/SYSTEM CLOCK (MHz)
SR	FS2	FS1	
256-fs Operation			
OFF/Low	ON/High	OFF/Low	32/8.192
OFF/Low	OFF/Low	ON/High	44.1/11.2896
OFF/Low	OFF/Low	OFF/Low	48/12.288
ON/High	ON/High	OFF/Low	64/16.384
ON/High	OFF/Low	ON/High	88.2/22.5792
ON/High	OFF/Low	OFF/Low	96/24.576
384-fs Operation			
OFF/Low	ON/High	OFF/Low	32/12.288
OFF/Low	OFF/Low	ON/High	44.1/16.9344
OFF/Low	OFF/Low	OFF/Low	48/18.432
ON/High	ON/High	OFF/Low	64/24.576
ON/High	OFF/Low	ON/High	88.2/33.8688[2]
ON/High	OFF/Low	OFF/Low	96/36.864[2]
512-fs Operation			
OFF/Low	ON/High	OFF/Low	16/8.192[3]
OFF/Low	OFF/Low	ON/High	22.05/11.2896
OFF/Low	OFF/Low	OFF/Low	24/12.288
ON/High	ON/High	OFF/Low	32/16.384
ON/High	OFF/Low	ON/High	44.1/22.5792
ON/High	OFF/Low	OFF/Low	48/24.576 (default)

(1) Select the clock output frequency of the PLL1707 SCKOx; the combination of FS2 = ON/High and FS1 = ON/High is reserved.
(2) Not applicable through the SPDIF interface due to a limitation of the DIT4096. Frequencies are applicable for PCM direct interface between the PCM1808 and externals.
(3) May not be applicable through the SPDIF interface due to interface receiver limitations of digital-domain measurement equipment, like Audio Precision. This frequency is applicable for PCM direct interface between the PCM1808 and externals.

1.2.2.5 Analog Input Level/Path Selection

The DEM-DAI1808 supports 1-Vrms and 2-Vrms input for full scale of analog input signal by the JP101, JP102 setting. For 2-Vrms input selection, an onboard 100-kHz LPF and –6-dB attenuator is applied on the input signal. The default setting is 2-Vrms input.

Table 1-6. Analog Input Level/Path Selection

JP101, JP102	DESCRIPTION
1 Vrms	1-Vrms full-scale analog input is fed to ADC directly.
2 Vrms	2-Vrms full-scale analog input is fed to ADC through 100 kHz LPF and –6-dB attenuator (default).

1.2.2.6 Reset Control

The DEM-DAI1808 supports Reset Control for DIT4096 by SW003.

1.2.2.7 S/PDIF Transmitter Format (Channel Status) Setting for DIT4096

The extended configurations of the digital audio interface transmitter, DIT4096, and the channel status of SPDIF can be set using the DIP switches, SW001. The individual switch settings and their functions are described in Table 1-7. For general evaluation or test of function and performance of the PCM1808, the change from default setting of this SW001 is not needed. This is provided for evaluation of the DIT4096 function, mainly related to channel status information.

Table 1-7. S/PDIF Transmitter Format (Channel Status) Setting for DIT4096

SW001	ON/OFF	DESCRIPTION
CSS	Off (High)	Channel status data bits are set in serial fashion at the COPY/C input with clock input at the SYNC input.
	On (Low)	COPY/C, L, /AUDIO, and /EMPH inputs are used to set associated channel status data bits (default).
COPY/C(1)	Off (High)	Copy and generation status information with L input for CSS = Low, channel status data bit = 1 for CSS = High
	On (Low)	Copy and generation status information with L input for CSS = Low, channel status data bit = 0 for CSS = High (default)
U	Off (High)	User data input = 1
	On (Low)	User data input = 0 (default)
V	Off (High)	Validity data input = 1
	On (Low)	Validity data input = 0 (default)
L(1)	Off (High)	Copy and generation status with COPY/C for CSS = Low
	On (Low)	Copy and generation status with COPY/C for CSS = Low (default)
/AUDIO	Off (High)	Audio data valid control input, not linear PCM
	On (Low)	Audio data valid control input, linear PCM (default)
/EMPH	Off (High)	Pre-emphasis status input, not applied pre-emphasis (default)
	On (Low)	Pre-emphasis status input, applied pre-emphasis
BLSM	Off (High)	BLS mode control input, BLS is an output (default)
	On (Low)	BLS mode control input, BLS is an input
BLS	Off (High)	Block start input for BLSM = Low, output for BLSM = High (default)
	On (Low)	Not block start

(1) Copy and generation status information for CSS = Low

COPY/C	L	COPY AND GENERATION STATUS
On (Low)	On (Low)	Consumer mode, PRO = 0, COPY = 0, L = 0 (default)
On (Low)	Off (High)	Consumer mode, PRO = 0, COPY = 0, L = 1
Off (High)	On (Low)	Consumer mode, PRO = 0, COPY = 1, L = 0
Off (High)	Off (High)	Professional mode, PRO = 1, No copy protection

1.2.2.8 Audio Interface Mode and Format Control for PCM1808

The audio interface mode and format control for the PCM1808 can be performed by the SW004 setting. The summary of the PCM1808 pin configuration is given in Table 1-8.

Table 1-8. Mode and Format Control for PCM1808

MD1 (#11)	MD0 (#10)	DESCRIPTION
Low	Low	Slave mode
Low	High	Master mode 512 fs (default)
High	Low	Master mode 384 fs
High	High	Master mode 256 fs

FMT (#12)	DESCRIPTION
Low	I^2S 24 bits (default)
High	Left-justified 24 bits

1.2.2.9 DAI Bridge and Control Bridge Selection

The DEM-DAI1808 supports flexible PCM audio interface through a DAI bridge, so that the PCM1808 can interface with external devices or equipment in place of an internal buffer and the DIT4096. Interfacing with externals can be done by changing JP052 and JP053 connections for SCLK, BCK, LRCK, DATA, and GND as shown in Figure 1-2.

The DEM-DAI1808 also supports flexible mode and format control to the PCM1808 by redirection of the control port through the header setting of the control bridge, JP054. The default setting is interfaced with internal DIT4096 and DIP switch, SW004.

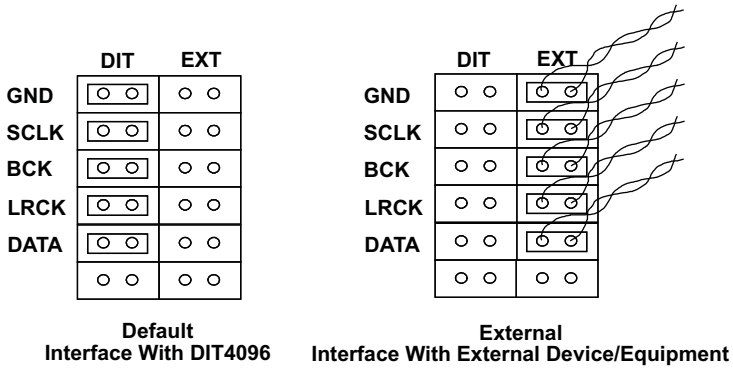
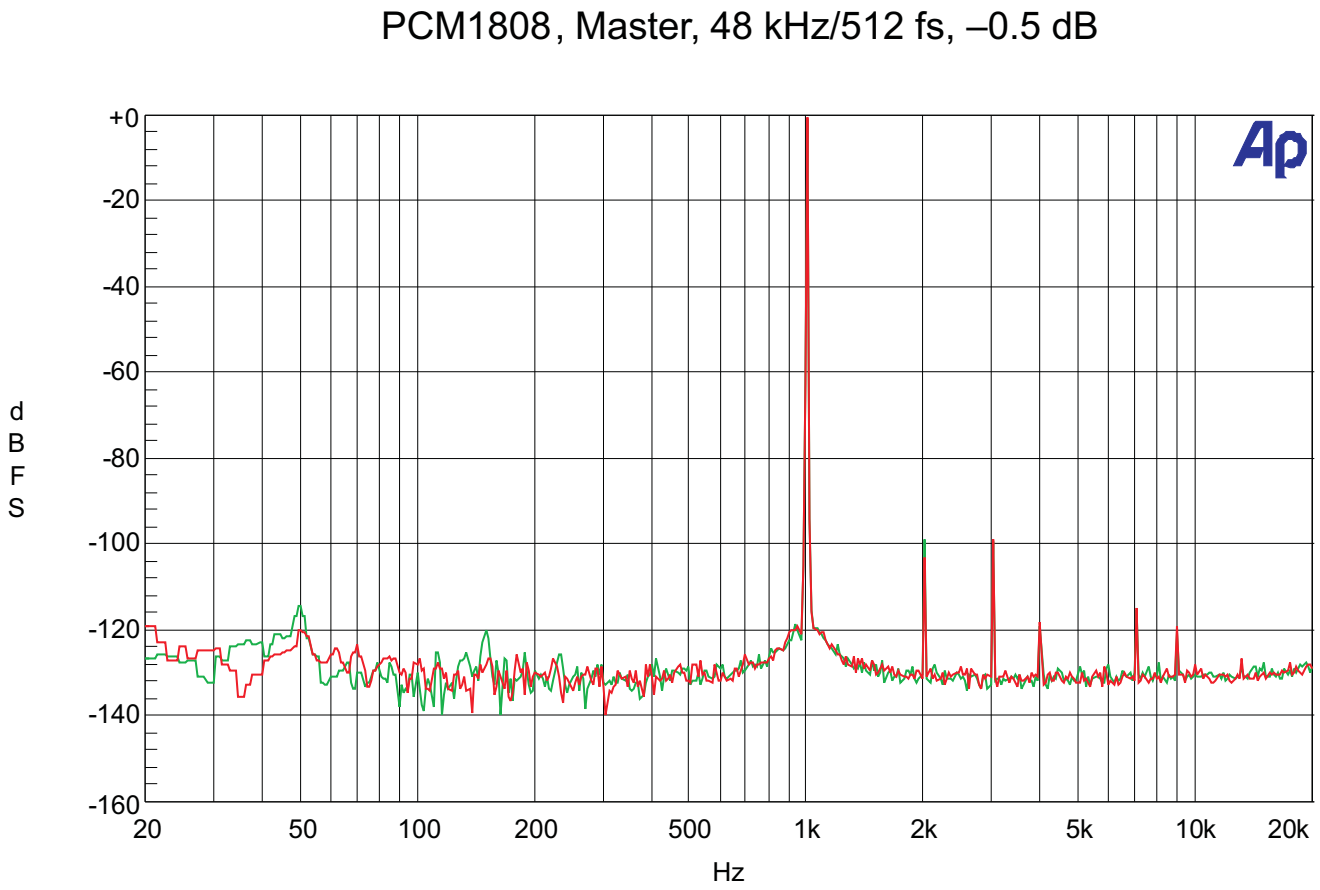


Figure 1-2. External Interfaces

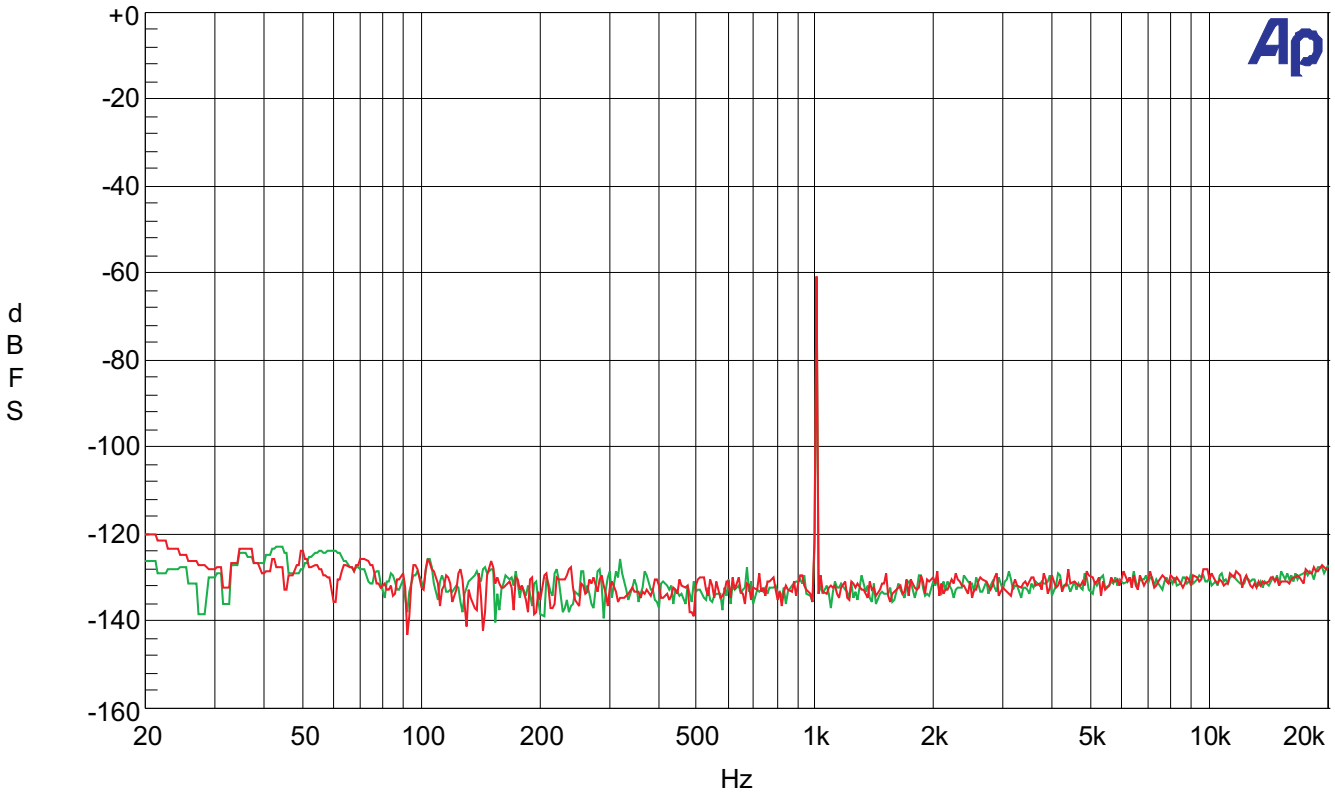
1.3 Typical Performance and Measurement Example

Typical performance of the DEM-DAI1808 for default condition is as follows, and FFT results for full-scale input and –60-dB input are shown.

THD+N @ 48 kHz/512 fs:	–93.5 dB
D. Range @ 48 kHz/512 fs:	99.3 dB
SNR @ 48 kHz/512 fs:	99.3 dB



PCM1808, Master, 48 kHz/512 fs, –60 dB



Schematics and Printed Circuit Boards

This chapter presents the DEM-DAI1808 schematics, Bill of Materials (BOM), and printed circuit boards.

Topic **Page**

2.1 DEM-DAI1808 Schematics

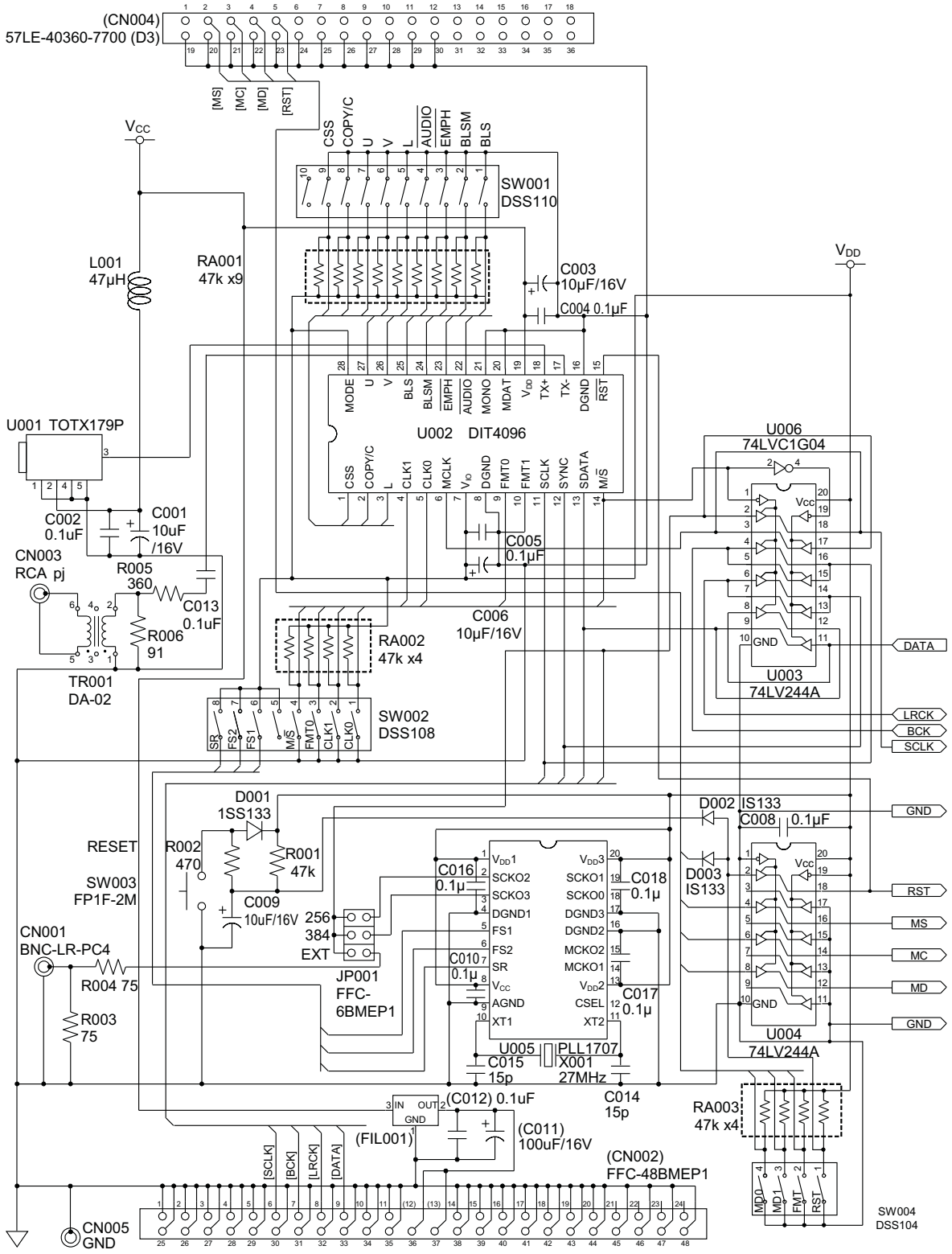


Figure 2-1. DEM-DAI1808 Digital Section (Digital Audio Interface)

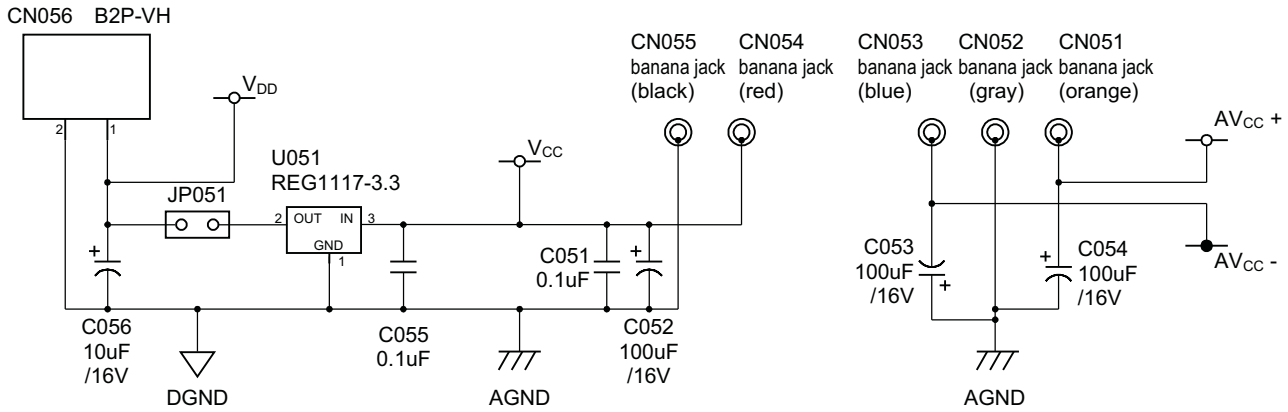


Figure 2-2. DEM-DAI1808 Regulator and Connector

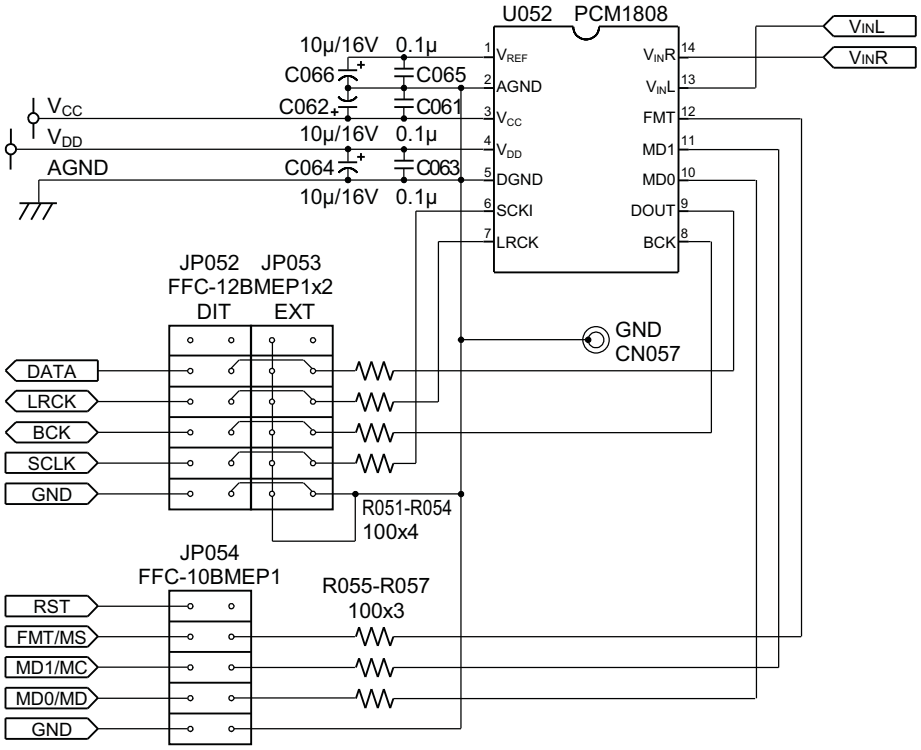


Figure 2-3. DEM-DAI1808 ADC Section

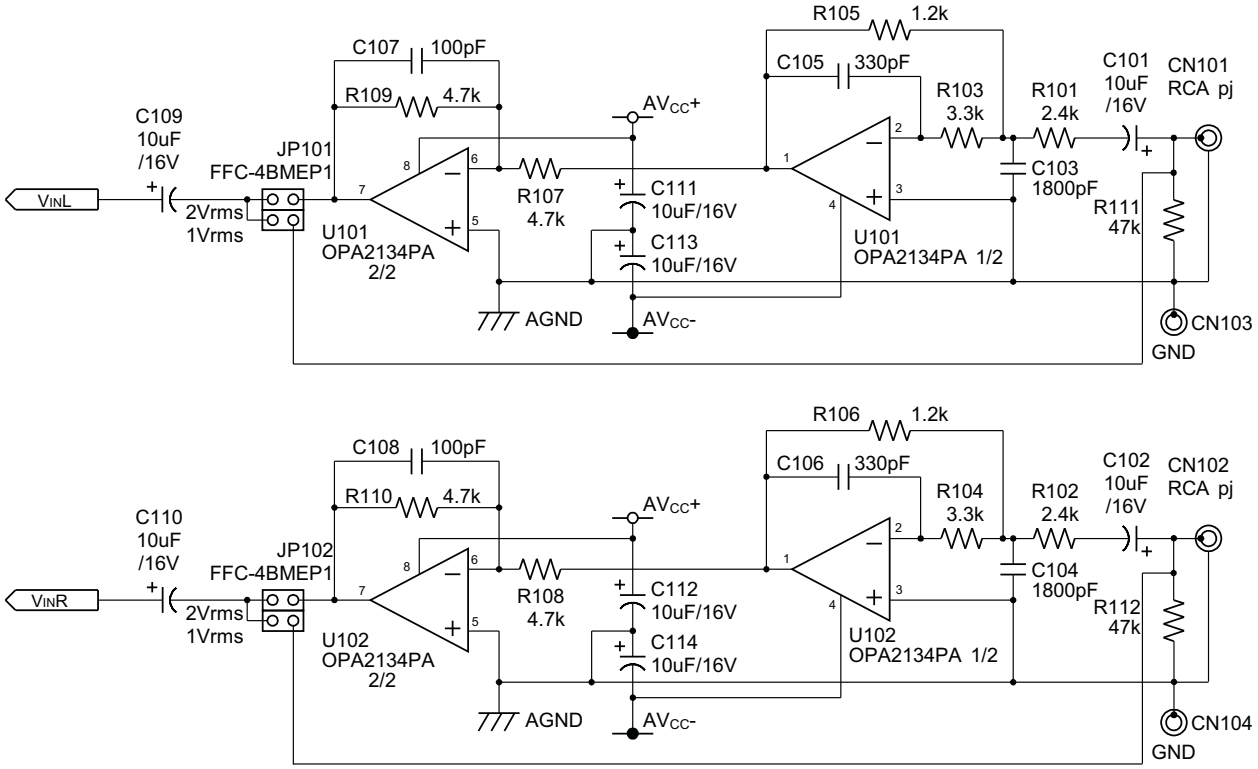


Figure 2-4. DEM-DAI1808 Analog Section

2.2 DEM-DAI1808 Bill of Materials (BOM)

REF. NO.	PART NAME	SPEC-1	SPEC-2	PART NO.	SUPPLIER	REMARKS
Parts List 1/4 (Digital Portion)						
C001	Electrolytic Capacitor	10 uF/16 V		R3A-16V100M	ELNA	
C002	Ceramic Capacitor	0.1 uF/25 V		PRE132F104Z50	Murata	
C003	Electrolytic Capacitor	10 uF/16 V		R3A-16V100M	ELNA	
C004	Ceramic Capacitor	0.1 uF/25 V		PRE132F104Z50	Murata	
C005	Electrolytic Capacitor	10 uF/16 V		R3A-16V100M	ELNA	
C006	Ceramic Capacitor	0.1 uF/25 V		PRE132F104Z50	Murata	
C007	Ceramic Capacitor	0.1 uF/25 V		PRE132F104Z50	Murata	
C008	Ceramic Capacitor	0.1 uF/25 V		PRE132F104Z50	Murata	
C009	Electrolytic Capacitor	10 uF/16 V		R3A-16V100M	ELNA	
C010	Ceramic Capacitor	0.1 uF/25 V		PRE132F104Z50	Murata	
C011	Electrolytic Capacitor	100 uF/16 V		ROA-16V101M	ELNA	Unmounted
C012	Ceramic Capacitor	0.1 uF/25 V		PRE132F104Z50	Murata	Unmounted
C013	Ceramic Capacitor	0.1 uF/25 V		PRE132F104Z50	Murata	
C014	Ceramic Capacitor	15 pF/50 V		PRE131CH150J50	Murata	
C015	Ceramic Capacitor	15 pF/50 V		PRE131CH150J50	Murata	
C016	Ceramic Capacitor	0.1 uF/25 V		PRE132F104Z50	Murata	
C017	Ceramic Capacitor	0.1 uF/25 V		PRE132F104Z50	Murata	
C018	Ceramic Capacitor	0.1 uF/25 V		PRE132F104Z50	Murata	
R001	Metal Film Resistor	1/8 W, 47 k	J			
R002	Metal Film Resistor	1/8 W, 470	J			
R003	Metal Film Resistor	1/8 W, 75	J			
R004	Metal Film Resistor	1/8 W, 75	J			
R005	Metal Film Resistor	1/8 W, 360	J			
R006	Metal Film Resistor	1/8 W, 91	J			
RA001	Resistor Array	47k × 9	J			
RA002	Resistor Array	47k × 4	J			
RA003	Resistor Array	47k × 4	J			
L001	Micro Inductor	47 uH	J	EL0606SKI-470J	TDK	
FIL001	Filter					Unmounted
D001	Diode			1S133	ROHM	
D002	Diode			1S133	ROHM	
D003	Diode			1S133	ROHM	
U001	Optical Transmitter			TOTX-179P	Toshiba	
U002	SPDIF Transmitter			DIT4096PW	TI	
U003	Buffer			SN74LV244A	TI	
U004	Buffer			SN74LV244A	TI	
U005	PLL Clock Generator			PLL1707DB	TI	
U006	One Gate Device	Inverter		SN74LVC1G04DBV	TI	
TR001	Pulse Transformer			DA-02	JPC	
X001	Crystal Resonator	27 MHz	±50 ppm	HC-49/U-S, 27 MHz	Kinseki	
SW001	DIP Switch			DSS110	Fujisoku	DIT
SW002	DIP Switch			DSS108	Fujisoku	DIT & PLL

REF. NO.	PART NAME	SPEC-1	SPEC-2	PART NO.	SUPPLIER	REMARKS
SW003	Push Switch			FP1F-2M	Fujisoku	Reset DIT
SW004	DIP Switch			DSS104	Fujisoku	Mode DUT
JP001	6-Pin Connector			FFC-6BMEP1	Honda	256/384/Ext
CN001	BNC Connector			BNC-LR-PC4		Right Angle
CN002	48-Pin Connector			FFC-48BMEP1	Honda	Unmounted
CN003	RCA Connector	Yellow		LPR6520-0804	SMK	
CN004	Connector			57LE-40360-7700	DDK	Unmounted
CN005	Test Terminal			LC-2-G	Mac8	GND
	Short Plug	×1		DIC-130	Honda	JP001
Parts List 2/4 (Power Portion)						
C051	Ceramic Capacitor	0.1 uF/25 V		PRE132F104Z50	Murata	
C052	Electrolytic Capacitor	100 uF/16 V		ROA-16V101M	ELNA	
C053	Electrolytic Capacitor	100 uF/16 V		ROA-16V101M	ELNA	
C054	Electrolytic Capacitor	100 uF/16 V		ROA-16V101M	ELNA	
C055	Ceramic Capacitor	0.1 uF/25 V		PRE132F104Z50	Murata	
C056	Electrolytic Capacitor	10 uF/16 V		R3A-16V100M	ELNA	
U051	3.3-V Regulator			REG1117-3.3	TI	
JP051	2-Pin Connector			FFC-2AMEP1	Honda	
CN051	Banana Jack	Orange				
CN052	Banana Jack	Gray				
CN053	Banana Jack	Blue				
CN054	Banana Jack	Red				
CN055	Banana Jack	Black				
CN056	VH Connector			B2P-VH	Nihon-Accyaku-Tanshi	
	Short Plug	×1		DIC-130	Honda	JP051
Parts List 3/4 (DUT Portion)						
C061	Ceramic Capacitor	0.1 uF/25 V	1608 type	GRM39F104Z25PT	Murata	Chip type
C062	Electrolytic Capacitor	10 uF/16 V		R3A-16V100M	ELNA	
C063	Ceramic Capacitor	0.1 uF/25 V	1608 type	GRM39F104Z25PT	Murata	Chip type
C064	Electrolytic Capacitor	10 uF/16 V		R3A-16V100M	ELNA	
C065	Ceramic Capacitor	0.1 uF/25 V	1608 type	GRM39F104Z25PT	Murata	Chip type
C066	Electrolytic Capacitor	10 uF/16 V		R3A-16V100M	ELNA	
R051	Metal Film Resistor	1/8 W, 100	J			Chip type
R052	Metal Film Resistor	1/8 W, 100	J			Chip type
R053	Metal Film Resistor	1/8 W, 100	J			Chip type
R054	Metal Film Resistor	1/8 W, 100	J			Chip type
R055	Metal Film Resistor	1/8 W, 100	J			Chip type
R056	Metal Film Resistor	1/8 W, 100	J			Chip type
R057	Metal Film Resistor	1/8 W, 100	J			Chip type
U052	A/D Converter (DUT)			PCM1808DB	TI	
JP052	12-Pin Connector			FFC-12BMEP1	Honda	
JP053	12-Pin Connector			FFC-12BMEP1	Honda	
JP054	10-Pin Connector			FFC-10BMEP1	Honda	

REF. NO.	PART NAME	SPEC-1	SPEC-2	PART NO.	SUPPLIER	REMARKS
CN057	Test Terminal			LC-2-G	Mac8	GND
	Short Plug	×10		DIC-130	Honda	JP052, 3, 4
Parts List 4/4 (Analog Portion)						
C101	Electrolytic Capacitor	10 uF/16 V		ROA-16V100M	ELNA	
C102	Electrolytic Capacitor	10 uF/16 V		ROA-16V100M	ELNA	
C103	Film Capacitor	1800 pF	J	APSF0100J182	Nissei	
C104	Film Capacitor	1800 pF	J	APSF0100J182	Nissei	
C105	Film Capacitor	330 pF	J	APSF0100J331	Nissei	
C106	Film Capacitor	330 pF	J	APSF0100J331	Nissei	
C107	Film Capacitor	100 pF	J	APSF0100J101	Nissei	
C108	Film Capacitor	100 pF	J	APSF0100J101	Nissei	
C109	Electrolytic Capacitor	10 uF/16 V		ROA-16V100M	ELNA	
C110	Electrolytic Capacitor	10 uF/16 V		ROA-16V100M	ELNA	
C111	Electrolytic Capacitor	10 uF/16 V		R3A-16V100M	ELNA	
C112	Electrolytic Capacitor	10 uF/16 V		R3A-16V100M	ELNA	
C113	Electrolytic Capacitor	10 uF/16 V		R3A-16V100M	ELNA	
C114	Electrolytic Capacitor	10 uF/16 V		R3A-16V100M	ELNA	
R101	Metal Film Resistor	1/8 W, 2.4 k	F			
R102	Metal Film Resistor	1/8 W, 2.4 k	F			
R103	Metal Film Resistor	1/8 W, 3.3 k	F			
R104	Metal Film Resistor	1/8 W, 3.3 k	F			
R105	Metal Film Resistor	1/8 W, 1.2 k	F			
R106	Metal Film Resistor	1/8 W, 1.2 k	F			
R107	Metal Film Resistor	1/8 W, 4.7 k	F			
R108	Metal Film Resistor	1/8 W, 4.7 k	F			
R109	Metal Film Resistor	1/8 W, 4.7 k	F			
R110	Metal Film Resistor	1/8 W, 4.7 k	F			
R111	Metal Film Resistor	1/8 W, 47 k	F			
R112	Metal Film Resistor	1/8 W, 47 k	F			
U101	Dual Op Amp	DIP		OPA2134PA	TI	
U102	Dual Op Amp	DIP		OPA2134PA	TI	
JP101	4-Pin Connector			FFC-4BMEP1	Honda	
JP102	4-Pin Connector			FFC-4BMEP1	Honda	
CN101	RCA Connector	White		LPR6520-0803	SMK	
CN102	RCA Connector	Red		LPR6520-0802	SMK	
CN103	Test Terminal			LC-2-G	Mac8	GND
CN104	Test Terminal			LC-2-G	Mac8	GND
	IC Socket	DIP 8 pin				U101
	IC Socket	DIP 8 pin				U102
	Short Plug	×2		DIC-130	Honda	JP101, 102

2.3 DEM-DAI1808 Printed Circuit Boards

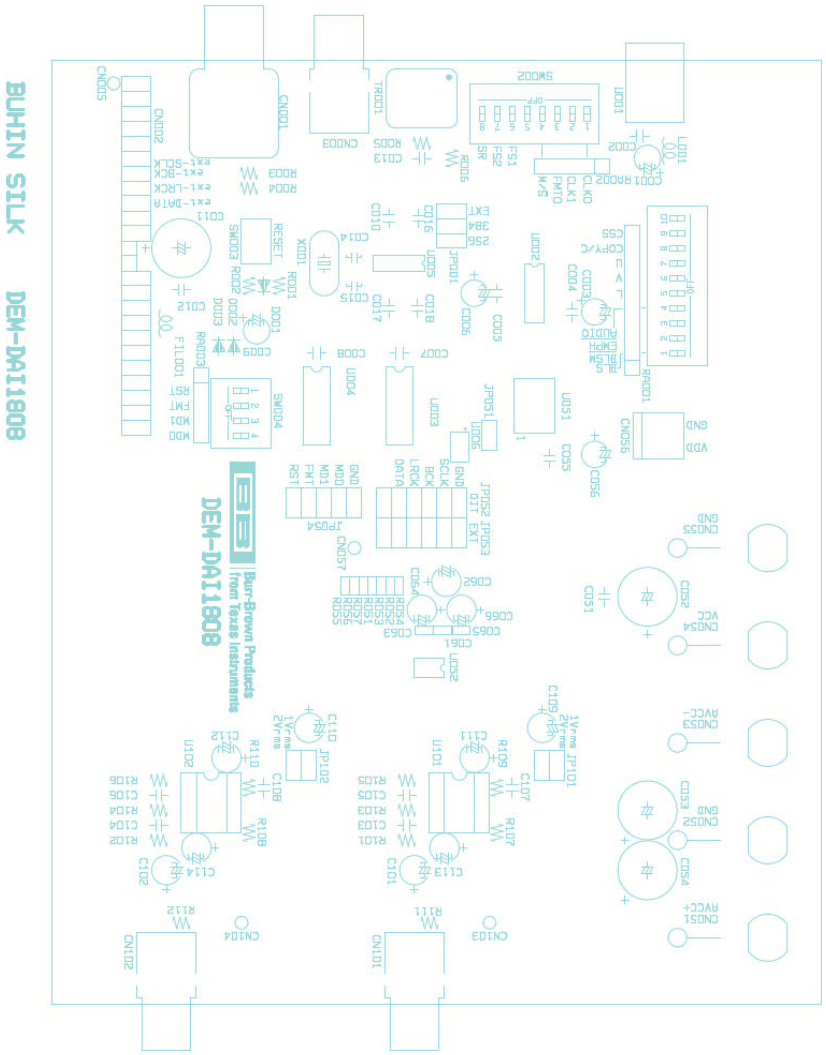


Figure 2-5. DEM-DAI1808 Silkscreen

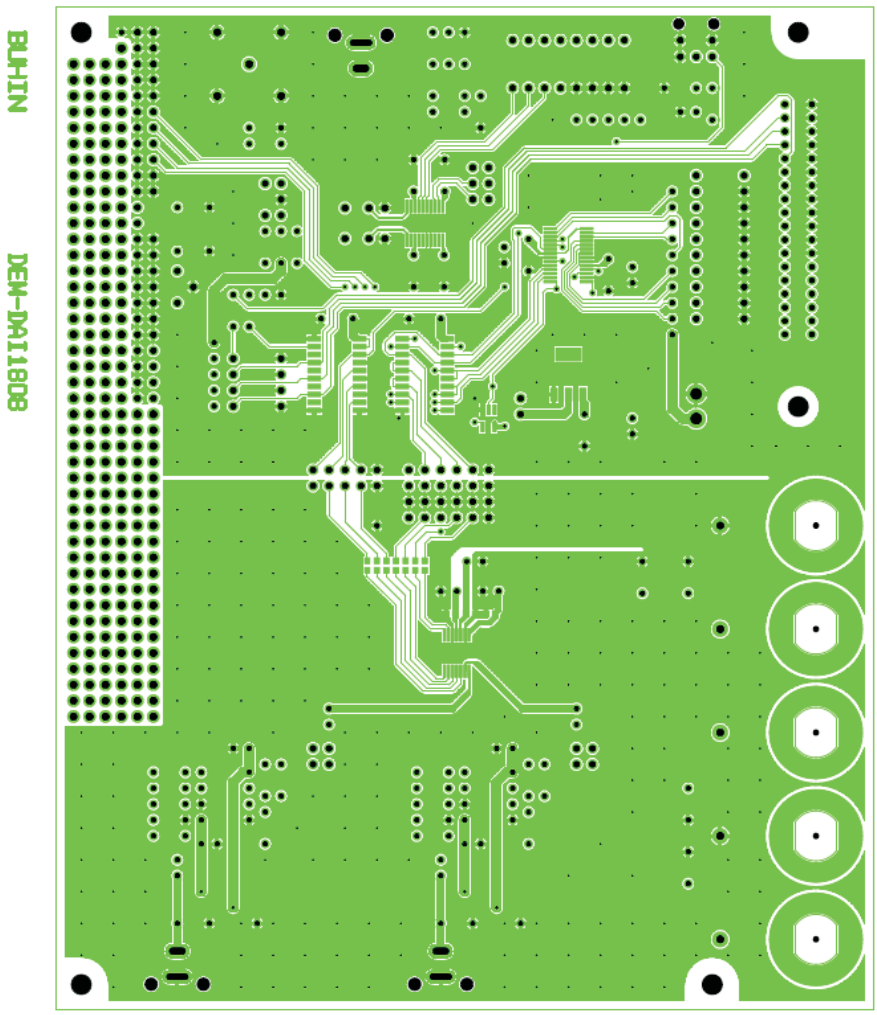


Figure 2-6. DEM-DAI1808 — Top View

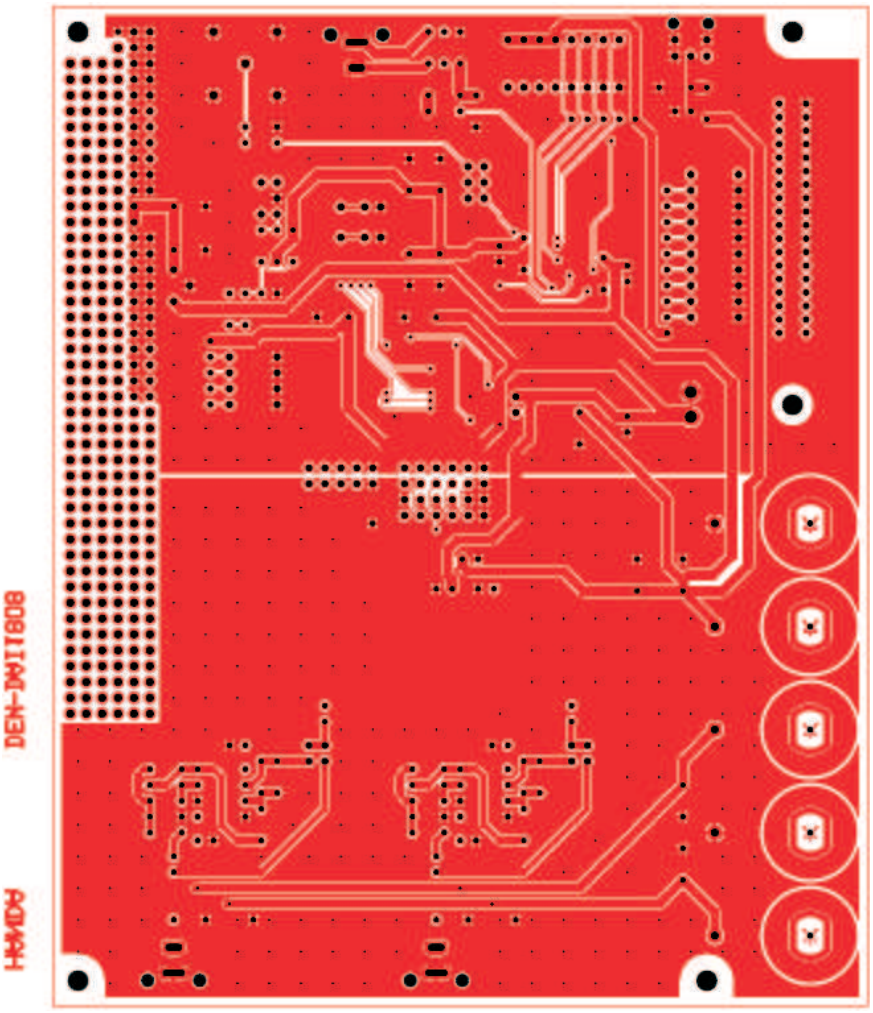


Figure 2-7. DEM-DAI1808 — Bottom View

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During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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