Application Note

Using LP8733xx and TPS65218xx PMICs to Power AM64x and AM243x Sitara Processors

ABSTRACT

This application note discusses two variants of the LP8733xx and two variants of the TPS65218xx power management ICs (PMIC) that power the AM64x and AM243x Sitara™ processor lines. The report highlights the benefits of each PMIC solution and includes a selection guide to compare options. Example power maps are provided to assist the design process.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

The AM64x and AM243x Sitara processor lines provide highly flexible, real-time, and low latency processing for a broad range of industrial applications. These processors come in an array of variants with up to two Arm® Cortex® -A53 cores and up to four Arm® Cortex® -R5F cores each. TI has multiple power management IC (PMIC) options to meet the complex power needs of each processor variant.

This application note reviews two variants of the LP8733xx and two variants of the TPS65218xx PMICs that power these Sitara processor lines. A selection guide outlines both a single-PMIC and dual-PMIC solution for the AM64x, and a single-PMIC solution for the AM243x. The application note also highlights the value each PMIC solution brings to the overall system and provides example power maps for each variant.

2 LP8733xx and TPS65218xx Device Overview

The LP8733xx and TPS65218xx are optimized and highly integrated power management solutions for the AM64x and AM243x processors. Table 2-1 provides an overview of the technical features for each PMIC family.

Table 2-1. LP8733xx and TPS65218xx Features

Features	LP8733xx	TPS65218xx
Input range	2.8 V to 5.5 V	2.7 V to 5.5 V (Converters) 1.8 V to 5.5 V (LDO)
Number of regulators	4	7
Number of DC-DC step-down converters	2	3 (Adjustable output voltage) 2 (Backup battery domain)
Number of Buck-boost converters	0	1
Number of LDOs	2	1
Additional Features	• 2 configurable GPO signals for sequencing • Interrupt function with programmable masking • Programmable power-good signal (PGOOD) • Output short-circuit and overload protection • Overtemperature warning and protection • Overvoltage protection	• 3 load switches • 3 general purpose I/Os • 2 backup battery supplies that can be configured to operate as always-on supplies with the addition of a coin cell battery • Customizable voltage thresholds for the UVLO and supervisor • Interrupts for overtemperature, overcurrent, and undervoltage can be monitored for the load switches • Power-fail comparator
Ability to reprogram using EEPROM	No	Yes

The LP8733xx is a one-time programmable (OTP) device that comes pre-programmed to simplify the design process and allows direct implementation of the given power configuration with no modifications needed.

The TPS65218xx is a non-volatile memory (NVM) device that comes both pre-programmed and user-programmable. For example, the TPS652185**5** is pre-programmed to meet the AM64x power sequence and configuration needs when paired with the LP873364. The TPS652181**5** is a user programmable *DIY* device that comes with a blank EEPROM and disabled regulators to provide freedom to customize the desired output voltages, sequencing and more from start up as further explained in Section 6. All devices in the TPS65218xx family have a reprogrammable EEPROM, allowing flexibility to change configuration settings according to system needs.

3 LP8733xx and TPS65218xx PMIC Variants

Table 3-1 shows a comparison of the regulator output settings for each LP8733xx variant. The two LP8733xx variants are OTP devices that are pre-programmed with set output voltages and sequencing to match the different AM64x or AM243x specifications. For more information on this device, please see the LP8733xx data sheet. For more details on each variant, please refer to the LP873364 Technical Reference Manual and the LP87334D Technical Reference Manual.

Table 3-1. LP8733xx variant comparison table

PMIC	LP873364		LP87334D	
Regulator Settings	Output Voltage	Startup / Shutdown Delay	Output Voltage	Startup / Shutdown Delay
Buck0	0.75 V	2 ms / 2 ms	0.85 V	2 ms / 2 ms
Buck1	3.3 V	0 ms / 2 ms	3.3 V	0 ms / 2 ms
LDO0	1.8 V	1 ms / 2 ms	1.8 V	1 ms / 2 ms
LDO1	1.8 V	1 ms / 2 ms	1.8 V	1 ms / 2 ms
GPO0	X[1]	15 ms / 0 ms	X[1]	15 ms / 0 ms
GPO2	X[1]	3 ms / 0 ms	X[1]	3 ms / 0 ms

[1] A set output voltage is not pre-programmed; GPO0 and GPO2 can be pulled up and used to sequence discrete components to the system.

Table 3-2 shows a comparison of the pre-programmed TPS6521855 versus the *DIY* TPS6521815 settings. The TPS6521855 is a pre-programmed NVM device that can be used with the LP873364 as a dual-PMIC solution for the AM64x processors. The TPS6521815 is the user-programmable *DIY* version, and will be discussed in greater detail in Section 6. For more information on each variant, please see the TPS6521855 and TPS6521815 data sheets.

Table 3-2. TPS65218xx Variant Comparison Table

PMIC	TPS6521855			TPS6521815		
Regulator Settings	Output Voltage	Enabled	Startup / Shutdown delay	Output Voltage	Enabled	Startup / Shutdown delay
DCDC1	1.1 V	Yes	10 ms / 8 ms	0.85 V to 1.675 V	No	X[2]
DCDC2	1.0 V	Yes	8 ms / 10 ms			
DCDC3	1.8 V	Yes	8 ms / 10 ms	0.9 V to 3.4 V	No	X[2]
DCDC4	2.5 V	Yes	6 ms / 12 ms	1.175 V to 3.4 V	No	X[2]
DCDC5	1.0 V	No	X[2]	1.0 V	No	X[2]
DCDC6	1.8 V	No	X[2]	1.8 V	No	X[2]
LDO1	3.3 V	Yes	4 ms / 14 ms	0.9 - 3.4 V	No	X[2]

[2] Register is not enabled, so regulator is not controlled by the sequencer. Regulator can be programmed with register enabled and desired startup/shutdown delay.

The AM64x and AM243x PMIC solution options using each LP8733xx and TPS65218xx PMIC variant are outlined in the next section in a PMIC Selection Guide.

4 PMIC Selection Guide

Table 4-1 details a selection guide for powering the AM64x or AM243x. The PMIC solution choice will depend on the desired power configuration, memory support, and peripherals support such as Ethernet PHY. The recommended discrete regulators to implement these supports are also listed. The next section provides example power maps for each PMIC solution, and also highlights additional design considerations such as solution size and cost.

Table 4-1. AM64x and AM243x PMIC Solution Selection Guide

	AM64x Single-PMIC Solution	AM64x Dual-PMIC Solution	AM243x (ALX Package) PMIC Solution		AM243x (ALV Package) PMIC Solution
PMIC	**LP873364**[3]	**LP873364 + TPS6521855**[4]	**LP87334D**[5]		
Memory Support	LPDDR4 or DDR4	LPDDR4 or DDR4	No	No	LPDDR4 or DDR4
Recommended Discrete Regulators	TPS745, TPS62822	TPS745	No	TPS62822 or TPS745 (for 1.1 V or 2.5 V Ethernet PHY support)	TPS62822, TPS745
PMIC Package Size	5 mm x 5 mm	5 mm x 5 mm + 6 mm x 6 mm	5 mm x 5 mm	5 mm x 5 mm	5 mm x 5 mm
Example Power Map	Figure 5-1 (with LPDDR4) Figure 5-2 (with DDR4)	Figure 5-3 (with LPDDR4) Figure 5-4(with DDR4)	Figure 5-5	Figure 5-6	Figure 5-7 (with LPDDR4) Figure 5-8(With DDR4)
Available TI design resources	• Powering the AM64x with the LP8733xx PMIC • LP873364 Technical Reference Manual	• Powering the AM64x with the LP8733xx PMIC: *Can the LP873364 be Used in a Dual PMIC Configuration?* • LP873364 Technical Reference Manual • Ready hardware solution: AM64x SK EVM	LP87334D Technical Reference Manual	LP87334D Technical Reference Manual	LP87334D Technical Reference Manual

[3] LP87334D is a viable alternate power solution if choosing to power VDD_CORE with under 0.85 V.

[4] The *DIY* PMIC TPS6521815 comes with all rails disabled, which is beneficial for allowing placement of the PMIC in the system without damaging the SoC during power up. The TPS6521815 can then be programed to the TPS6521855 register settings.

[5] The *DIY* PMIC TPS6521815 can be used in place of LP87334D to fully customize the power solution, however it may provide more regulators than needed for the processor.

5 Example Power Maps

The following section provides an example power map for the PMIC solutions outlined in Table 4-1, above. Additional details and solution benefits are described for each PMIC solution.

5.1 AM64x Single-PMIC Solution

An example power map using LP873364 for the AM64x with LPDDR4 memory support is shown in Figure 5-1, and with DDR4 memory support in Figure 5-2.

LP873364 has four rails and two configurable GPOs that can be used for sequencing. Therefore, the LP873364 solution consists of 1 PMIC + × discretes (depending on implementation of LPDDR4 or DDR4). This single-PMIC LP873364 solution is cost and size optimized compared to the AM64x dual-PMIC solution. The PCB area using the LP873364 solution with LPDDR4 memory support is about a 42% reduction in size as compared to the current AM64x SK EVM. This solution has also been extensively tested in the lab for power, sequencing, brownout, and fault conditions. Please refer to the Powering the AM64x with the LP8733xx PMIC application brief for in-depth information on implementing this solution.

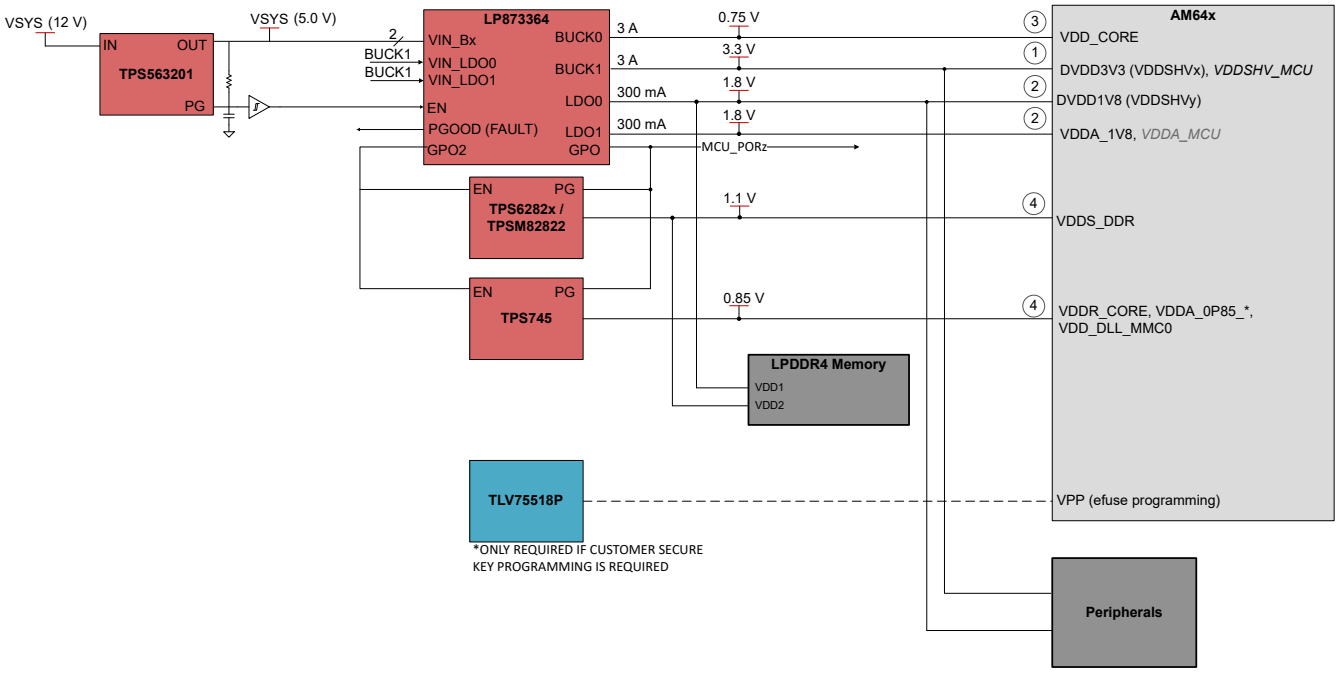


Figure 5-1. Using LP873364 to Power AM64x with LPDDR4 Memory Support

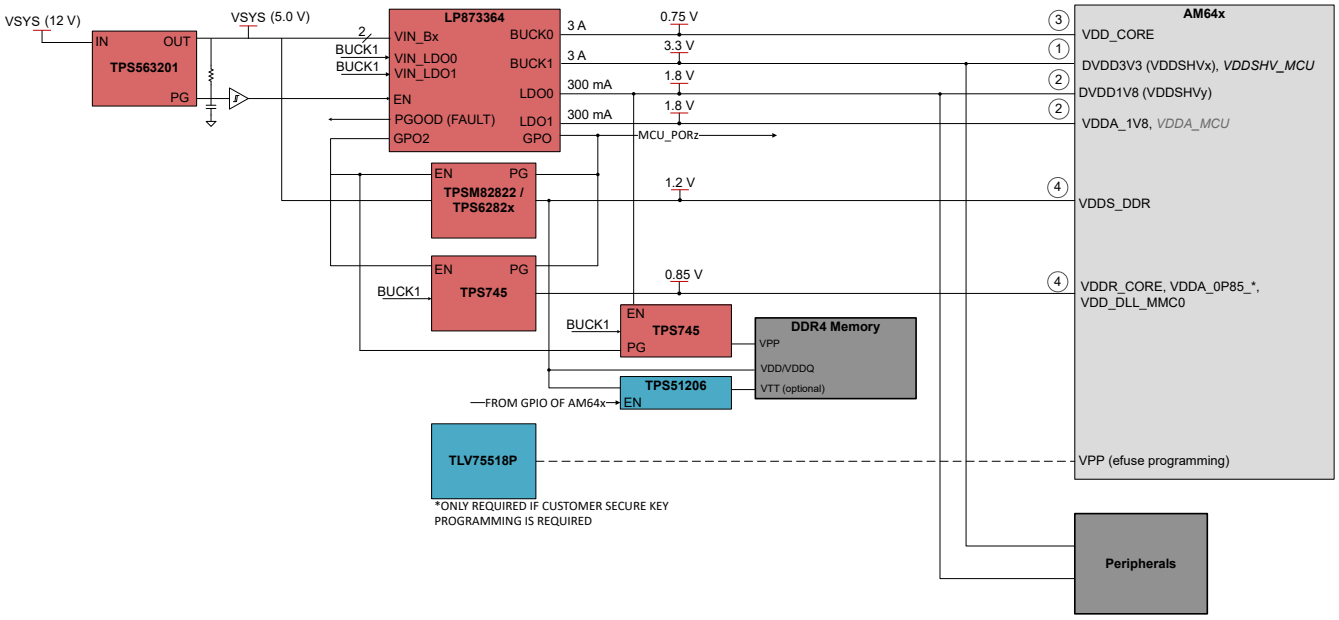


Figure 5-2. Using LP873364 to Power AM64x with DDR4 Memory Support

Figure 5-2 provides an example power map using LP873364 for the AM64x with DDR4 memory support. A second TPS745 discrete LDO is enabled by LP873364 LDO0 to supply the DDR4 VPP rail.

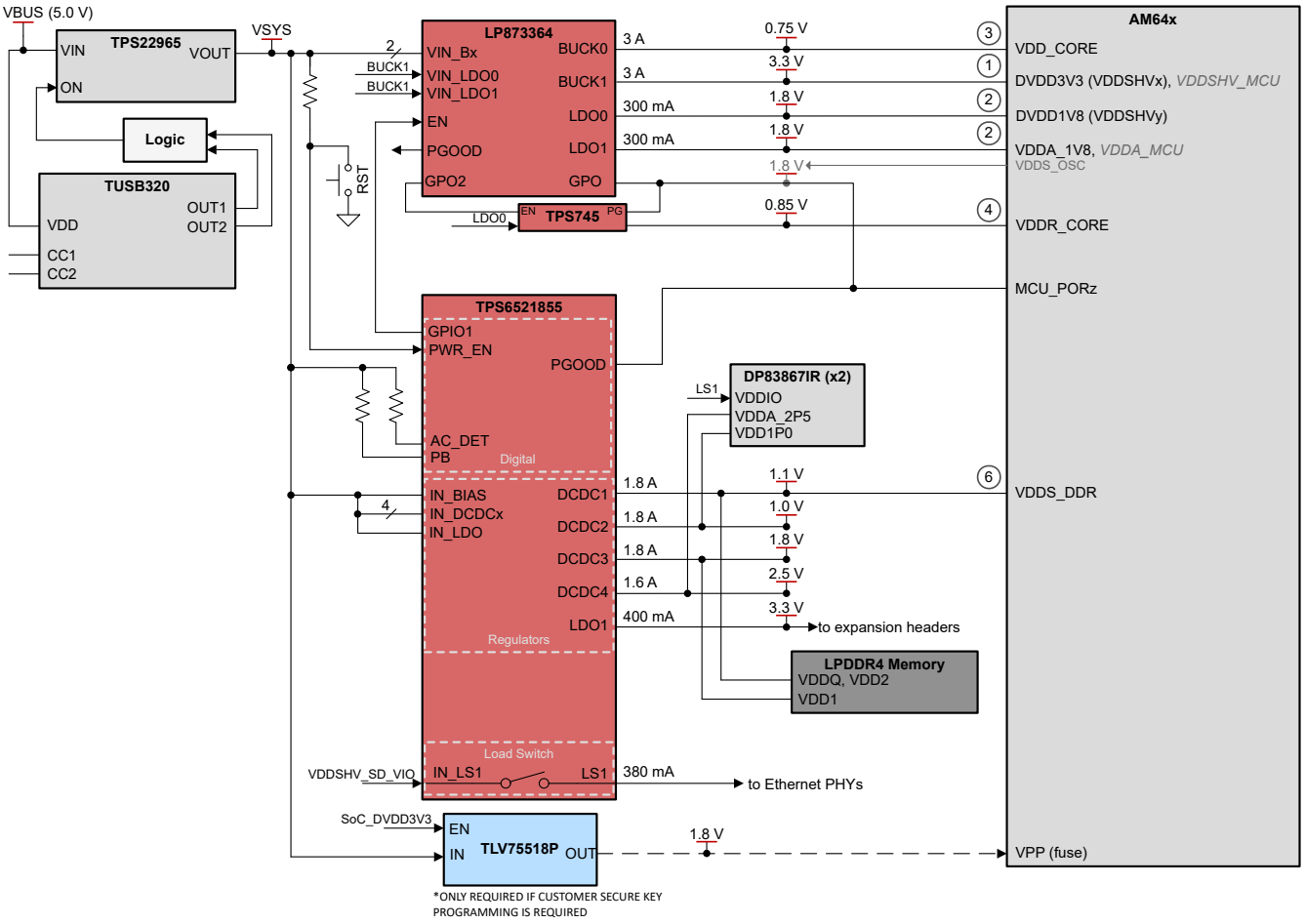
5.2 AM64x Dual-PMIC Solution

An example power map using LP873364 and TPS6521855 for the AM64x with LPDDR4 memory support is shown in Figure 5-3, and with DDR4 memory support in Figure 5-4.

This dual-PMIC solution is able to provide more rails and flexibility than the single-PMIC solution. The additional rails increase functionality such as allowing interface with additional ICs like TI's DP83867 Gigabyte PHYs.

TPS6521855 comes pre-programmed for interface with LPDDR4 memory. However, it maintains the programmable DIY functionality of the TPS65218xx family, so it can be reprogrammed for DDR4 memory use. Also, as further explained in Section 6, the *DIY* PMIC TPS6521815 can also be programmed to power this configuration.

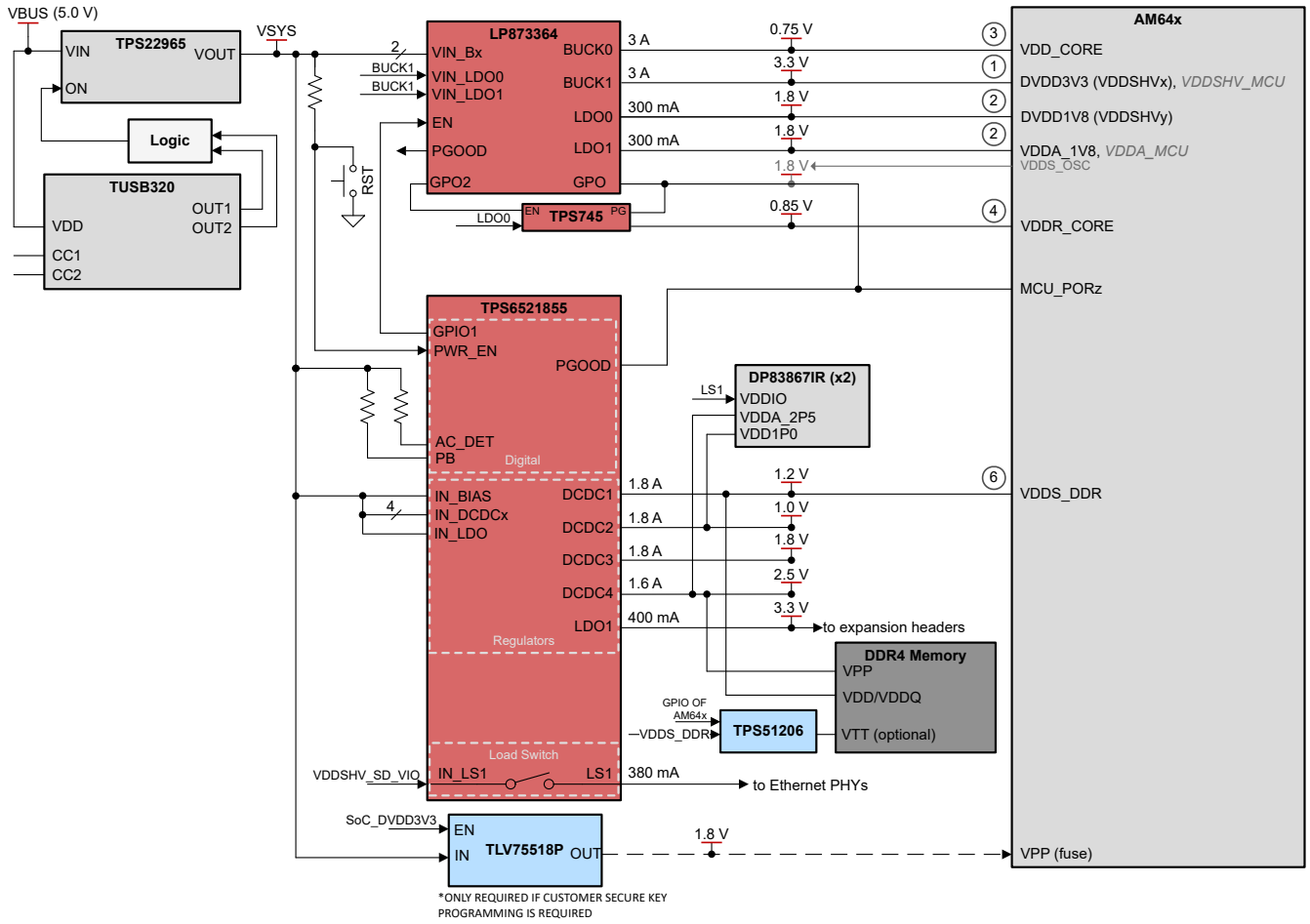
Please refer to the *Can the LP873364 be Used in a Dual PMIC Configuration?* section of the Powering the AM64x with the LP8733xx PMIC application brief for more information on implementing this solution.



Note 1: Please advise that this PMIC solution has been tested for power and sequencing, but has not been extensively tested for all fault conditions.

Note 2: DCDC3 should not be used as an alternative rail to LDO0 for DVDD1V8 as it will violate the AM64x power sequencing requirements

Figure 5-3. Using LP873364 and TPS6521855 to Power AM64x with LPDDR4 Memory and Ethernet PHY Support



Note 1: Please advise that this PMIC solution has been tested for power and sequencing, but has not been extensively tested for all fault conditions.

Note 2: DCDC3 should not be used as an alternative rail to LDO0 for DVDD1V8 as it will violate the AM64x power sequencing requirements

Figure 5-4. Using LP873364 and TPS6521855 to Power AM64x with DDR4 Memory and Ethernet PHY Support

5.3 AM243x (ALX Package) Single-PMIC Solution

Figure 5-5 shows an example power map using the LP87334D to power the core rails of the AM243x (ALX Package) processor. The AM243x (ALX Package) body size is 11 mm × 11 mm, and does not support LPDDR4 or DDR4 memory.

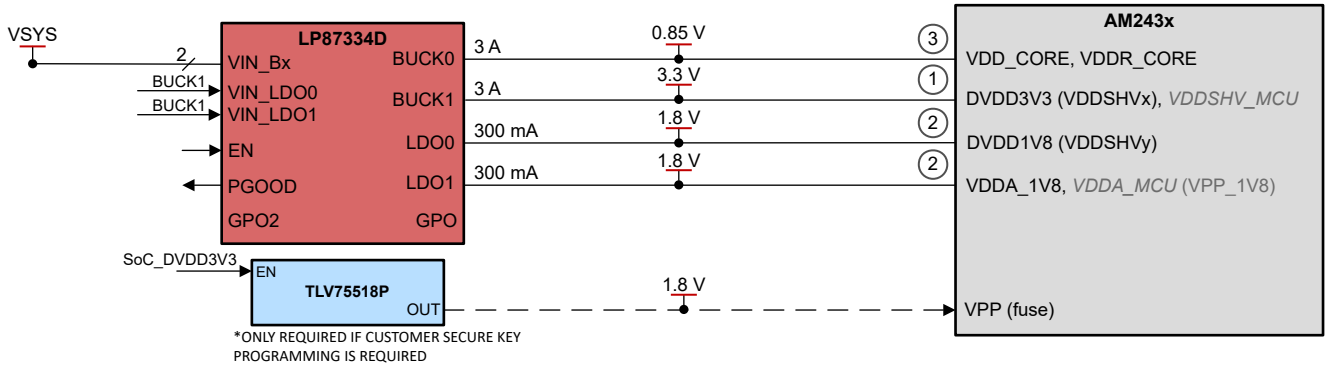


Figure 5-5. Using LP87334D to Power AM243x (ALX Package) Core Rails

Figure 5-6 shows an example power map that utilizes two GPOs to sequence additional regulators TPS62822 (buck regulator) and TPS745 (LDO) for Ethernet PHY support. TPS62822 can power 1.1 V Ethernet PHY when enabled by GPO2, and can be substituted with TPSM82822, a module with a step-down converter with an integrated inductor. TPS745 can power 2.5 V Ethernet PHY when enabled by LDO0, as shown in the below example power map.

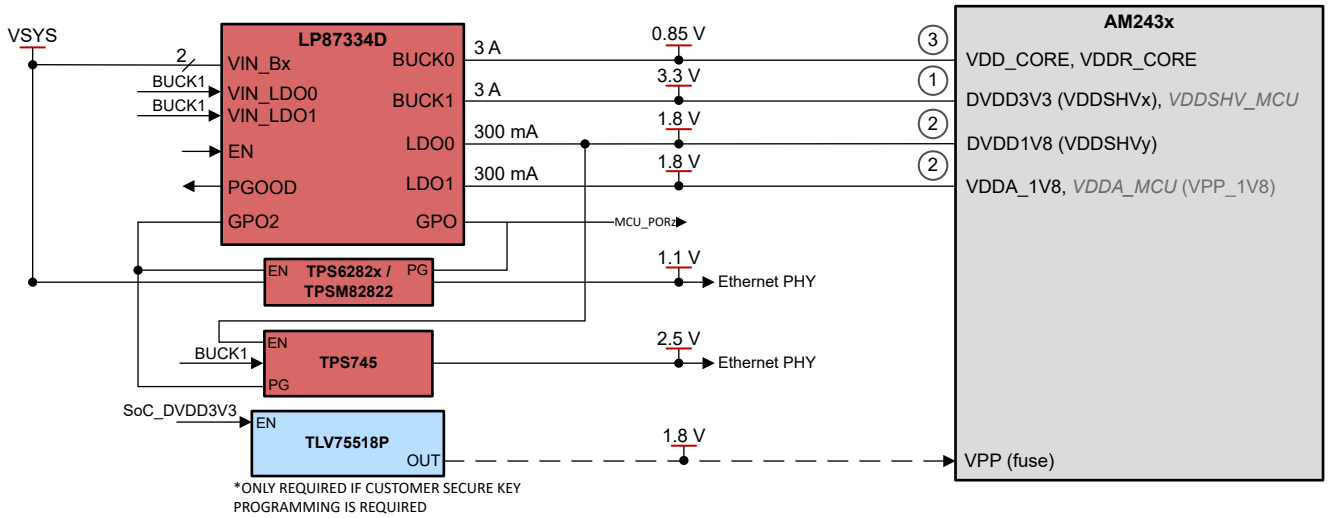


Figure 5-6. Using LP87334D to Power AM243x (ALX Package) with Ethernet PHY Support

5.4 AM243x (ALV Package) Single-PMIC Solution

An example power map using LP87334D to power the AM243x (ALV Package) processor with LPDDR4 memory support is shown in Figure 5-7, and with DDR4 memory support in Figure 5-8. The AM243x (ALV Package) body size is 17.2 mm × 17.2 mm, which has a benefit of pin-to-pin compatibility with the AM64x.

For applications using LPDDR4 memory, TPS62822 powers VDDS_DDR of the AM64x and VDD2 of the LPDDR4. TPS62822 is enabled by LP87334D GPO2, and can be substituted with TPSM82822, a module with a step-down converter with an integrated inductor. The memory's VDD1 is powered by LDO0 of the LP87334D.

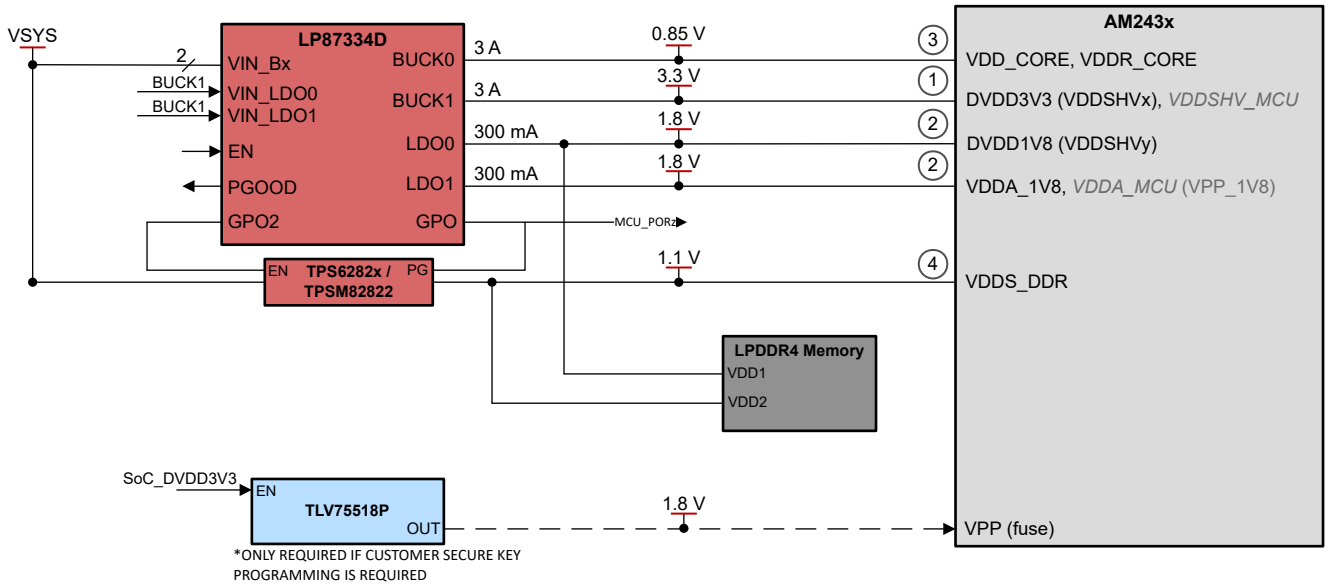


Figure 5-7. Using LP87334D to Power AM243x (ALV Package) with LPDDR4 Memory Support

For applications using DDR4 memory, TPS62822 (TPSM82822) powers VDDS_DDR of the AM64x and VDD of the DDR4. A discrete LDO TPS745 is enabled by LDO0 to supply the DDR4 VPP rail.

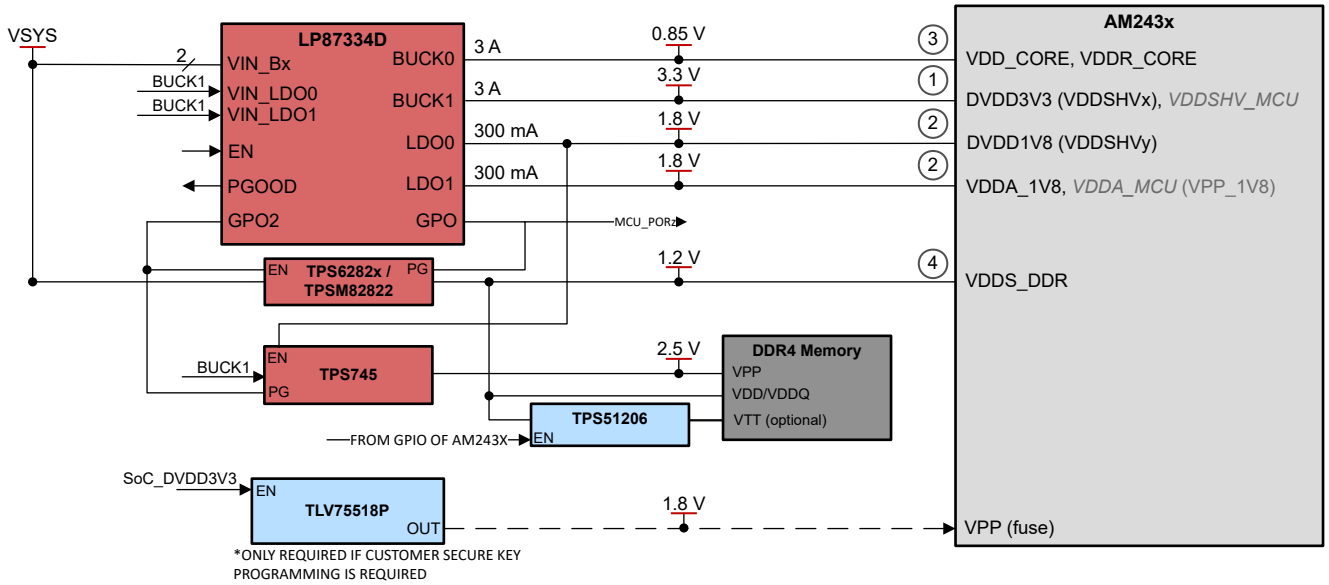


Figure 5-8. Using LP87334D to Power AM243x (ALV Package) with DDR4 Memory Support

6 TPS6521815 Programming Information

The user-programmable TPS6521815 is a NVM device that allows full customization of the output voltages, sequencing, GPIO control, and more to best meet system needs. The entire programming process is outlined in the TPS65218D0 Training Videos. Other resources to support the TPS6521815 programming process include:

- The BOOSTXL-TPS65218 BoosterPack™, which enables customer programming of the OTP memory of the TPS65218 for rapid prototyping and quicker time to market.
- The BOOSTXL-TPS65218 EVM User's Guide, which provides a guideline to program the OTP memory of the TPS65218 using BOOSTXL-TPS65218 BoosterPack™.
- The TPS521815 product folder for additional device information and available resources.
- Arrow Manufacturing Services for production programming services.

7 Conclusion

The LP733xx and TPS65218xx used either standalone or in conjunction can support the wide power needs and use cases of the AM64x and AM243x Sitara processor lines. This overview outlined the different use cases and benefits of each solution to help you select the right PMIC solution for your system. Example power maps were also provided to showcase different power configurations and help accelerate the design process. The highly integrated LP8733xx and TPS65218xx PMIC families have multiple technical benefits and features to deliver optimized power solutions for the AM64x and AM243x processor lines.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265