

PGA450-Q1 Reset Issue During VPWR Ramp Down

ABSTRACT

During a VPWR ramp down, the 8051W microcontroller comes out of reset incorrectly when VPWR is between the typical values of 3.5 V and 3.2 V which leads to faulty code execution. This application report describes this issue and the workaround for this issue.

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1 Overview

During a VPWR ramp down, the 8051W microcontroller comes out of reset incorrectly when VPWR is between the typical values of 3.5 V and 3.2 V which leads to faulty code execution.

The PGA450-Q1 device has an internal power-on-reset (POR) circuit and an AVDD undervoltage (AVDD UV) detection circuit. When the POR signal goes high, the digital core comes out of reset. However, the microprocessor remains in reset while the AVDD UV flag stays high which ensures that the microprocessor executes code only when VPWR has reached 5.5 V or higher.

During a ramp down, the AVDD flag incorrectly goes low when VPWR reaches 3.5 V. The POR signal does not go low until VPWR reaches 3.2 V. Therefore, a window exists on VPWR between 3.5 V and 3.2 V during which the microprocessor comes out of reset and starts begins code. With VPWR as low as 3.5 V, the internal regulators, oscillator, and biasing blocks are barely functional and well beyond the parametric limits which leads to faulty code execution. This is a problem only during a ramp down of VPWR. During a ramp up of VPWR, the POR signal goes high at 3.7 V, by which time the AVDD UV flag is functional, and the microprocessor remains in reset until VPWR is greater than 5.5 V.

Figure 1 shows the situation.

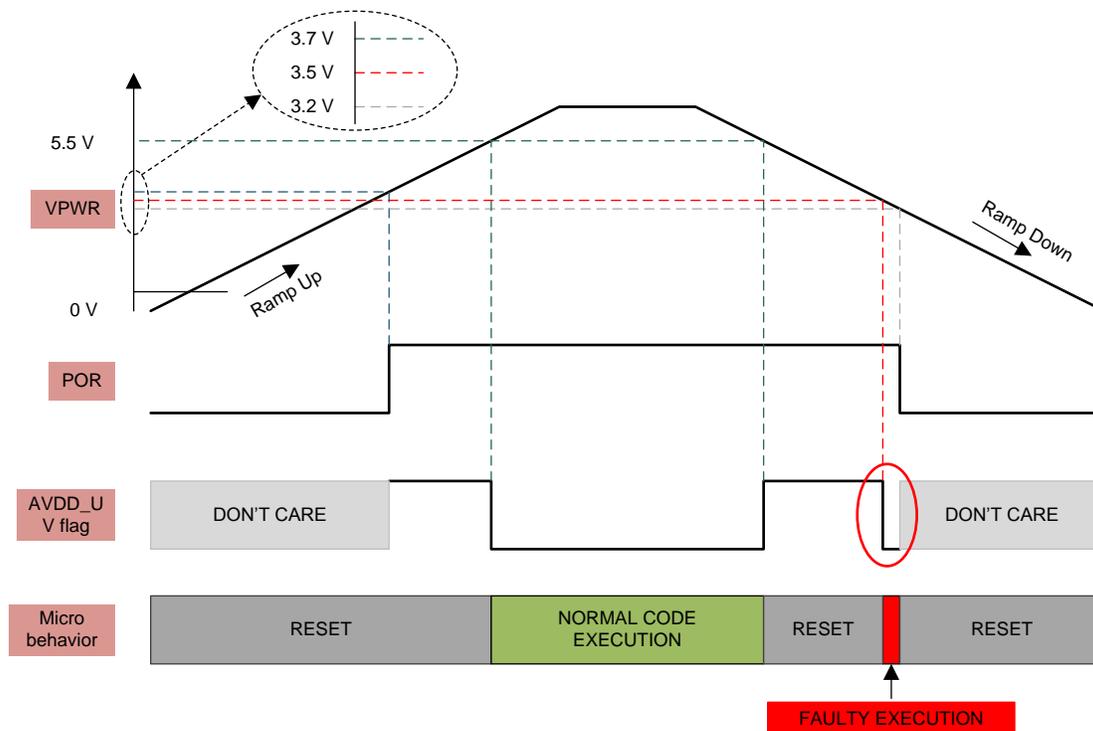


Figure 1. Faulty Code Execution During Ramp Down

2 System Impact

The release from reset while in an undervoltage condition can cause faulty code execution; however, the workaround should be simple to incorporate in most systems.

3 System Workaround

The VPWR ramp down should be faster than 1 V for every ms (especially from 4 V to 3 V). The 2-ms deglitch filter on the AVDD UV flag ensures that the microprocessor stays in reset during this ramp-down time. The necessary VPWR capacitor value to ensure this varies depending on the power source. A good value to begin with is 27 μ F.

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