

WiLink™ 8Q 0.65-mm Pitch Flip Chip Ball Grid Array Package Reference Guide

This document provides board mount application guidelines for Pb-free flip chip BGA packages with a 0.65 millimeter pitch, including device handling and management, PCB design guidelines, PCB assembly parameters, rework processes and troubleshooting.

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Trademarks

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1 Introduction

The WiLink™ 8 WL18xxQ is a highly integrated single-chip CMOS (45-nm process) WLAN, BT, BLE, ANT device that forms a complete stand-alone communication system. The device is the 8th-generation connectivity combo chip from TI. The WL18xxQ is based upon proven technology and complements the TI integrated devices for connectivity portfolio. This device is ideal for use in mobile devices, mobile computer, and catalog embedded device applications due to its low-current, small area, and coexistence-friendly features.

1.1 0.65-mm FCBGA Pitch Application Report Scope

1.1.1 Generic Product Description

- 0.65-mm pitch FCBGA
- Organic material based substrate
- ROHS and Lead-free compliant

The information and data contained within the bulletin are based on extensive laboratory testing, industry-recognized best practices and the following package characteristics:

- FCBGA pitch: 0.65 mm
- Mass: 0.2 to 0.3 g, depending on body size
- Ball diameter: 0.4 mm
- Co-planarity: 0.10-mm maximum

1.2 Example of a Mechanical Drawing for a 0.65-mm FCBGA Pitch Package

For an example of a WiLink 8Q 0.65-mm BGA Pitch Package, see [Figure 15](#).

2 PCB Design Considerations

2.1 Land Diameters and Solder Mask Opening Diameters

The primary board design considerations include metal-pad sizes and associated solder-mask openings. PCB pads/land patterns, which are used for surface mount assembly:

- Non-solder mask defined (NSMD) — The metal pad on the PCB (to which a package BGA solder ball is attached) is smaller than the solder mask opening.

Figure 1 and Figure 2 illustrate the metal-pad and associated solder-mask openings

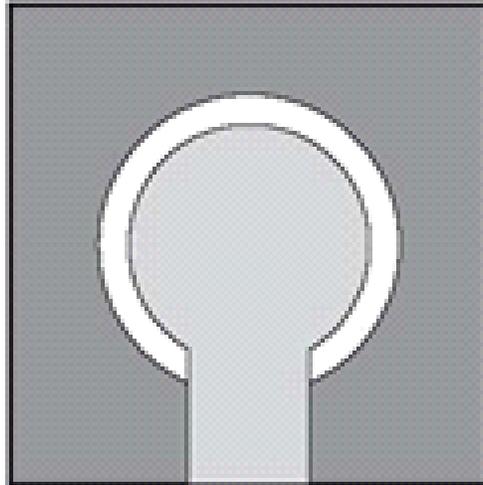


Figure 1. NSMD Pads – Top View

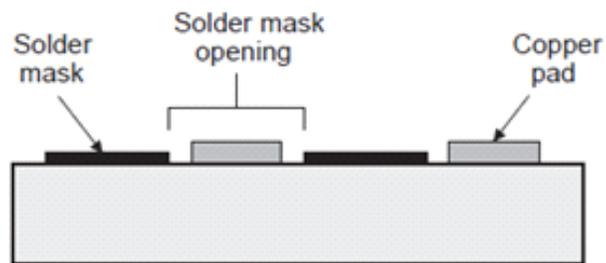


Figure 2. NSMD – Cross-Sectional View

2.1.1 Non-Solder-Mask-Defined (NSMD) Land

With NSMD-configured pads, there is a gap between the solder mask and the circular contact pad (refer to [Figure 1](#)). With this configuration, the solder flows over the top surface and the sides of the contact pad.

NSMD lands have these advantages:

- The additional NSMD soldering area results in a stronger mechanical bond
- NSMD pads are smaller than SMD pads, allowing more room for escape trace routing

A disadvantage of the NSMD land is that surrounding traces can be exposed if not properly dimensioned, providing potential for short circuits during ball attach and reflow.

[Table 1](#) shows optimum solder mask opening land pad diameters for the package and the PCB for a flip chip BGA with 0.65-mm pitch. The solder mask on NSMD lands is considered a PCB fabrication process defect.

Table 1. Recommended PCB Land Pattern Design Guidelines⁽¹⁾

Ball Pitch	Ball Size ⁽²⁾	Solder Mask Type	PCB Design		Stencil Design		Area Aspect Ratio ⁽³⁾⁽⁴⁾
			SMO	Pad Size	Thickness	Aperture	
0.65	0.4	NSMD	0.45	0.35	0.10–0.125	0.35	0.69

⁽¹⁾ All measurement are in mm.

⁽²⁾ Ball size, SMO(solder mask opening), Pad Size, and Aperture are shown as diameters.

⁽³⁾ Area Aspect Ratio = Area of Aperture / Area of Aperture Wall

⁽⁴⁾ For optimal release of solder paste, it is recommended the Area Aspect Ratio ≥ 0.66 .

2.2 PCB Routing

2.2.1 Routing of 0.65mm pitch Standard BGA Arrays

Routing of PCB for parts with 0.65-mm pitch depends on the configuration of the BGA array, the number of signals being routed and the size of the land pad. Typical escape routing strategies include the following:

First two outside rows: the first two outside rows of balls are usually routed easily on the top layer of the PCB. The first row has traces going straight out from the BGA footprint, and the second row is easily routed in between the balls of the first row. The 0.65-mm pitch will allow standard and economical 0.1-mm (4 mil) trace size with 0.1-mm (4 mil) clearance between features (NSMD design only).

Third row: the third row usually cannot get out past the congestion of the first two rows on the top layer, and requires a via to get to the second routing layer. On a full ball or standard BGA array, the via needs to be placed in between four balls, next to the balls on the third row. Due to the restricted placement area, typical PCB manufacturing practices that require an 18-mil diameter annular ring/10 mil-hole (18/10) cannot be used because it is not possible to fit an 18-mil diameter via in between the four balls at 0.65-mm pitch.

Given the routing constraints of 0.65-mm pitch standard BGA components, there are two main paths for routing PCB boards, and they can be differentiated by cost.

The more economical routing solution for 0.65-mm pitch standard BGA, which typically adds about 20%–25% to the PCB cost relative to 0.8-mm pitch, uses 16-mil diameter vias with 8 mil diameter finished hole size (16/8) and 4-mil trace/space rules.

The 16/8 vias sizes offer the lowest cost solution, but are only practical if:

- The PCB manufacturer has proven capability in creating 16-mil diameter vias in production quantities, a trend that is emerging at the time of publication
- The design does not use all the BGA balls. When using 16-mil vias, the layout will only permit 4-mil traces between every other via; therefore, creative routing strategies are required. Sometimes routing out with 16/8 vias is possible; sometimes it is not, depending on the device and the design.

The costlier, but often more realistic solution typically applied to 0.65-mm pitch, usually at 2× the PCB cost of 0.8-mm pitch, involves use of 12- to 14-mil diameter High Density Interconnect (HDI) micro vias with 6- to 7-mil holes and 3- to 4-mil trace/space rules.

- This design approach is more common and often used when space is at a premium
- If other components dictate HDI interconnects regardless of the BGA layout, then there is no added cost (because micro vias are already in use) and PCB size is greatly reduced

Table 2 shows PCB feature sizes for standard BGA arrays with 0.65-mm pitch.

Table 2. PCB Features for Both Standard and Via Channel BGA Arrays

PCB Typical Feature Sizes For Standard and Via-Channel 0.65-mm pitch BGA Arrays					
BGA Array Type	Via Diameter	Via Hole Size	Trace Size	Clearance	Micro Vias?
Standard	16 mil ⁽¹⁾	8 mil ⁽¹⁾	4 mil ⁽¹⁾	4 mil*	No

⁽¹⁾ 16/8 vias are possible for best case scenarios. 16-mil diameter/8-mil hole vias are only possible if done in a creative way that puts traces only in between every other via. 16/8 vias, when placed between the balls, will move enough to allow one 4 mil trace per pair, but not one 4 mil trace per via. Therefore, 16/8-mil vias should be possible in some applications but not all. For a full BGA array, it is not possible to use them. Also, 16/8 vias are not widely available on production scales at the time of publishing.

2.2.2 PCB Layer Counts

2.2.2.1 PCB Layer Count for Standard BGA Arrays

The layers required to route a particular design can be easily estimated given the number and locations of signals. Assuming the PCB feature sizes in [Table 2](#), the PCB would be routed as follows:

- The first 2 rows will route on the top layer. The second 2 rows will route on the second layer. An additional PCB layer will be required for every row in past the first 2.
- Therefore, if "Rows_in" = the maximum number of rows in (from the outside of the BGA array) the centermost signal is located, then:
 - 2 Rows_in = 1 PCB signal layer
 - 3 Rows_in = 2 PCB signal layers
 - 4 Rows_in = 2 PCB signal layers
 - 5 Rows_in = 3 PCB signal layers
 - 6 Rows_in = 4 PCB signal layers
 - 7 Rows_in = 5 PCB signal layers

For example, if a signal called I2C_CLK were required in the design, and it was located five rows in from the outside (counting all rows), then it would require 3 PCB signal layers, plus at least 2 PCB layers for power and ground, adding to 5 layers total. Because PCBs are manufactured with layer symmetry about the centerline, a 6 layer PCB would be specified.

Depending on the power requirements and the power signal routing, an additional power layer may be required, but can be avoided with strategic design practices.

2.3 Keep Out Zones

A minimum 3.8-mm (0.150") clearance should be maintained around the perimeter of the component.

If the edges of the boards are to be used for conveyer transfer, a cleared zone of at least 3.17 mm (0.125") should be allowed. Usually, the longest edges of the board are used for this purpose, and the actual width of the keep out area depends on equipment capability. Although no component lands or fiducials can be present in this area, breakaway tabs may be in it.

2.4 Summary of PCB Design Recommendations

[Table 3](#) lists the basic design recommendations for a WiLink 8 FCBGA PCB.

Table 3. WiLink 8Q FCBGA Package Circuit Board Design Recommendations

Design Area/Parameter		
Pad Design Recommendations	Pad geometry (mm)	0.32
	Pad opening (mm, NSMD)	0.45
PCB Assembly Recommendations	Solder paste type (Pb-free)	Sn/Ag/Cu-based
	Stencil thickness (mm)	0.10 to 0.125
	Recommended PCB surface finish	OSP
	Maximum reflow temperature (°C)	+260°C
	Maximum reflow time (sec)	40 to 60
	Maximum soak temperature (°C)	+180°C
	Maximum soak time (sec)	90 sec
	# Reflow maximum	Maximum 3
Package Storage Information	Storage conditions	≤ 30°C/85% RH
	Moisture sensitivity level (MSL)	L3
	Possible prebake recommendations	125C/24H

3 Solder Paste and Stencil Printing

3.1 Solder Paste Selection

The FCBGA is compatible with a broad range of commercially available Type 3 (mesh size –325/+500, particle size 25-45 μm) and Type 4 (mesh size –400/+625, particle size 20–38 μm) solder pastes.

The component has been assembly tested with both no-clean and water-washable lead-free solder paste products. Due to the I/O density and low package standoff, no clean solder processes are recommended. If water-washable assembly materials are used, cleaning process information is presented in [Section 6](#).

3.2 Stencil Design

The optimum stencil design is 0.35-mm (0.014") circular apertures on 1250 μm (0.005") foils. These dimensions produce a pad-to-wall Area Ratio of 0.70, and should consistently supply approximately 0.013 mm³ (770 mils³) of solder paste for each deposit. Smaller apertures or thicker foils may change the Area Ratio, the paste deposit volumes, and the repeatability of the print process.

The 0.35-mm (0.014") square apertures, as well as 0.30-mm (0.012") and 0.40-mm (0.016") diameter circular apertures have been tested and provided acceptable results. However, square apertures may introduce variation to the paste deposits' print definition and volume repeatability. Additionally, smaller circular apertures may increase the risk of open joints or head-in-pillow defects, and larger circular apertures increase the risk of solder bridges and solder balls.

Stencil thicknesses other than 0.005" have not been tested. If PCB design mandates other foil thicknesses, the aperture sizes should be adjusted appropriately to maintain a area ratio of 0.66".

3.3 Stencil Print Registration

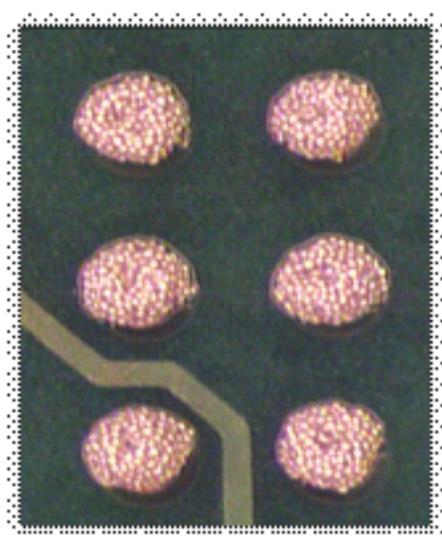


Figure 3. Preferred Solder Paste Alignment

Ideally, paste prints should be centered on the PCB pad, as seen in [Figure 3](#) Mis-registration of up to 50 μm (0.002") in X and/or Y directions is acceptable. Print offsets greater than 50 μm (0.002"), are not acceptable and the print should be rejected.

3.4 Solder Paste Print Quality

Poor quality solder paste prints are the primary source of PCB assembly defects that require rework. The FCBGA rework process is highly dependent on operator skill level and presents a risk of permanent damage to the PCB. Therefore, care should be taken to optimize and monitor the stencil printing process to insure the best possible solder paste print quality.

4 Pick and Place Process

4.1 Packaging

Components are shipped in standard JEDEC trays. The trays are sealed in moisture barrier bags with desiccants and humidity indicator cards.

4.1.1 Moisture Sensitivity and Pre-bake

The Moisture Sensitivity Level (MSL) of the devices is Level 3.

If components are removed from their protective storage environment and exposed to ambient environment ($\leq 30^{\circ}\text{C}/60\%RH$) for more than 168 hours, bake for a minimum of 48 hours at 125°C (260°F), or in accordance with guidelines contained within IPC/JEDEC J-STD-033B (available on-line at www.jedec.org) to prevent package damage from the outgassing of absorbed moisture.

4.2 Electrostatic Discharge Sensitive Devices (ESDS)

All electronic components can be damaged by electrostatic discharge (ESD) throughout their life cycle. Static charge is produced whenever there is movement. ESD controls help to reduce charge generation, limit potential differences between objects (grounding), neutralize charges (ionizers), and remove field effects.

Devices assembled in flip chip BGA packages should be considered ESD-sensitive. Care in handling should be used when processing FCBGA packages.

4.3 Component Weight

The mass of the component is approximately 0.2 to 0.3 g for this body size.

4.4 Nozzle Selection

Nozzles should have a vacuum area sufficient to prevent the device from slipping or spinning during rotation. In applications testing, a 0.34" diameter nozzle provided enough suction to maintain stability during movement in the placement system.

4.5 Vision and Alignment

It is preferred that placement machine vision systems capture the entire perimeter arrays for best alignment results. It is acceptable to use only corner balls for alignment, but the centering process may not be as accurate as when the full perimeter is used.

4.6 Ball Presence

All components are checked for 100% ball presence as part of TI's extensive quality assurance procedure. However, balls can occasionally get removed, generally due to improper handling in transit from the BGA packaging facility to the assembler's production line. It is suggested that a ball presence check be performed by the placement machine vision system. If the vision system is not capable of checking all balls, it should be programmed to check as many as possible.

4.7 Placement Force

Placement force of 150 grams has been used in laboratory testing and has proven to be a satisfactory placement force, retaining the component during conveyance between machines on a typical SMT line. Lower placement forces may not properly retain the component; higher placement forces may deform the solder paste deposits. Either deviation may cause soldering defects.

4.8 Placement Accuracy and Self-Centering

Fine Pitch placement machines should typically place components within 25 μm (0.001") of the programmed location.

To simulate a worst-case scenario, placement was tested with 100- μm (0.004") offsets in both X and Y directions concurrently. In this test, components all self-centered, no soldering defects were formed, and no solder balls were observed under X-ray inspection.

5 Reflow

5.1 Instrumentation

The reflow process should be thermally profiled using thermocouples and a digital data logger.

5.2 Thermocouple Attachment

Each of three key areas on the device should have at least one thermocouple attached: balls on the inner array, balls on the perimeter/outside corner, and the package body.

5.3 Reflow Profile Considerations

The solder paste manufacturer's guidelines for reflow parameters should be applied when profiling PCBs. The components have soldered satisfactorily in tests with peak temperatures ranging from 230°C to 240°C, and TALs from 45 to 150 seconds.

The component's body temperature should not exceed 260°C at any time during the reflow process.

The component's body temperature should not exceed 255°C for more than 30 seconds.

An example of a typical soak profile is shown in [Figure 4](#). It is a soak-style profile; straight ramp-style profiles such as the one seen in [Figure 8](#) (rework section) are also acceptable.

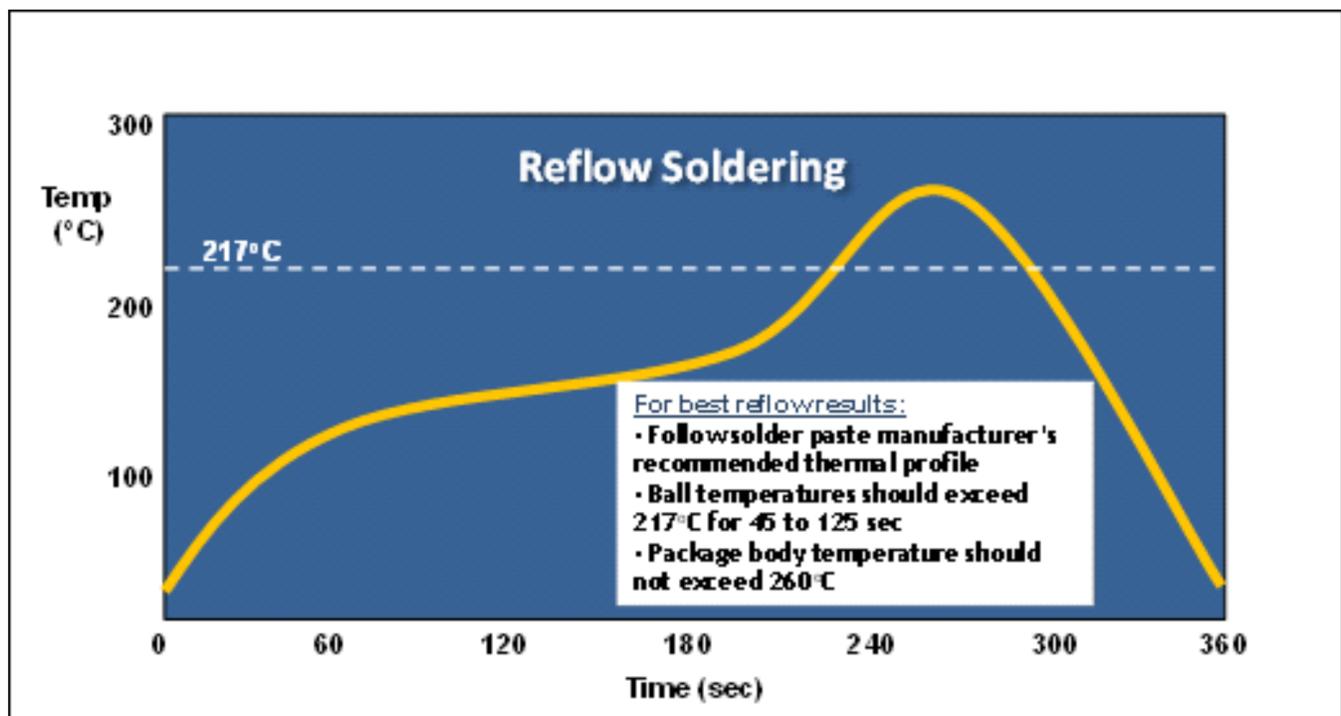


Figure 4. Sample Reflow Profile

5.4 Reflow Environment

Assemblies were tested in both air and nitrogen environments, and demonstrated good soldering in both. The nitrogen environments that were used contained between 1000 ppm and 2000 ppm O₂.

5.5 Double-Sided Reflow

Assemblies were tested on a second reflow pass with the assembly inverted. X-ray inspection showed no open or head-in-pillow defects after the second pass, indicating double-sided reflow compatibility.

5.6 Alternative Alloys

All test assemblies were soldered with SAC305 (Sn3.0Ag0.5Cu) alloy. No alternative alloys have been tested.

6 Defluxing (Cleaning)

6.1 Water Cleanability

Test assemblies were soldered with water-washable solder paste and cleaned in an in-line, deionized water-only process. The washed board was tested with an ionograph, and no contamination was detected.

6.2 Cleaning Agents

Depending on cleaner equipment and process configuration, saponifiers may be added to the wash process to ensure cleanliness underneath the component.

6.3 Cleanliness Testing

Overall assembly cleanliness may be assessed with an ionograph; however, this test method averages the detected contamination over the entire surface area of the PCB and is not a direct indicator of complete flux residue removal from underneath the component. Ion chromatography of the PCB area under the component is the best way to validate cleanliness during assembly process development. The innermost area of the device should be tested, as shown in [Figure 5](#).

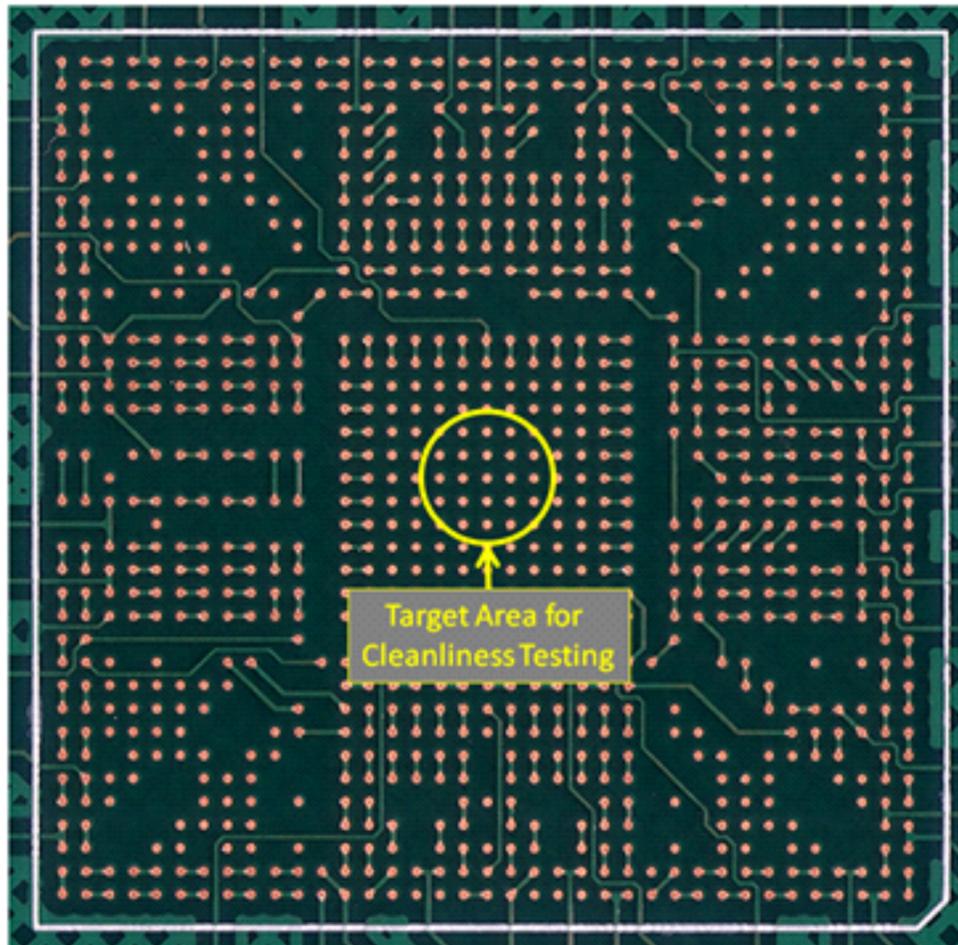


Figure 5. Example of Key Area to Test for Complete Flux Residue Removal

6.4 Process Validation

Prior to production, the adequacy of the cleaning process should be verified via ion chromatography.

In general, aqueous cleaning processes should be regularly monitored to assure that they are performing as expected. Incomplete removal of water-washable flux residues can cause electromigration, dendritic growth, and ultimate failure of the circuit assemblies while in service.

7 Inspection

7.1 Sampling Frequency

It is suggested that 100% of the assemblies be inspected with X-Ray imaging as part of their production process.

7.2 Automatic X-Ray Inspection (AXI)

The 3-dimensional AXI is the best available method for BGA solder defect detection in production environments. Due to the possibility of false calls, however, defects should be verified visually or with 2-D X-ray analysis before any rework is performed.

7.3 Visual Inspection

Visual inspection, using mirrors, prisms, or microscopes fitted with fiber optic cameras can be used to verify defects if they are detected in the outermost row/column of outer perimeter array balls, as seen in [Figure 6](#).

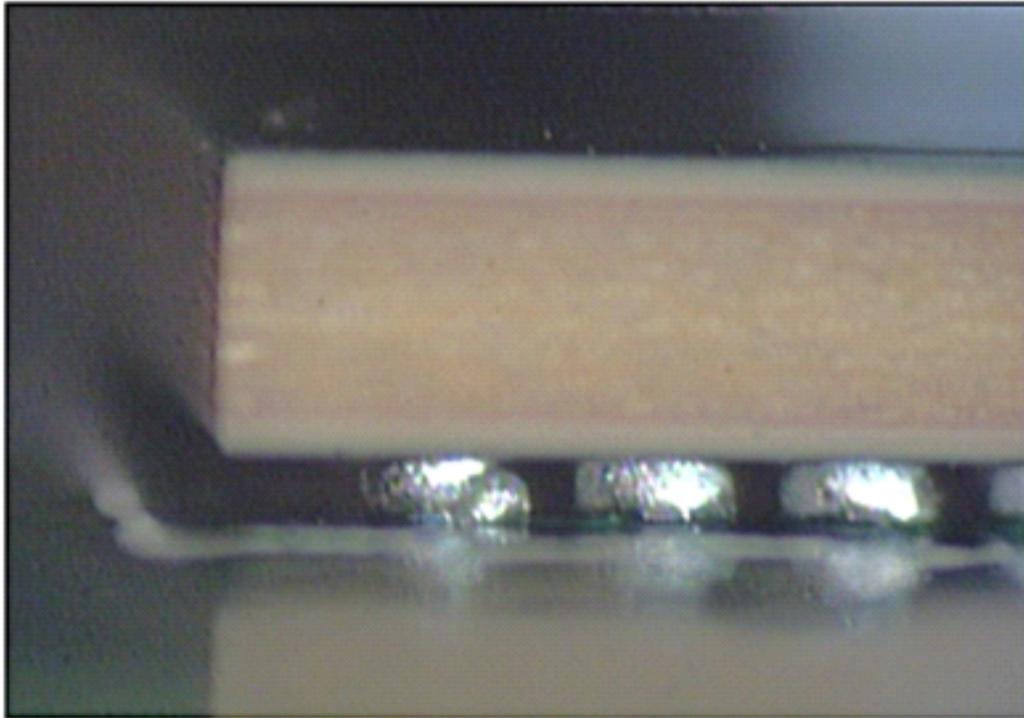


Figure 6. Example of Soldering Defect (Head-In-Pillow) on Perimeter Verified Visually

7.4 Transmission 2-dimensional X-ray

Transmission X-ray inspection, especially at orthogonal angles, can be used to

1. identify defects if 3-dimensional X-ray is not available
2. verify defects identified by 3-dimensional X-ray inspection

Figure 7 shows a head in pillow defect located using 2-dimensional X-ray.

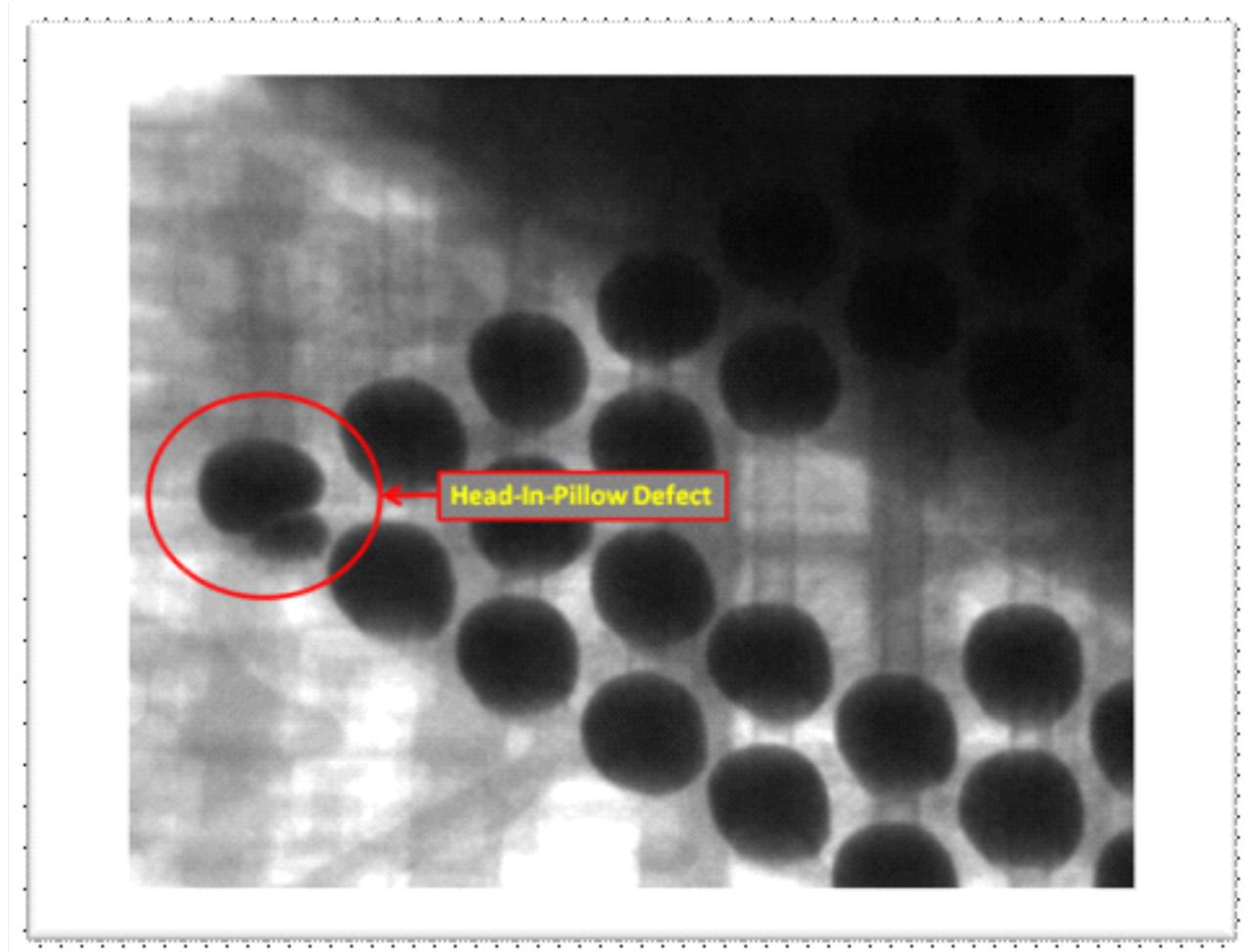


Figure 7. Example of Defect Verified with 2-D X-Ray

8 Rework

8.1 Necessity and Prevention

If soldering defects are identified during inspection, they must be carefully reworked using the best available practices. Proper rework equipment and highly skilled operators are required to perform these operations. Additionally, SMT processes should be optimized to prevent soldering defects, because each step of the rework process presents risk of irreparable damage to the PCB.

8.2 Pre-bake

Prior to rework, the assembly should be baked for 24 hours at 105°C to remove any absorbed moisture into the PCB or components. If heat-sensitive components are on the PCB, they should be removed before the pre-bake step of the process.

8.3 Thermal Profiles

Each unique PCB design must be profiled in the rework station on which it will be processed. PCB thermal densities vary from one design to another, and rework equipment thermal transfer efficiencies vary from one machine to another.

8.4 Reflow Profile Considerations

Thermal profile considerations are similar to those for the mass reflow of the PCB:

Preheat should be applied from both sides of the PCB.

Some rework stations offer optional body cooling. If the machine is equipped with this option, it should be used. If it is not equipped, care should be taken to insure the package body temperature does not exceed 260°C, and does not exceed 255°C for more than 30 seconds.

If small discrete components are located close enough to the edges of the package to get reflowed during the thermal process, they may be temporarily removed and resoldered after the rework is completed, or they can be covered with polyimide tape to maintain their position during the BGA removal and replacement process.

Figure 8 shows a typical rework profile.

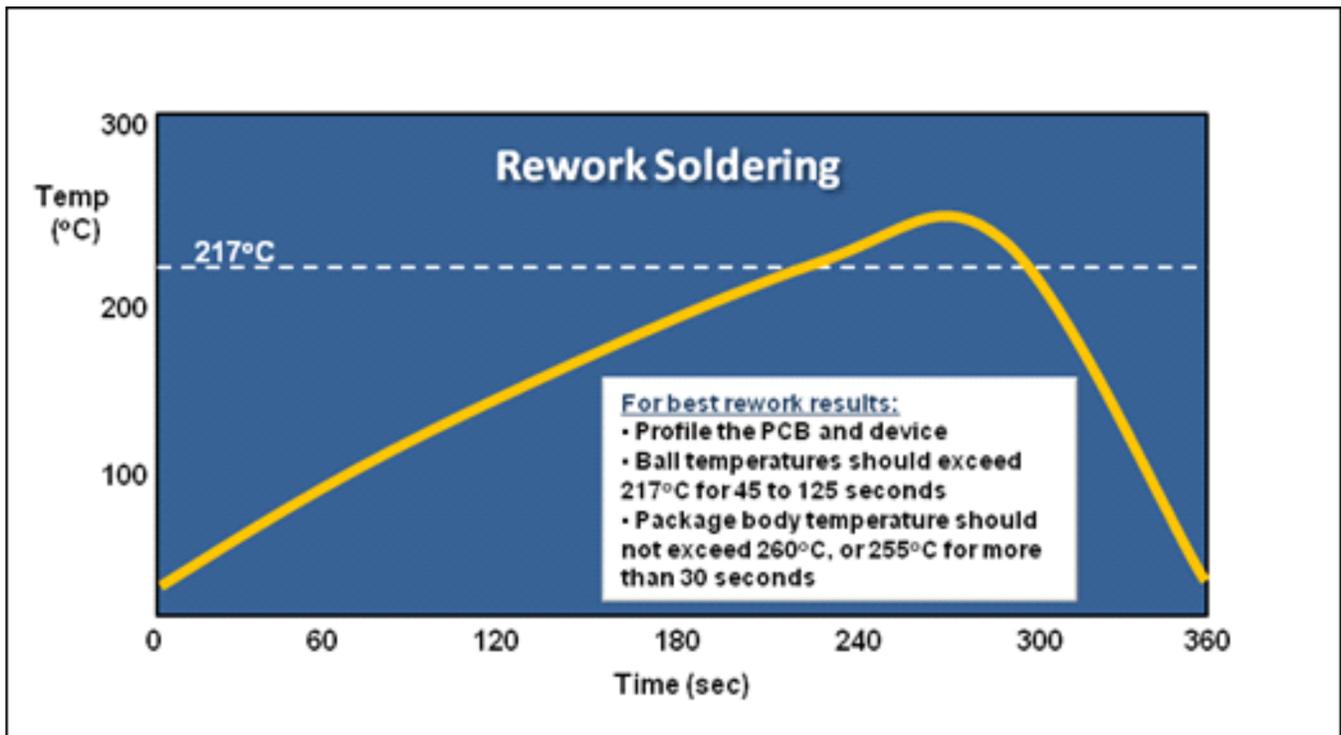


Figure 8. Rework Profile Considerations

8.5 Device Removal and Inspection

A standard square nozzle matched to the package size is recommended for device removal and replacement. Air or nitrogen may be used as a gas medium. Once all the solder joints have reached liquidus temperatures, the device should be lifted directly off the board with the rework machine's vacuum head. The component should be scrapped and replaced with a new device. Removing and re-using the component can impact its reliability.

The PCB should also be inspected to insure no solder mask or pads have been lifted in the process, as seen in [Figure 9](#). If pads are lifted, the PCB should be scrapped, as some of the pads contain microvias. If solder mask has been lifted, it may be repaired using standard mask repair supplies and techniques.

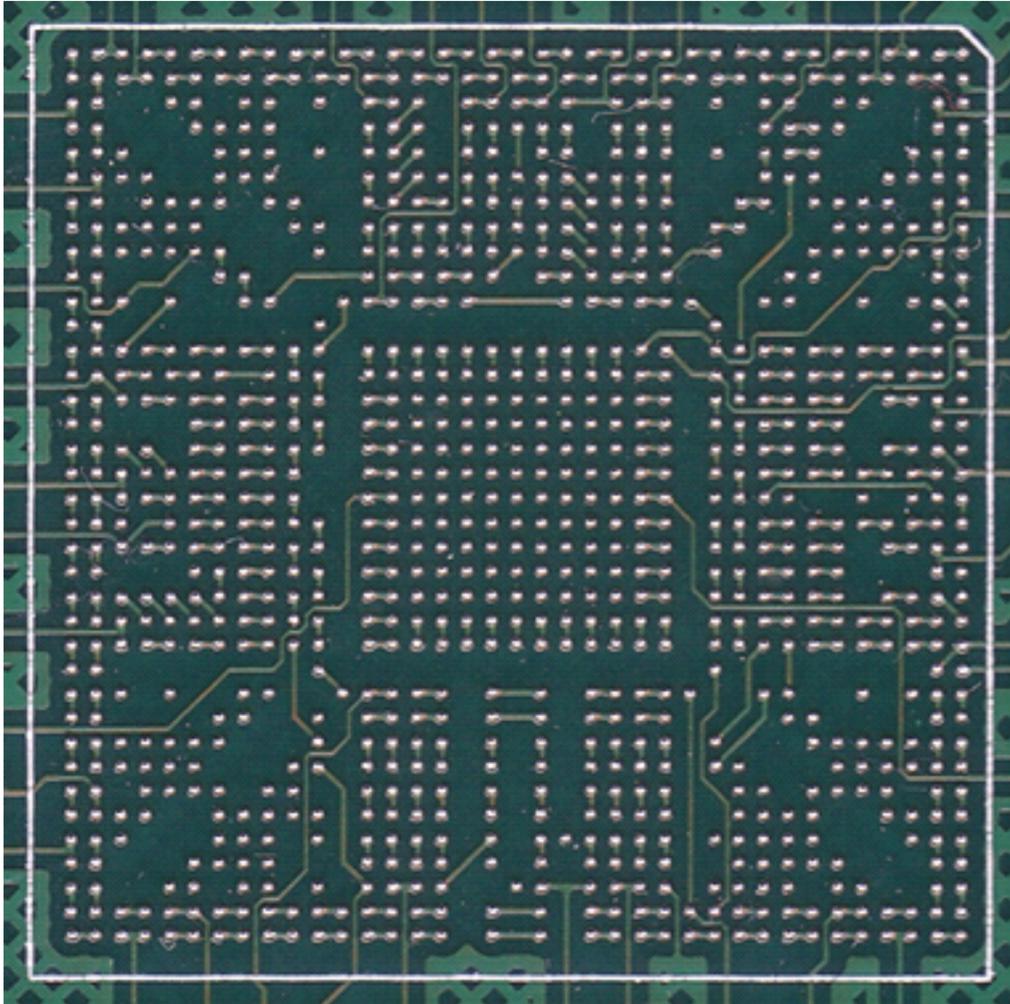


Figure 9. Example of PCB Inspection after Device Removal

8.6 Site Redressing

Excess solder that remains on the PCB pads should only be removed by automated vacuum scavenging, preferably with automatic height control, as shown in [Figure 10](#).

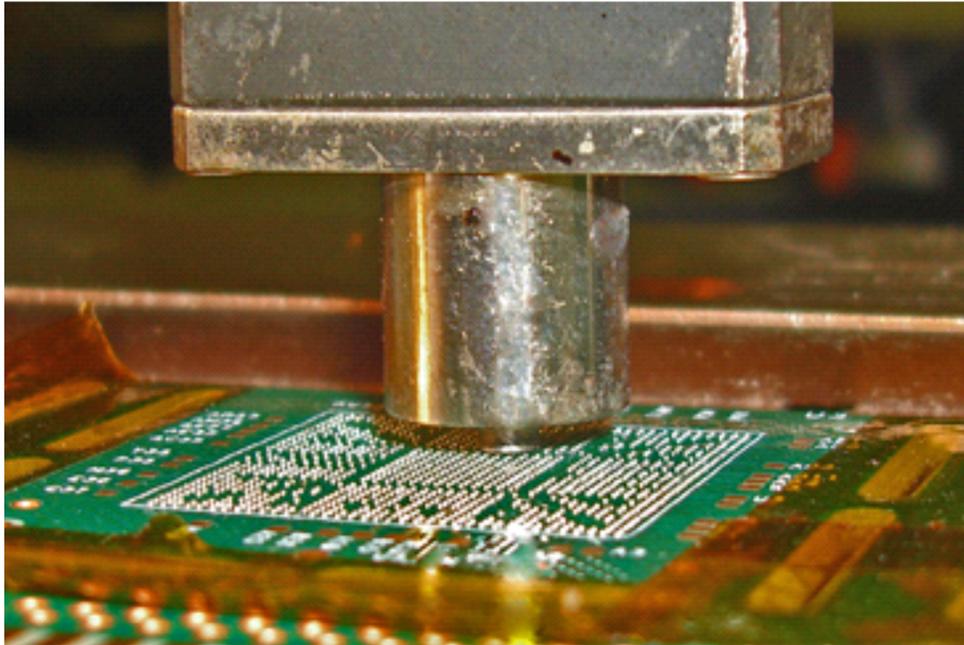


Figure 10. Example of Automated Vacuum Removal of Excess Solder from Pads

After scavenging, some solder should remain on the pads, as shown in [Figure 11](#).

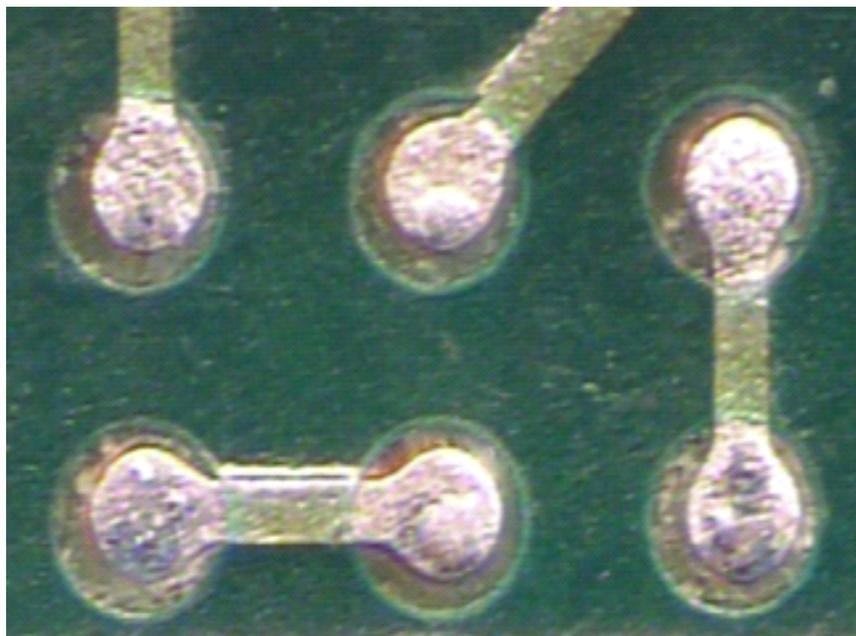


Figure 11. Example of Cleaned PCB Pads Ready to Accept Fresh Solder Paste

The pitch and population density 0.65mm devices preclude manual vacuum scavenging or solder wicking with braid. Both manual processes are likely to lift pads and/or damage solder mask, and therefore are not recommended.

8.7 Solder Replenishment

The rework process must include solder replenishment. Repair processes that use flux only are not recommended, as they are more likely to result in soldering or positional defects. Two methods of solder replenishment are available: depositing paste on the circuit board, and depositing paste on the balls.

8.7.1 Preferred Method: Paste on PCB

If proper clearance is available around the perimeter of the device to accommodate a small metal or polyimide stencil, this method should be used, as it is more robust than printing solder paste directly onto the device's balls.

Rework stencils for depositing solder paste onto the PCB should use the same recommended design as the SMT stencils: 0.35-mm (0.014") circular apertures on 125- μ m (0.005") foils.

8.7.2 Acceptable Method: Paste on Balls

The application of solder paste directly onto the solder balls is acceptable if a small stencil cannot be fit onto the PCB, but it is not as robust as printing onto the PCB itself. It supplies less solder paste volume and is less predictable, thereby offering more opportunities for open, insufficient, or head-in-pillow solder defects.

If paste is printed on the balls, a small fixture to hold the stencil and device, like the one shown in [Figure 12](#), should be installed on the rework station.

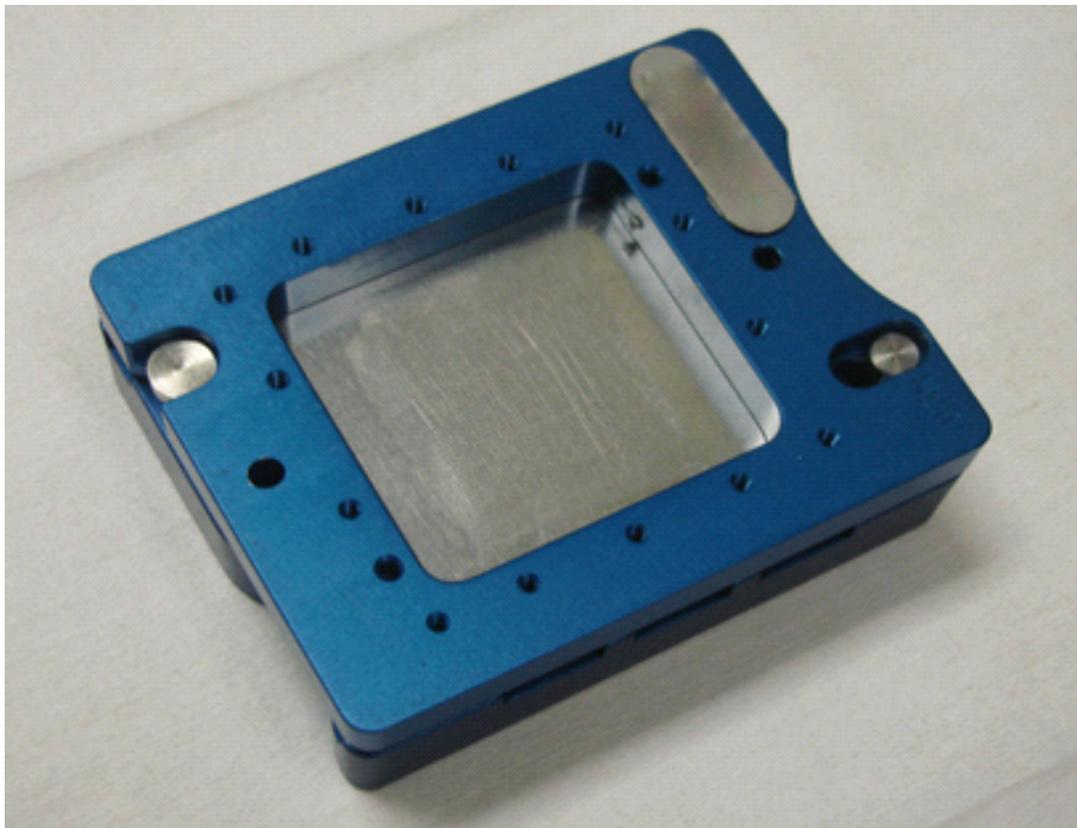


Figure 12. Example of Fixture for Printing Paste on BGA Balls

Tests conducted using the paste on ball method with 0.23 × 0.30-mm (0.009 × 0.012") rectangular apertures produced acceptable solder joints, but, the solder paste deposits have lower volumes and are less consistent than when they are printed on the PCB pads.

Figure 13 and Figure 14 show the same photo of typical paste-on-ball solder paste prints. The paste deposits have been outlined in red to illustrate the variation in deposit consistency that is characteristic of the paste-on-ball printing process.

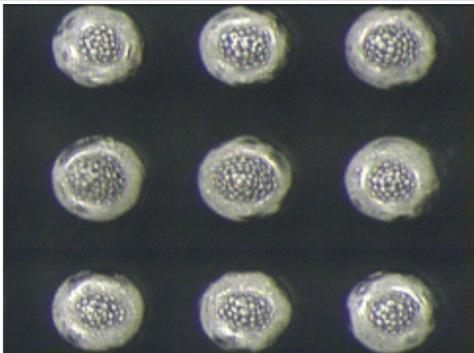


Figure 13. Example of Solder Paste Printed on BGA Balls

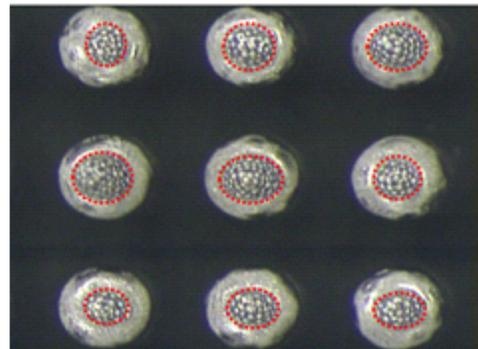


Figure 14. Example of Solder Paste Volume Variation on BGA Balls

8.8 Device Replacement

The component should be aligned with the pads using the optics on the rework station. Placement force should be minimal.

8.9 Reflow Soldering

The same customized reflow profile that was used to remove the device should be used to replace it. Nitrogen, if available, can be used to resolder the component; tests in air produced satisfactory results.

8.10 Inspection

Solder joints should undergo 100% X-Ray inspection to insure rework was successful

9 Troubleshooting Guide

The troubleshooting guide shown as Table 4 lists some common assembly defects and typical causes for each. It is possible that other factors may cause these defects – if none of the recommended solutions resolves the defect, more extensive failure analysis may be required to determine the root cause.

Table 4. Troubleshooting Guide

Defect	Recommended Solutions
Head on Pillow	<ul style="list-style-type: none"> • Check Solder Paste Volumes to ensure that there are no insufficient prints
	<ul style="list-style-type: none"> • Check the temperature gradient across the BGA. It should be 10°C or less, with lower temperature gradients preferred
	<ul style="list-style-type: none"> • Check with the solder paste manufacturer to ensure that the solder paste is designed to minimize head in pillow defects
	<ul style="list-style-type: none"> • Check that the reflow profile meets the paste manufacturer's guidelines. Generally, the time to peak temperature should be less than 6 minutes and the soak should be less than 2 minutes, but these guidelines may vary by paste. Incorrect profiling may exhaust the flux, or may insufficiently activate it.
	<ul style="list-style-type: none"> • Use nitrogen as a reflow environment. Ensure that the oxygen levels are within specification when using nitrogen
	<ul style="list-style-type: none"> • Check the lot number, date code and storage conditions for the component
	<ul style="list-style-type: none"> • Ensure that the maximum recommended bakeout time has not been exceeded.

Table 4. Troubleshooting Guide (continued)

Defect	Recommended Solutions
Solder Shorts or Bridges	• Check solder paste prints for excessive volume or mis-registration
	• Check that the stencil underwiping frequency is adequate and the wiping process is effective
	• Verify placement accuracy and ensure that placement pressure is not excessive
	• Ensure that the printed circuit assemblies do not experience sudden acceleration or deceleration prior to reflow
Opens or Insufficients	• Check Stencil for apertures clogged with solder paste
	• Verify that the stencil apertures and the PCB pads are within the designed specification.
	• Check the temperature gradient across the BGA and ensure that it is 10°C or less, with lower temperature gradients preferred
Voids	• Check to ensure that the reflow profile matches the paste supplier's recommendations
	• Ensure that microvias are filled. If microvia filling does not meet specification, contact the PCB manufacturer.
	• If planar microvoids near the printed circuit board are detected, contact the PCB manufacturer, as these may be signs of a surface finish defect

10 Technical Specifications

10.1 Packaging Information

Table 5 defines the WiLink 8Q FCBGA package specifications.

Table 5. WiLink 8Q FCBGA Package Information

Component ID Code/Number/Name		
Package Type and Name	FCBGA (10 × 10 × 1.17; 0.65 mm)	
Package Marking	Component	TI logo
	Orientation	#A1 / bottom right corner
Package Attributes	Ball count	169
	Ball pitch (mm)	0.65
	Ball diameter / dimensions (mm)	0.40 ± 0.05
	Ball height / substrate standoff (mm)	0.31
	Coplanarity (mm)	0.10 (maximum)
	Package thickness (mm)	1.260 (maximum)
	Maximum footprint (mm × mm)—center to center	10.10 × 10.10
	Interconnect method (WB, TAB, FC)	FC
	Daisy-chain level(if daisy-chain component)	Level 3
	Available shipping media	Tape and reel

Table 6 shows the typical WiLink 8Q FCBGA PCB materials list.

Table 6. WiLink 8Q FCBGA Package Structure and Materials

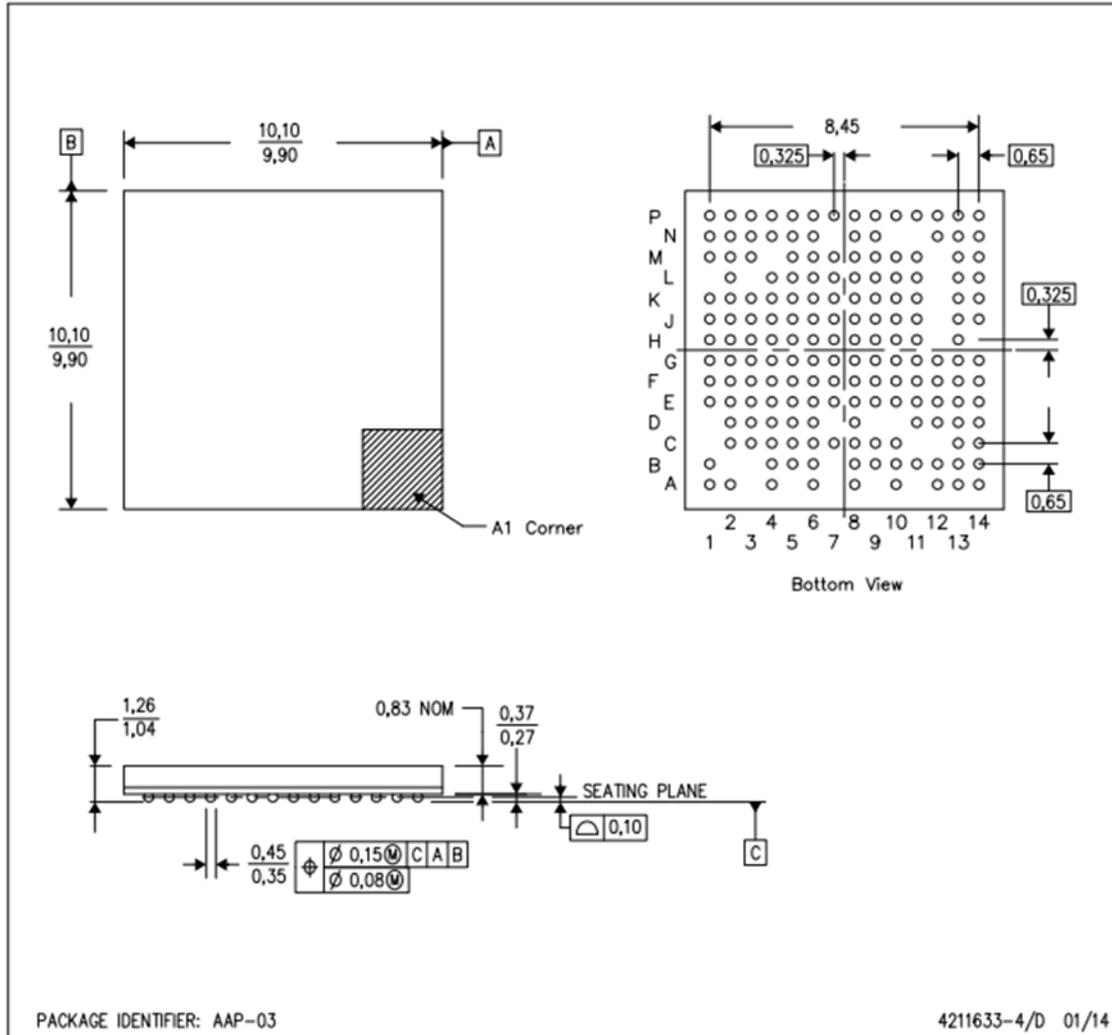
Structural Information	Material
Conductor material	Cu
Die bond pad metallization	AL
Solder ball composition	LF35/SAC305

10.2 Mechanical Data

Figure 15 shows the package drawing.

AAP (S-FCBGA-N169)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y1.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Flip chip application only.
 - D. Pb-free bump and solder ball.

Figure 15. Package Drawing

The following packaging information reflects the most current released data available for the designated package example. For more details, see [Table 7](#).

Table 7. AAP Package Drawing and Dimensions

Description	Min	Nom	Max
Body size (W, mm)	9.900	10.000	10.100
Body size (L, mm)	9.900	10.000	10.100
Overall thickness (t, mm)	1.040	1.170	1.260
Terminal pitch (mm)	—	0.650	—
Ball / Terminal diameter (mm)	0.350	0.400	0.450
Ball height (mm)	0.270	0.320	0.370
Coplanarity at terminal / ball side (mm)	—	—	0.100

11 Summary

Designing highly reliable systems using flip chip BGA packages is possible with a good understanding of the manufacturing process and the impact of each design element on PCB performance.

For reliability, careful attention should be provided for the physical characteristics of the copper lands on the PCB. Matching the land diameter on the PCB to that on the BGA package ensures a robust solder connection.

In addition to properly designing the PCB, the following assembly considerations are necessary:

- Understand the reflow process which best fits your PCB system mounting requirements.
- Follow the provided reflow profile and compare closely to the solder paste manufacturer's recommended reflow profile.

On new PCB designs, conduct appropriate strain and strain rate characterization on the PCB assembly process prior to component-mounting.

Avoid excessive shock and bending of the PC board during assembly, handling, and testing of FCBGAs.

Finally, always follow the directions provided for handling moisture-sensitive devices. Keep the required documentation readily available to avoid potential disruptions associated with moisture-induced problems.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (August 2015) to B Revision	Page
• Removed "Typically between 17 mm and 25 mm in body size, but not limited to" and "Thermally enhanced with a metal, heat-dissipative lid" from Generic Product Description List.....	3
• Changed from Mass: 2.2 to 7.5g to 0.2 to 0.3 g throughout document	3
• Deleted "Solder mask defined (SMD) — The solder mask opening is smaller than the metal pad." under non-solder mask defined (NSMD).	3
• Changed can be exposed "when trace routing is dense" to can be exposed "if not properly dimensioned,"	5
• Removed 2.1.2 Solder-Mask-Defined (SMD) Land	5
• Removed SMD from Solder Mask Type, SMO=0.35, Pad Size=0.45 from Table 1.	5
• Removed BGA arrays and information from PCB routing section	6
• Removed "Routing of 0.6hmm pitch Via Channel™ BGA Arrays Section	6
• Removed from table 2: BGA Array Type=Via-Channel, Via Diameter=20 mil, 18 mil, Via Hole Size=12-10 mil, 10-8 mil, Trace Size=4 mil, 4 mil, Clearance=4 mil, 4 mil, Micro Vias?=No, No	6
• Removed from table 2 on Standard BGA Array Type: Via Diameter=12 mil, Via Hole Size=6 mil, Trace Size=4 mil, Clearance= 4=mil, Micro Vias?=Yes.....	6
• Removed PCB Feature Sizes Section.....	7
• Removed 2.2.4.2 PCB Layer Count for Via Channel™ BGA arrays section and title	7
• Removed Figure 9 Acceptable Solder Paste Alignment and Figure 10 Unacceptable Solder Paste alignment and all references to them	8
• Removed "To simulate a worst-case paste alignment condition, prints were intentionally offset by 100µm (0.004") in both X and Y directions. During the laboratory testing, the offset prints produced satisfactory results, with no solder defects formed. It should be noted that the tested offsets were extreme conditions and, while they can occur in production environments, are generally considered outside of the typical process window for most SMT assemblies of this complexity level." after "and the print should be rejected." in Section 3.3	8
• Changed "If components are removed from their protective storage environment and exposed to ambient environment (≤30°C/60%RH) for more than 72 hours" to 168 hours	9
• Removed Figure 11 Example of X-Ray Image of Intentional Component Placement Offset and Figure 12 Example of X-Ray of Component Centered after Reflow Process and references	10
• Removed section 4.9 Orientation Indicator and Figure 13 Example of Orientation Indicators.....	10
• Added Technical Specifications and Packaging Information sections	20
• Added package drawing	21
• Removed "When designing with Via Channel Array™ technology, escape routing can be accomplished with a 4-layer PCB design and standard 20/10 PTH vias. High Density Interconnect PCB technology is not necessary. By depopulating balls from a full array in strategic locations, the Via Channel™ approach allocates space within the component footprint to allow complete signal routing with standard size traces and vias. This option greatly reduces PCB fabrication costs when compared with typical 0.65mm BGA packages." after ...each design element on PCB performance	22

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