Errata

MSPM0G351x, MSPM0G151x Microcontrollers

ABSTRACT

This document describes the known exceptions to the functional specifications (advisories).

Table of Contents

1 Functional Advisories 1
2 Preprogrammed Software Advisories 2
3 Debug Only Advisories 2
4 Fixed by Compiler Advisories 2
5 Device Nomenclature 2
5.1 Device Symbolization and Revision Identification 2
6 Advisory Descriptions 4
7 Trademarks 14
8 Revision History 14

1 Functional Advisories

Advisories that affect the device operation, function, or parametrics.

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev A	Rev C
ADC_ERR_05	✓	✓
ADC_ERR_06	✓	✓
ADC_ERR_07	✓	✓
ADC_ERR_08	✓	✓
CPU_ERR_01	✓	✓
CPU_ERR_02	✓	✓
FLASH_ERR_01	✓	✓
FLASH_ERR_02	✓	✓
I2C_ERR_05	✓	✓
PMCU_ERR_07	✓	✓
PMCU_ERR_10	✓	
PMCU_ERR_13	✓	✓
SPI_ERR_02	✓	✓
SPI_ERR_04	✓	✓
SPI_ERR_05	✓	✓
SPI_ERR_06	✓	✓
SPI_ERR_07	✓	✓
SRAM_ERR_01	✓	
SYSOSC_ERR_01	✓	✓
SYSOSC_ERR_02	✓	✓
TIMER_ERR_06	✓	✓
UART_ERR_01	✓	✓
UART_ERR_02	✓	✓

Errata Number	Rev A	Rev C
UART_ERR_04	✓	✓
UART_ERR_05	✓	✓
UART_ERR_06	✓	✓
UART_ERR_07	✓	✓
UART_ERR_08	✓	✓

2 Preprogrammed Software Advisories

Advisories that affect factory-programmed software.

✓ The check mark indicates that the issue is present in the specified revision.

3 Debug Only Advisories

Advisories that affect only debug operation.

✓ The check mark indicates that the issue is present in the specified revision.

4 Fixed by Compiler Advisories

Advisories that are resolved by compiler workaround. Refer to each advisory for the IDE and compiler versions with a workaround.

✓ The check mark indicates that the issue is present in the specified revision.

5 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

Support tool naming prefixes:

X: Development-support product that has not yet completed Texas Instruments internal qualification testing.

null: Fully-qualified development-support product.

XMS devices and X development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format.

5.1 Device Symbolization and Revision Identification

The package diagrams below indicate the package symbolization scheme, and Table 5-1 defines the device revision to version ID mapping.

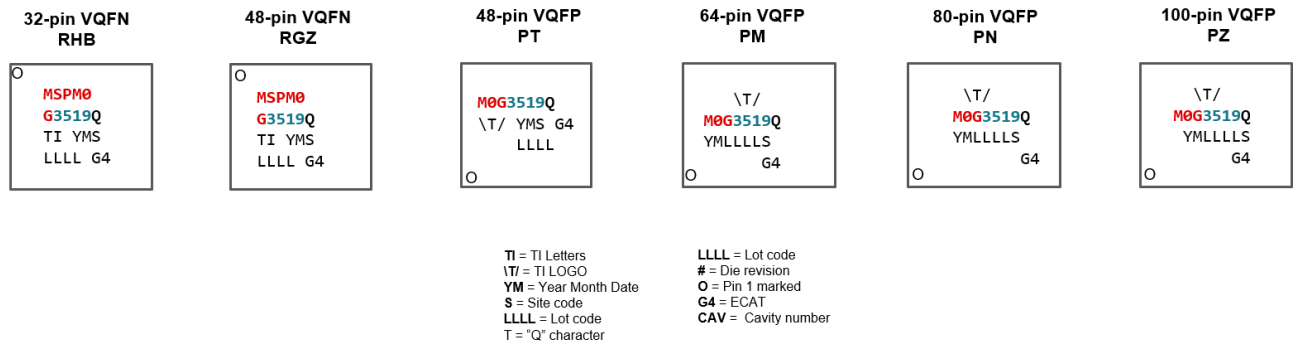

Figure 5-1. Package Symbolization

Table 5-1. Die Revisions

Revision Letter	Version (in the device factory constants memory)
A	1
C	2

The revision letter indicates the product hardware revision. Advisories in this document are marked as applicable or not applicable for a given device based on the revision letter. This letter maps to an integer stored in the memory of the device, which can be used to look up the revision using application software or a connected debug probe.

6 Advisory Descriptions

ADC_ERR_05 *ADC Module*

Category

Functional

Function

HW Event generated before enabling IP, ADC Trigger will stay in queue

Description

When ADC is configured in HW event trigger mode and the trigger is generated before enabling the ADC, the ADC trigger will stay in queue. Once ADC is enabled, it will trigger sampling and conversion.

Workaround

After configuring ADC in HW trigger mode, enable ADC first before giving external trigger.

ADC_ERR_06 *ADC Module*

Category

Functional

Function

ADC Output code jumps degrading DNL/INL specification

Description

The ADC may have errors at a rate as high as 1 in 25M conversions in 12-bit mode. When a conversion error occurs, it will be a maximum +/- 64LSB random jump in the digital output of the ADC without a corresponding change in the ADC input voltage. The magnitude of this jump is larger near major transitions in the bit values of the ADC result (more bits transitioning from 1->0, or 0->1), and largest around midscale (2048 or 0x800). Depending on the application needs the best workaround may vary, but the following workarounds in software are proposed. Selection of the best workaround is left to the judgment of the system designer.

Workaround

Workaround 1: Upon ADC result outside of application threshold (via ADC Window Comparator or software thresholding), trigger or wait for another ADC result before making critical system decisions

Workaround 2: During post-processing, discard ADC values which are sufficiently far from the median or expected value. The expected value should be based on the average of real samples taken in the system, and the threshold for rejection should be based on the magnitude of the measured system noise.

Workaround 3: Use ADC sample averaging to minimize the effect of the results of any single incorrect conversion.

ADC_ERR_07 *ADC Module*

Category

Functional

Function

The conversion underflow flag UVIFG not set as expected under certain sequence

ADC_ERR_07
(continued)

ADC Module

Description

Scenario:
1. PWREN and configured adc in single mode.
2. Enabling ADC and waiting for at least 6usec.
3. Put SC bit high and wait for z number of cycles.
4. Read the busy bit and if busy bit is low, read ADC_SVT_MEMRES0 Register
5. Store the read value in sram

Observation:
1. If Optimization is high and z <11 cycles, UVIFG Flag getting set. Data Read is correct when z=10 since it takes few cycle, but z<10 gives data val =0 because MEMRES is not updated by this time when we are trying to read from MEMRES.
2. If Optimization is high and z >= 11, UVIFG Flag not getting set and data Read is correct
3. If Optimization is 0 and z >= 5, UVIFG Flag not getting set and data Read is correct

Workaround

No workarounds.

ADC_ERR_08

ADC Module

Category

Functional

Function

ADCMEMRES swap is seen when PA15 is toggling

Description

When ADC is configured in below settings:
1. ADC is configured in repeat sequence mode.
2. FIFO is disabled.
Set up condition:
1. ADC can use internal/external channels for which data needs to be converted.
2. PA15 is toggled from TB when IO is configured in input mode or PA15 is generating PWM when IO is configured in output mode.
Observation:
1. When the software is starting the ADC conversion, sometimes MEMRES data is being swapped. Means the data which needs to be in MEMRES0 is coming into MEMRES1, MEMRES1 data is coming into MEMRES2..so on.
Root cause:
The toggling signal on PA15 could affect the conversion clock of the ADC. And the increasing in frequency of conversion clock is making ADC to read out faster before the actual data comes then causes MEMRES 1 reads MEMRES0 sometimes and so on.

Workaround

Avoid input/output toggling signal on PA15.

CPU_ERR_01

CPU Module

Category

Functional

CPU_ERR_01 (continued) — ***CPU Module***

Function

CPU cache content can get corrupted

Description

Cache corruption can occur when switching between accessing Main flash memory, and other memory regions such as NONMAIN or Calibration data areas.

Workaround

Use the following procedure to access areas outside main memory safely:
1. Disable the cache by setting CTL.ICACHE to "0".
2. Perform needed access to memory area.
3. Re-enable cache by setting CTL.ICACHE to "1".

CPU_ERR_02 — ***CPU Module***

Category

Functional

Function

Limitation of disabling prefetch feature for CPUSS

Description

CPU prefetch disable will not take effect if there is a pending flash memory access.

Workaround

Disable prefetch. Then issue a memory access to the shutdown memory (SHUTDNSTORE) in SYSCTL.

FLASH_ERR_01 — ***FLASH Module***

Category

Functional

Function

Access to FACTORY region will lead to hard fault with MCLK is sourced from PLL at 80MHz

Description

Access to FACTORY region when the MCLK is sourcing from PLL at a high frequency(with flash wait state as 2) will trigger a hard fault.

Workaround

Set MCLK at a lower frequency(with flash wait state as 0 or 1) to access FACTORY region.

FLASH_ERR_02 — ***FLASH Module***

Category

Functional

Function

Debug disable in NONMAIN can be re-enable using default password

FLASH_ERR_02 (continued) — ***FLASH Module***

Description

If debug is disabled in NONMAIN configuration, it still can be enabled using default password.

Workaround

1. Set the DEBUGACCESS to Debug Enabled with Password option and provide a unique password in the PWDDEBUGLOCK field. For higher security, it is recommended to have device-unique passwords that are cryptographically random. This would allow debug access with the right 128-bit password but can still allow some debug commands and access to the CFG-AP and SEC-AP.
2. Disable the physical SW Debug Port entirely by disabling SWDP_MODE. This fully prevents any debug access or requests to the device, but may affect Failure Analysis and return flows.

I2C_ERR_05 — ***I2C Module***

Category

Functional

Function

I2C SDA may get stuck to zero if we toggle ACTIVE bit during ongoing transaction

Description

If ACTIVE bit is toggled during an ongoing transfer, its state machine will be reset. However, the SDA and SCL output which is driven by the master will not get reset. There is a situation where SDA is 0 and master has gone into IDLE state, here the master won't be able to move forward from the IDLE state or update the SDA value. Slave's BUSBUSY is set (toggling of the ACTIVE bit is leading to a start being detected on the line) and the BUSBUSY won't be cleared as the master will not be able to drive a STOP to clear it.

Workaround

Do not toggle the ACTIVE bit during an ongoing transaction.

PMCU_ERR_07 — ***PMCU Module***

Category

Functional

Function

NRST<1sec pulse giving wrong rstcause in shutdown mode

Description

The rstcause value is wrong under the following condition. Though the expected rstcause is 0x05. (i) Device is configured for shutdown mode (ii) WFI() is called (iii) Give NRST<1sec pulse to bring device out from shutdown mode

Workaround

No workaround.

PMCU_ERR_10 — ***PMCU Module***

Category

Functional

PMCU_ERR_10 (continued)

PMCU Module

Function

VBOOST might have larger delay under certain operating conditions

Description

VBOOST for analog MUX has large delay at VDD<1.8V, which delays settling time of other modules like HFXT, COMP, SYSOSC(FCL-external R),OPA and GPAMP.

Workaround

Keep VDD>=1.8V and use VBOOST in ONALWAYS mode using GENCLKCFG[23:22]=0x2.

PMCU_ERR_13

PMCU Module

Category

Functional

Function

MCU may get stuck while waking up from STOP2 & STANDBY0 at certain scenario

Description

When there is a pending prefetch access before device transitions to STOP2 & STANDBY0. A pending prefetch access such as a timer has just run to completion and DMA has received the event from the GPIO, in that scenario neither DMA transfer happens nor timer ISR execution takes place as well as CPU gets stuck. This issue arises when WFI instruction is half word aligned, wait state of device is 2 and there is a pending prefetch access before device transitions to LPM.

Workaround

Before going to LPM, customer can disable the prefetch and run some dummy instructions (like shutdown register read or any peripheral read) which doesn't access prefetch so that prefetch can get disabled and doesn't cause the device to hang when waking up from LPM as no prefetch access will be pending.

SPI_ERR_02

SPI Module

Category

Functional

Function

Missing SPI Clock and data bytes after wake-up from low power mode (LPM)

Description

After device wake-up from a low power state, the SPI module may not properly propagate the first few clock cycles and data bits of the first byte sent out.

Workaround

To ensure SPI data integrity after a wakeup, use the following sequence when entering and exiting LPMs:

1.Disable SPI module
2.Wait for Interrupt(WFI)- enter LPM
3.Wake up from LPM (any source).
4.Enable the SPI module.

SPI_ERR_04 *SPI Module*

Category

Functional

Function

IDLE/BUSY status toggle after each frame receive when SPI peripheral is in only receive mode.

Description

In case of SPI peripheral in only receiving mode, the IDLE interrupt and
BUSY status are toggling after each frame receive while SPI is receiving data continuously(SPI_PHASE=1). Here there is no data loaded into peripheral TXFIFO and TXFIFO is empty.

Workaround

Do not use SPI peripheral only receive mode. Set SPI in peripheral simultaneous transmit and receive mode.

SPI_ERR_05 *SPI Module*

Category

Functional

Function

SPI Peripheral Receive Timeout interrupt is setting irrespective of RXFIFO data

Description

When using SPI timeout interrupt, the RXTIMEOUT counter started decrementing from the point that peripheral is stopped receiving SPI clock and setting the RXTIMEOUT interrupt irrespective of data exists in RXFIFO or not, which does not match the description in the TRM: SPI peripheral receive timeout(RTOUT) interrupt is "asserted when the receive FIFO is not empty, and no further data is received in the specified time at CTL1.RXTIMEOUT.

Workaround

Repeat load RXTIMEROUT counter value while receive FIFO is empty, and start timeout counting only when receive FIFO gets any data.

SPI_ERR_06 *SPI Module*

Category

Functional

Function

IDLE/BUSY status does not reflect the correct status of SPI IP when debug halt is asserted

Description

IDLE/BUSY is independent of halt, it is only gating the RXFIFO/TXFIFO writing/reading strobes. So, if controller is sending data, although it's not latched in FIFO but the BUSY is getting set. The POCI line transmits the previously transmitted data on the line during halt

Workaround

Don't use IDLE/BUSY status when SPI IP is halted.

SPI_ERR_07	*SPI Module*
Category	Functional
Function	SPI underflow event may not generate if read/write to TXFIFO happen at the same time for SPI peripheral
Description	TXFIFO for SPI peripheral uses a bus synchronization scheme. While the control signal from BUSCLK domain to SPICLK domain is getting transferred, if read and write pointer points to the same head of FIFO, there is a possibility of data coherence issues. This issue only happens in corner case scenarios, and cause no underflow event being generated.
Workaround	Customer must ensure that TXFIFO on peripheral can never be empty when Controller is addressing the peripheral.

SRAM_ERR_01	*SRAM Module*
Category	Functional
Function	SRAM Parity and ECC function is not supported on Rev A devices
Description	SRAM Parity and ECC function is not supported on Rev A devices. Please do not use SRAM Parity and ECC function on Rev A devices.
Workaround	None.

SYSOSC_ERR_01	*SYSOSC Module*
Category	Functional
Function	MFCLK drift when using SYSOSC FCL together with STOP1 mode
Description	If MFCLK is enabled AND SYSOSC is using the frequency correction loop (FCL) mode AND the STOP1 low power operating mode is used, Then the MFCLK may drift by two cycles when SYSOSC shifts from 4MHz back to 32MHz (either upon exit from STOP1 to RUN mode or upon an asynchronous fast clock request that forces SYSOSC to 32MHz).
Workaround	Use STOP0 mode instead of STOP1 mode. There is no MFCLK drift when STOP0 mode is used. OR Do not use SYSOSC in the FCL mode (leave FCL disabled) when using STOP1.

SYSOSC_ERR_02 *SYSOSC Module*

Category

Functional

Function

MFCLK does not work when Async clock request is received in an LPM where SYSOSC was disabled in FCL mode

Description

MFCLK will not start to toggle in below scenario:
1. FCL mode is enabled and then MFCLK is enabled
2. Enter a low power mode where SYSOSC is disabled (SLEEP2/STOP2/STANDBY0/ STANDBY1).
3. Now async requst is received from some peripherals which use MFCLK as functional clock.
This is happening because on receiving async request, SYSOSC gets enabled and ulpclk becomes 32MHz. But the SYSOSCTRIM FSM does not move from DISABLE state. Due to this, the FCL bases MFCLK is gated off and it does not toggle at all.

Workaround

Avoid using this scenario condition.

TIMER_ERR_06 *TIMA and TIMG Module*

Category

Functional

Function

Writing 0 to CLKEN bit does not disable counter

Description

Writing 0 to the Counter Clock Control Register(CCLKCTL) Clock Enable bit(CLKEN) does not stop the timer.

Workaround

Stop the timer by writing 0 to the Counter Control(CTRCTL) Enable(EN) bit.

UART_ERR_01 *UART Module*

Category

Functional

Function

UART start condition not detected when transitioning to STANDBY1 Mode

Description

After servicing an asynchronous fast clock request that was initiated by a UART transmission while the device was in STANDBY1 mode, the device will return to STANDBY1 mode. If another UART transmission begins during the transition back to STANDBY1 mode, the data is not correctly detected and received by the device.

Workaround

Use STANDBY0 mode or higher low power mode when expecting repeated UART start conditions.

UART_ERR_02 *UART Module*

Category

Functional

Function

UART End of Transmission interrupt not set when only TXE is enabled

Description

UART End Of Transmission (EOT) interrupt does not trigger when the device is set for transmit only (CTL0.TXE = 1, CTL0.RXE = 0). EOT successfully triggers when device is set for transmit and receive (CTL0.TXE = 1, CTL0.RXE = 1)

Workaround

Set both CTL0.TXE and CTL0.RXE bits when utilizing the UART end of transmission interrupt. Note that you do not need to assign a pin as UART receive.

UART_ERR_04 *UART Module*

Category

Functional

Function

Incorrect UART data received with the fast clock request is disabled when clock transitions from SYSOSC to LFOSC

Description

Scenario:
1. LFCLK selected as functional clock for UART
2. Baud rate of 9600 configured with 3x oversampling
3. UART fast clock request has been disabled
If the ULPCLK changes from SYSOSC to LFOSC in the middle of a UART RX transfer, it is observed that one bit is read incorrectly

Workaround

Enable UART fast clock request while using UART in LPM modes.

UART_ERR_05 *UART Module*

Category

Functional

Function

Limitation of debug halt feature in UART module

Description

All Tx FIFO elements are sent out before the communication comes to a halt against the expectation of completing the existing frame and halt.

Workaround

Please ensure data is not written into the TX FIFO after debug halt is asserted.

UART_ERR_06 *UART Module*

Category

Functional

UART_ERR_06 (continued)

UART Module

Function

Unexpected behavior RTOUT/Busy/Async in UART 9-bit mode

Description

UART receive timeout (RTOUT) is not working correctly in multi node scenario, where one UART will act as controller and other UART nodes as peripherals , each peripheral is configured with different address in 9-bit UART mode.
First UART controller communicated with UART peripheral1, by sending peripheral1's address as a first byte and then data, peripheral1 has seen the address match and received the data. Once controller is done with peripheral1, peripheral1 is not setting the RTOUT after the configured timeout period, if controller immediately starts the communication with another UART peripheral (peripheral2) which is configured with different address on the bus. The peripheral1 RTOUT counter is resetting while communication ongoing with peripheral2 and peripheral1 setting it's RTOUT only after UART controller is completed the communication with peripheral2 .
Similar behavior observed with BUSY and Async request. Busy and Async request is setting even if address does not match while controller communicating with other peripheral on the bus.

Workaround

Do not use RTOUT/ BUSY /Async clock request behavior in multi node UART communication where single controller is tied to multiple peripherals.

UART_ERR_07

UART Module

Category

Functional

Function

RTOUT counter not counting as per expectation in IDLE LINE MODE

Description

In IDLE LINE MODE in UART, RTOUT counter gets stuck at even when the line is IDLE and FIFO has some elements. This means that RTOUT interrupts will not work in IDLE LINE MODE.
In case of an Address Mismatch, RTOUT counter is reloaded when it sees toggles on the Rx line.
In case of a multi-responder scenario this could lead to an indefinite delay in getting an RTOUT event when communication is happening between the commander and some other responder.

Workaround

Do not enable RTOUT feature when UART module is used either in IDLELINE mode/ multi-node UART application.

UART_ERR_08

UART Module

Category

Functional

Function

STAT BUSY does not represent the correct status of UART module

UART_ERR_08
(continued) ***UART Module***

Description

STAT BUSY is staying high even if UART module is disabled and there is data available in TXFIFO.

Workaround

Poll TXFIFO status and the CTL0.ENABLE register bit to identify BUSY status.

7 Trademarks

All trademarks are the property of their respective owners.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 1, 2024 to March 30, 2025 (from Revision * (November 2024) to Revision A (March 2025)) **Page**

- Added ADC_ERR_07, ADC_ERR_08, CPU_ERR_02, FLASH_ERR_02, PMCU_ERR_13, SPI_ERR_06, SPI_ERR_07, UART_ERR_04, UART_ERR_05, UART_ERR_06, UART_ERR_07 and UART_ERR_08. 1
- Removed ADC_ERR_04, ADC_ERR_05, PMCU_ERR_04, PMCU_ERR_05, PMCU_ERR_06, and UART_ERR_01; Added ADC_ERR_06, I2C_ERR_03, and PMCU_ERR_07 1
- ADC_ERR_06 Description was updated 4
- ADC_ERR_06 Workaround was updated 4
- ADC_ERR_07 Description was updated 4
- ADC_ERR_07 Workaround was updated 4
- ADC_ERR_08 Category was updated 5
- ADC_ERR_08 Module was updated 5
- ADC_ERR_08 Function was updated 5
- ADC_ERR_08 Description was updated 5
- ADC_ERR_08 Workaround was updated 5
- CPU_ERR_02 Category was updated 6
- CPU_ERR_02 Module was updated 6
- CPU_ERR_02 Function was updated 6
- CPU_ERR_02 Description was updated 6
- CPU_ERR_02 Workaround was updated 6
- FLASH_ERR_02 Category was updated 6
- FLASH_ERR_02 Module was updated 6
- FLASH_ERR_02 Function was updated 6
- FLASH_ERR_02 Description was updated 6
- FLASH_ERR_02 Workaround was updated 6
- PMCU_ERR_13 Category was updated 8
- PMCU_ERR_13 Module was updated 8
- PMCU_ERR_13 Function was updated 8
- PMCU_ERR_13 Workaround was updated 8
- PMCU_ERR_13 Description was updated 8
- SPI_ERR_04 Description was updated 9
- SPI_ERR_04 Workaround was updated 9
- SPI_ERR_06 Category was updated 9
- SPI_ERR_06 Module was updated 9
- SPI_ERR_06 Function was updated 9
- SPI_ERR_06 Workaround was updated 9
- SPI_ERR_06 Description was updated 9
- SPI_ERR_07 Category was updated 10

- SPI_ERR_07 Module was updated..... 10
- SPI_ERR_07 Function was updated..... 10
- SPI_ERR_07 Description was updated..... 10
- SPI_ERR_07 Workaround was updated..... 10
- UART_ERR_04 Category was updated..... 12
- UART_ERR_04 Module was updated..... 12
- UART_ERR_04 Function was updated..... 12
- UART_ERR_04 Description was updated..... 12
- UART_ERR_04 Workaround was updated..... 12
- UART_ERR_05 Category was updated..... 12
- UART_ERR_05 Module was updated..... 12
- UART_ERR_05 Function was updated..... 12
- UART_ERR_05 Description was updated..... 12
- UART_ERR_05 Workaround was updated..... 12
- UART_ERR_06 Category was updated..... 12
- UART_ERR_06 Module was updated..... 12
- UART_ERR_06 Function was updated..... 12
- UART_ERR_06 Workaround was updated..... 12
- UART_ERR_06 Description was updated..... 12
- UART_ERR_07 Category was updated..... 13
- UART_ERR_07 Module was updated..... 13
- UART_ERR_07 Function was updated..... 13
- UART_ERR_07 Workaround was updated..... 13
- UART_ERR_07 Description was updated..... 13
- UART_ERR_08 Category was updated..... 13
- UART_ERR_08 Module was updated..... 13
- UART_ERR_08 Function was updated..... 13
- UART_ERR_08 Description was updated..... 13
- UART_ERR_08 Workaround was updated..... 13

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265