WHITE PAPER

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Getting the most out of a high-resolution timer

Introduction

In microcontroller (MCU) systems, a high resolution timer uses high frequency timer clocks, usually much high than the MCU operating frequency, to generate higher resolution timer ticks in the order of a few nanoseconds or even a few hundred picoseconds. This provides finer granularity in timing control, such as timer PWM duty cycle resolution and timer input capture resolution, which is beneficial in applications like LED lighting, inverters/converters, digital power, motor control and other high accuracy digital control applications.

On TI's ultra-low-power MSP430™ MCUs, the 16-bit Timer_D supports high-resolution mode by generating timer clocks up to 256 MHz or 4 ns resolution. Applications like PWM DAC, capacitive touch sensing, LED lighting and other general purpose digital control applications benefit from high resolution timer functionality to address traditionally accepted implementation limitations.

This paper will discuss PWM DAC application, including the parameters affecting effective PWM DAC resolution and how Timer_D high resolution mode enables achieving higher D/A resolution.

PWM DAC application

A digital-to-analog converter (DAC) generates an analog output that is proportional to its digital input. Using a PWM signal followed by a low pass filter is an easy way to achieve DAC functionality and is referred to as PWM DAC. PWM DACs fit well into systems that require DAC functionality, but at a lower cost than high end MCUs with integrated DACs, or external high-accuracy stand-alone DACs. The PWM DAC implementation is not new, but performance limitations have historically confined its use to low-resolution, low-bandwidth applications. We will discuss the known limitations of PWM DAC designs and how high resolution timers (such as Timer_D on MSP430 MCUs) enable higher effective PWM DAC resolution.

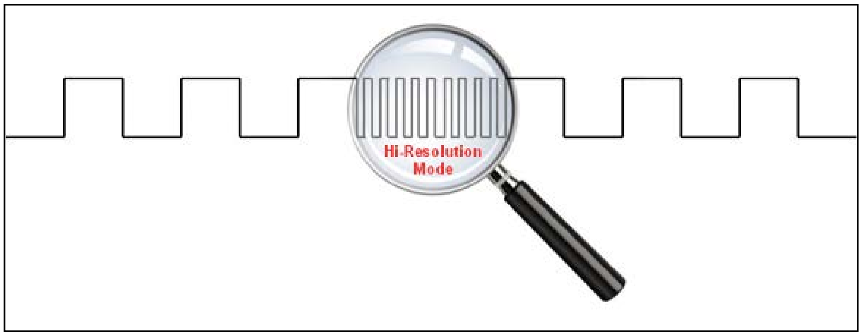

Figure 1: High resolution timers provide finer granularity in timing control.

The following sections present the parameters that influence the effective PWM DAC resolution and shows the importance of selecting the optimum PWM signal frequency for achieving the best effective DAC resolution.

PWM DAC duty cycle resolution

A PWM signal is defined as a digital signal with a fixed frequency and varying duty cycle (represented by the ratio of ON time to period). And, for a given timer clock frequency, the PWM duty cycle resolution is represented as the maximum number of PWM duty cycle steps that can be packed in a PWM period. The DAC resolution is defined as the smallest analog increment possible with the D/A converter which corresponds to one converter digital code change.

In PWM DAC implementations, each PWM duty cycle value corresponds to an average analog voltage level. Therefore, PWM DAC duty cycle resolution is referred to as the smallest increment in the PWM duty cycle, which corresponds to the smallest analog increment of the PWM DAC. For example, a 1 MHz timer that generates a 125 kHz PWM signal has 8 duty cycle steps. And, a PWM DAC using this PWM signal can generate 2^3 analog levels (corresponding to the 8 PWM duty cycle steps), thus yielding a PWM DAC duty cycle resolution of 3 bits. Note this is not the same as effective PWM DAC resolution, which will be discussed later in this paper.

For a given timer clock frequency, decreasing the PWM signal frequency increases the PWM DAC duty cycle resolution and in turn, the overall PWM DAC resolution. Another approach to achieve the same is to increase the timer clock frequency itself by using a high-resolution timer; we will get to that after discussing the known PWM DAC design limitations. So far we've observed that decreasing PWM signal frequency will increase PWM DAC duty cycle resolution.

Analog filter selection and harmonic ripple in PWM DAC output

In this section, we will discuss why we can't just decrease PWM signal frequency in PWM DAC applications. The key to PWM DAC implementation is selecting the right analog low pass filter that follows the PWM signal to generate corresponding analog levels. In order to generate appropriate analog voltages based on the PWM duty cycle, the low pass filter should filter out the PWM signal frequency (or the carrier frequency in this case) and let only the analog signal bandwidth pass through. Increased filter orders give better frequency response with faster roll-off rates. See figure 2 below. However, by increasing filter orders, the cost, complexity, and phase delay in the system also increases; keeping design cost and complexity in mind, selecting a lower order low pass filter (in this case, first or second order LPFs) is important and this works well if the PWM signal frequency that needs to be filtered out is increased.

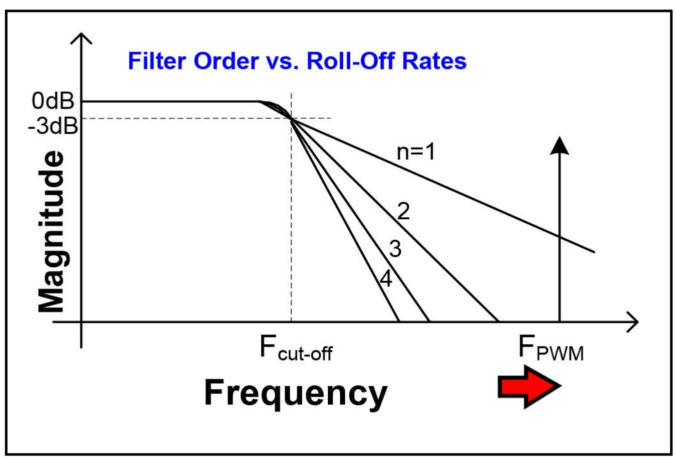

Figure 2: Low pass filter response – filter order vs. roll-off rates

Another important parameter to consider is the unfiltered harmonics (integer multiples of the fundamental frequency, which in this case is the PWM signal frequency) that cause ripple on the PWM DAC low pass filter output. This parameter affects the total uncertainty at output and in turn, the effective PWM DAC resolution. See figure 3 below. As the fundamental harmonic frequency gets closer to the filter cutoff frequency, the harmonic ripple amplitude is higher. Therefore, increasing the PWM signal frequency in this case will decrease the harmonic ripple amplitude at the PWM DAC output (even when a lower order filter is used).

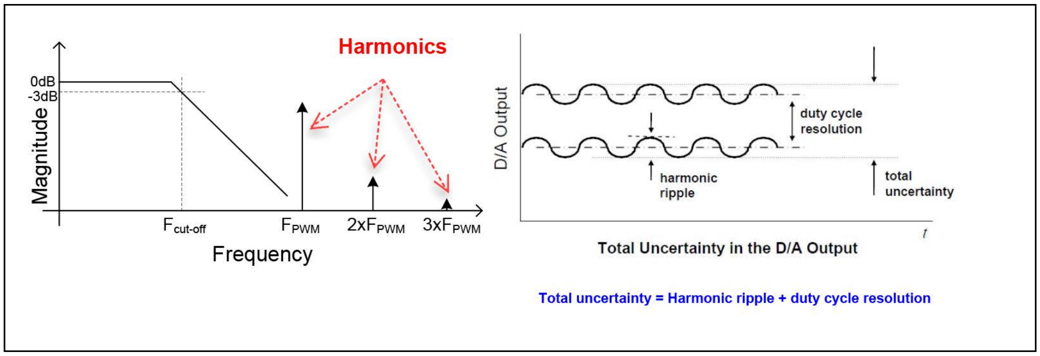

Figure 3: Harmonics and total uncertainty at PWM DAC output.

Effective PWM DAC resolution using Timer_D hi-resolution mode

The total uncertainty at the PWM DAC output reflects the "effective" PWM DAC resolution and is influenced by both the PWM duty cycle resolution and the peak-to-peak harmonic ripple seen at the filter output. So far we understand that these two factors require the PWM signal frequency to be moved in the opposite direction and an optimal PWM signal frequency needs to be chosen such that the total uncertainty of the DAC output is the smallest.

Figure 4 below shows curves of effective PWM DAC resolution (considering a second order RC filter with 20 kHz signal bandwidth) swept across various PWM signal frequencies, using different Timer_D clock frequencies. Those frequencies include 16MHz, 25 MHz in normal resolution mode, and 128 MHz, 256 MHz in high resolution mode. At lower PWM signal frequencies, the effective PWM DAC resolution is affected by the ripple uncertainty and at higher PWM signal frequencies, the resolution is affected by the PWM duty-cycle resolution.

For details regarding simulation and experimental analysis of the effective PWM DAC resolution for various low pass filter designs, refer to PWM DAC Using MSP430 High-Resolution Timer.

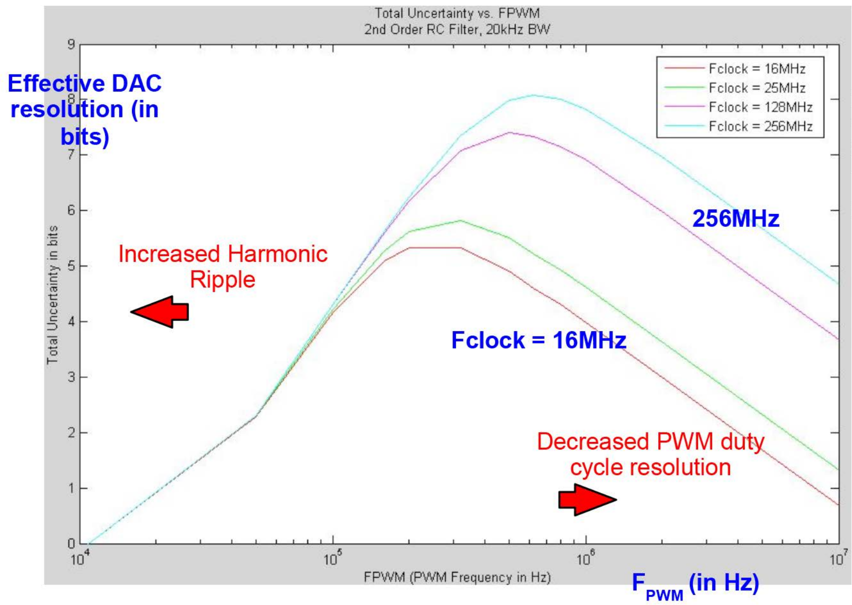

Figure 4: Effective PWM DAC Resolution vs. PWM signal frequency for different timer clock frequencies, considering a 2nd order RC filter with 20kHz bandwidth.

For a given timer clock frequency (Fclock), the optimum PWM signal frequency (f_{PWM}) is where the DAC resolution curve peaks. But the interesting thing to note is that for a specific analog filter, the high resolution timer clock frequencies (Fclock = 128 MHz, 256 MHz),–yield increased effective PWM DAC resolution (up to 3-bits in this example).

Conclusion

In summary, the Timer_D hi-resolution mode on ultra-low power MSP430F51xx MCUs enables PWM DAC designs to achieve increased D/A resolution. Using the PWM DAC with Timer_D hi-resolution mode can essentially be a cost effective solution compared to selecting MCUs with an integrated DAC module or using external DACs that offer the same or higher resolution, if the effective resolution achieved meets the system application requirements.

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