

ISOM8110 Single-Channel Opto-Emulator with Analog Transistor Output Evaluation Module

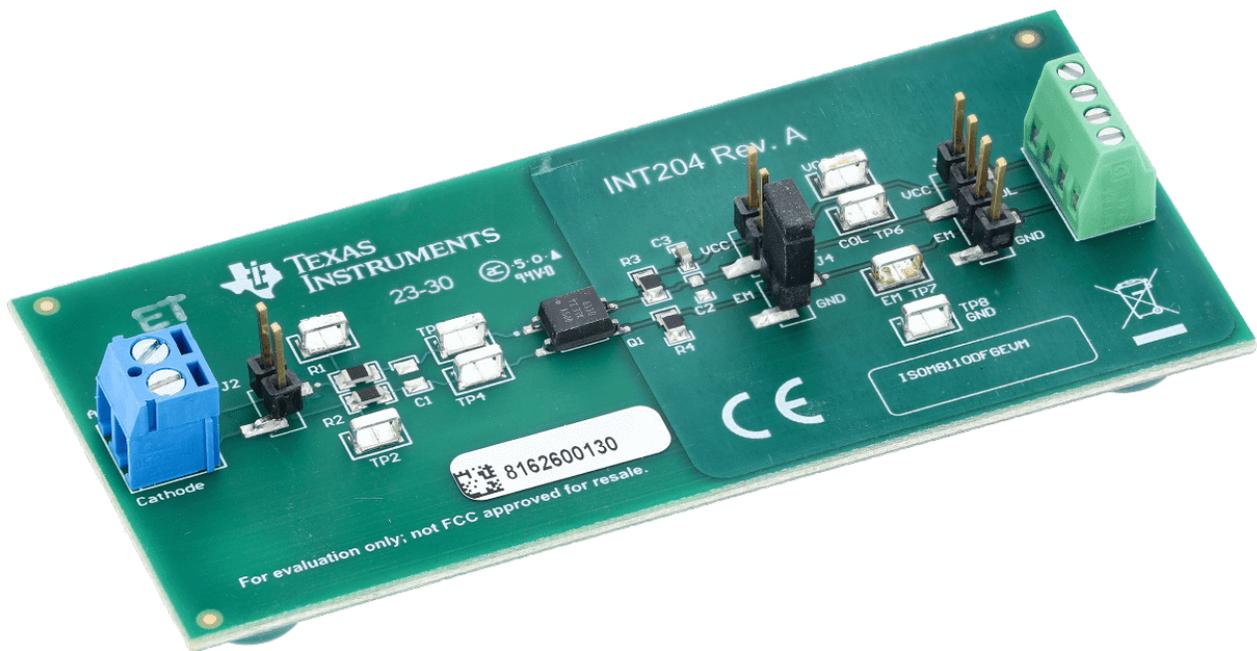


Description

The **ISOM8110** opto-emulator offers significant reliability and performance advantages compared to optocouplers, including high bandwidth, low turn-off delay, low power consumption, wider temperature ranges, tight CTR and process controls resulting in small part-to-part skew. Since there is no aging effect or temperature variation to compensate for, the emulated diode-input stage consumes less power than optocouplers.

Features

- Platform for complete evaluation of the **ISOM8110DFG**
- Test points and jumper options
- Passives and footprints for basic modifications included
- Drop-in upgradable and pin-compatible for popular phototransistor optocouplers
- 1 channel diode-emulator input
- Current transfer ratio (CTR): at $I_F = 5\text{mA}$, $V_{CE} = 5\text{V}$ – ISOM8110: 100% to 155%
- High collector-emitter voltage: $V_{CEO}(\text{max}) = 80\text{V}$
- Robust isolation barrier



ISOM8110DFGEVM

1 Evaluation Module Overview

1.1 Introduction

The [ISOM8110DFGEVM](#) user's guide describes the functionality of the [ISOM8110](#) Single-Channel Opto-Emulator with Analog Transistor Output Evaluation Module (EVM). The ISOM8110DFGEVM supports evaluation of TI's ISOM8110 Opto-Emulator in a 4-pin DFG SOIC package. This user's guide describes EVM operation with respect to the ISOM8110 under 5V operation. The EVM can be reconfigured for evaluation with a larger input signal or other applications by changing the EVM configuration and component values. The user's guide also covers the channel configuration of the ISOM8110, EVM schematic, and typical setup.

CAUTION

This evaluation module is made available for isolator parameter performance evaluation only and is not intended for isolation voltage testing. To prevent damage to the EVM, any voltage applied as a supply or digital input/output must be maintained within the recommended operating conditions of the device.

1.2 Kit Contents

This evaluation module contains one PCB evaluation board containing one ISOM8110DFG device. The major components of the ISOM8110 evaluation board are:

- ISOM8110DFG Opto-Emulator
- Multiple on-board test points

To demonstrate functionality of the ISOM8110DFG, TI recommends the following (not included):

- Oscilloscope
- Signal Generator

1.3 Specification

The [ISOM8110](#) device is capable of being pin-compatible and drop-in replaceable with many opto-coupler devices with transistor outputs. Opto-emulators offer significant reliability and performance advantages compared to traditional opto-couplers, including tighter current transfer ratio (CTR), low input current, and wider temperature ranges.

The ISOM8110 Opto-Emulator replicates the characteristics of traditional opto-couplers without the drawbacks of aging and thermal drift by using an input-diode emulator and output stage separated by a silicon oxide (SiO₂) insulation barrier. When used with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents from interfering with or damaging sensitive circuitry.

1.4 Device Information

The [ISOM8110DFGEVM](#) contains one ISOM8110 and all other passive components required for operation. The various components included in the evaluation module directly control the operation and functionality of the ISOM8110. If necessary, then components can be removed, added, or replaced to modify the behavior of the ISOM8110 accordingly for any given application.

2 Hardware

2.1 EVM Setup and Operation

Basic EVM Setup

This section describes the setup and operation of the EVM for parameter performance evaluation. Figure 2-1 shows a typical test configuration of the ISOM8110 Opto-Emulator EVM using a current source.

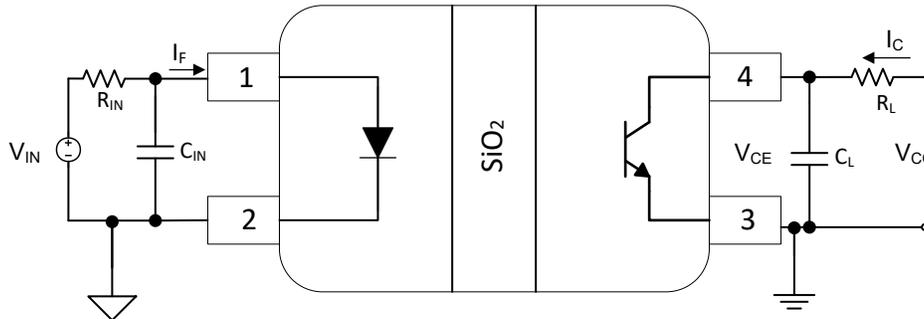


Figure 2-1. Basic EVM Operation

ISOM8110DFGEVM has *do not populate* (DNP) footprints for components which can be populated to apply different test conditions to the device. Section 2.1 lists and describes possible test configurations that can be achieved by modifying different components on the EVM.

Table 2-1. Component Configurations

Component	Description
R1	R1 is sized for 5V operation. If a larger supply is needed, then select a resistor that provides the proper I_F current to the anode.
J3	Shunt J3 to use the output as a high side output (emitter pin). Never shunt J3 and J4 at the same time.
J4	Shunt J4 to use the output as a low side output (collector pin). Never shunt J3 and J4 at the same time.
C1, C2	C1 and C2 can be used to add capacitance to the input diode or collector output, respectively.

2.2 Pin Configuration of the ISOM8110 Single-Channel Opto-Emulator with Analog Transistor Output

Figure 2-2 shows the ISOM8110 Single-Channel Opto-Emulator with Analog Transistor Output pin configuration.

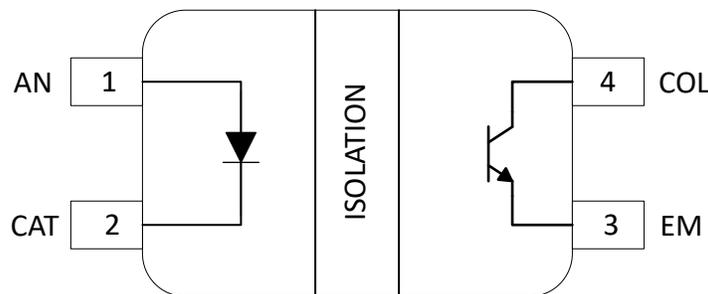


Figure 2-2. ISOM8110 Single-Channel Opto-Emulator with Analog Transistor Output Pin Configuration

3 Hardware Design Files

3.1 Schematics

The ISOM8110DFGEVM has additional footprints that gives the user flexibility to test a variety of common applications.

Other positions on the board can be modified as well. For example, R1 can be changed to accommodate different current requirements, and C2 can be added to test the device with resistive or capacitive loading. See ISOM8110DFGEVM for the EVM schematic and see [Table 2-1](#) for more information on alternate EVM configurations.

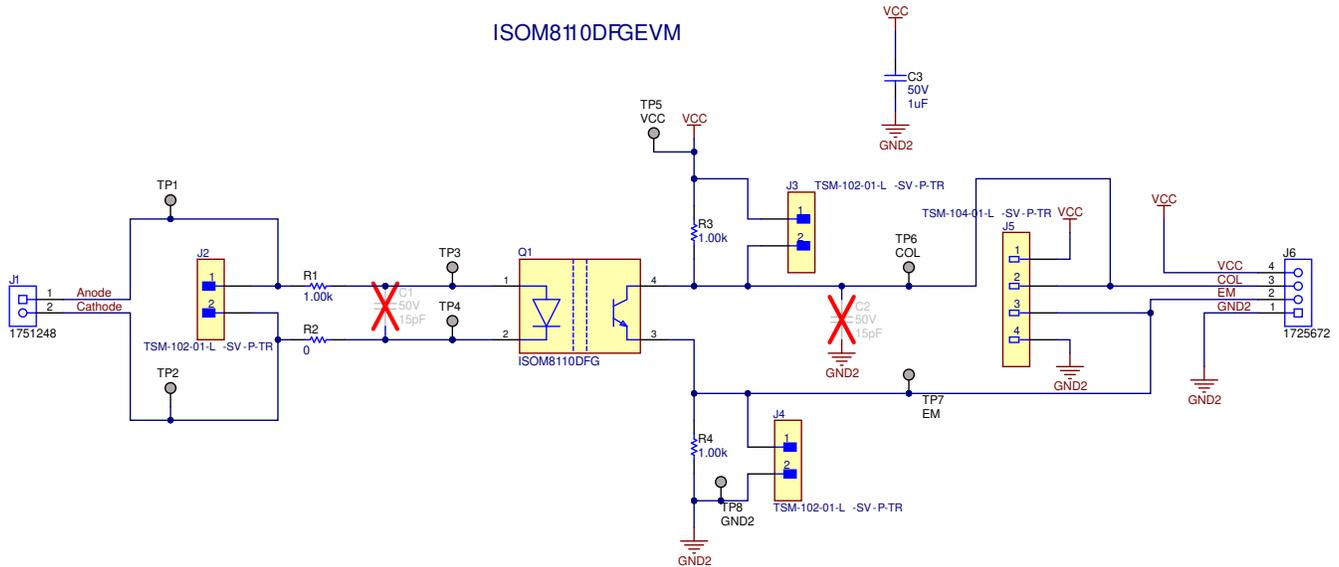


Figure 3-1. ISOM8110DFGEVM Schematic

3.2 PCB Layout and 3D Diagram

Figure 3-2 and Figure 3-3 show the printed-circuit board (PCB) layout top and bottom, respectively, and Figure 3-4 shows a 3D diagram of the EVM PCB.

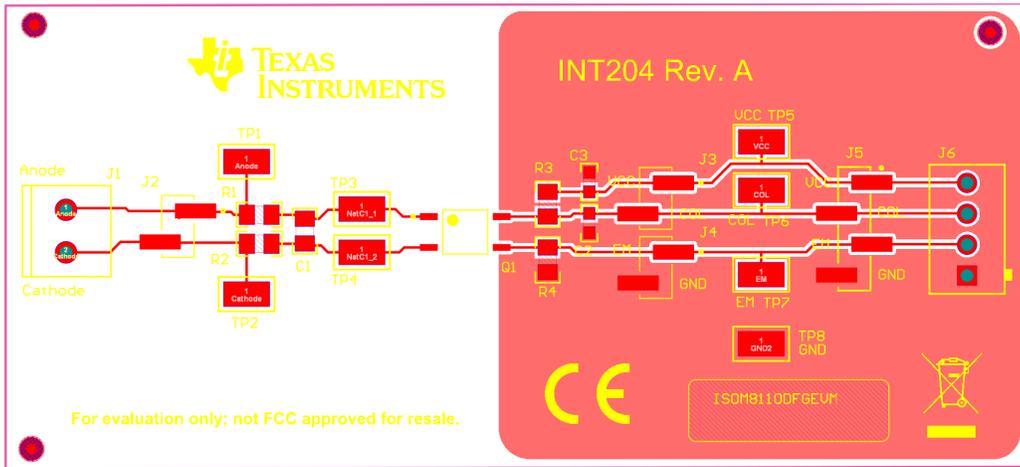


Figure 3-2. ISOM8110DFGEVM PCB Layout - Top

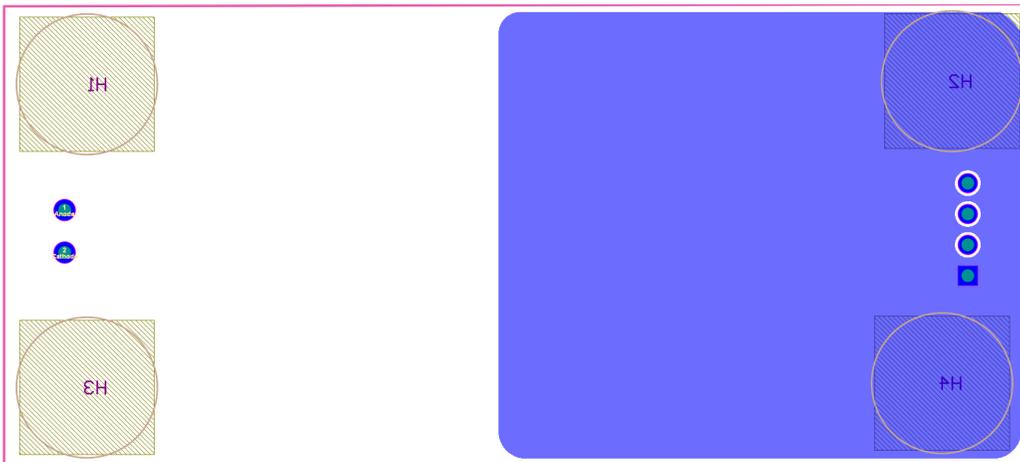


Figure 3-3. ISOM8110DFGEVM PCB Layout - Bottom

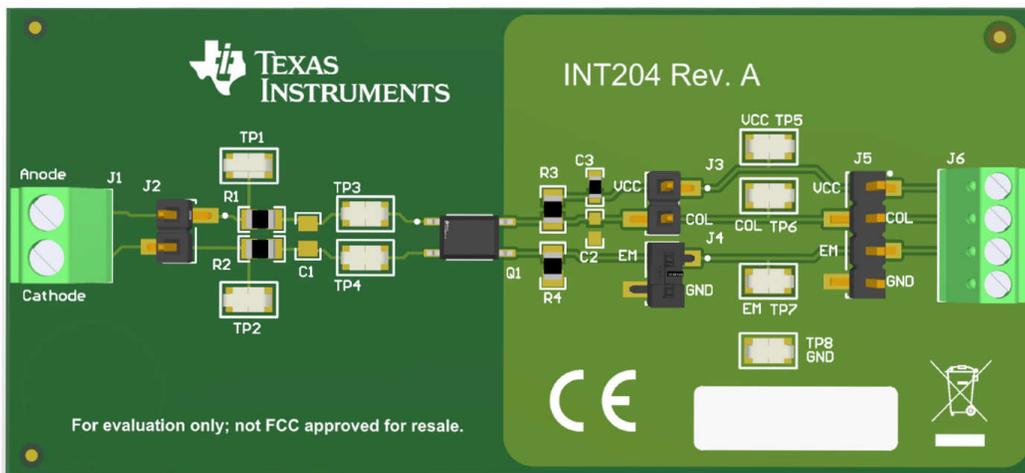


Figure 3-4. ISOM8110DFGEVM PCB 3D Diagram

3.3 Bill of Materials

Table 3-1 lists the bill of materials (BOM) for the ISOM8110DFGEVM.

Table 3-1. Bill of Materials

Item #	Designator	Manufacturer	Description
1	C3	TDK	CAP, CERM, 1uF, 50V, +/- 10%, X5R, 0603
2	H1, H2, H3, H4	3M	Bumpon, Hemisphere, 0.44 X 0.20, Clear
3	J1	Phoenix Contact	Conn Term Block, 2POS, 3.5mm, TH
4	J2, J3, J4	Samtec	Connector Header Surface Mount 2 position 0.100" (2.54mm)
5	J5	Samtec	Connector Header Surface Mount 4 position 0.100" (2.54mm)
6	J6	Phoenix Contact	Terminal Block, 4x1, 2.54mm, Green, TH
7	Q1	Texas Instruments	3.75-kVRMS, Single-Channel Opto-Emulator with Transistor Output
8	R1, R3, R4	Panasonic	RES, 1.00 k, 1%, 0.25 W, 0805
9	R2	Yageo America	RES, 0, 5%, 0.125 W, 0805
10	SH-J1	Samtec	Shunt, 100mil, Gold plated, Black
11	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	Keystone	Test Point, Miniature, SMT
12	C1	Yageo America	CAP, CERM, 15pF, 50V, +/- 5%, C0G/NP0, 0805
13	C2	MuRata	CAP, CERM, 15pF, 50V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603

4 Additional Information

Trademarks

All trademarks are the property of their respective owners.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated