

ADC08xx0 Evaluation Module

This user's guide describes the function and use of the ADC08xx0 evaluation module (EVM). Included in this document are a quick-start guide, instructions for optimizing evaluation results, jumper and connector descriptions, software description, and alternate hardware configurations.

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1 Overview

The ADC08xx0EVM is an evaluation module (EVM) designed to evaluate the ADC08xx0. The EVM provides simple and minimal external components to minimize system cost and power consumption.

The following features apply to this EVM:

- 8-bit, low-cost, high-speed, CMOS interface ADC08xx0
- External clock for sample clocking with an option to add an onboard crystal oscillator
- Option to provide separate clocks to ADC and FPGA
- TPS7A47 user-programmable RF low-dropout (LDO) voltage regulator
- CDCV304 high-performance, low-skew, PCI_X-compliant clock buffer
- SN74AVC16244 *Dynamic Output Control*, low-noise 16-bit output buffer

The ADC08xx0EVM is designed to work seamlessly with the TSW1400EVM, TI's CMOS and LVDS pattern generator and data-capture board, through the *High-Speed Data Converter Pro* Graphical User Interface (HSDC Pro GUI) software tool for high-speed data converter evaluation.

1.1 Required Hardware

The following equipment is **included** in the EVM evaluation kit:

- ADC08xx0EVM
- Standard banana jack power supply cables

The following list of equipment are items that are **not included** in the EVM evaluation kit but are items required for evaluation of this product in order to achieve the best performance:

- *TSW1400EVM Data Capture Board*, 5-V DC cable connector, and mini-USB cable
- Computer running Microsoft® Windows® 8, Windows 7, or Windows XP
- One low-noise signal generator. Recommendations:
 - RF generator, > +17 dBm, < -40 dBc harmonics, < 500 fsec jitter 20 kHz–20 MHz, 1-MHz to 2-GHz frequency range
 - Examples: TSW2170EVM, HP HP8644B, Rohde & Schwarz SMA100A
- DC power supply. Recommendations:
 - DC Power Supply, 0-6 VDC, > 3 A
 - Examples: Agilent E363A or equivalent
- Bandpass filter for desired analog input. Recommendations:
 - Filter, ≥ 60-dB harmonic attenuation, ≤ 5% bandwidth, > +18-dBm power, < 5-dB insertion loss
 - Examples: Trilithic 5VH-series Tunable BPF, K&L BT-series Tunable BPF, TTE KC6 or KC7-series Fixed BPF
- Signal path cables, SMA or BNC with BNC-to-SMA adapters

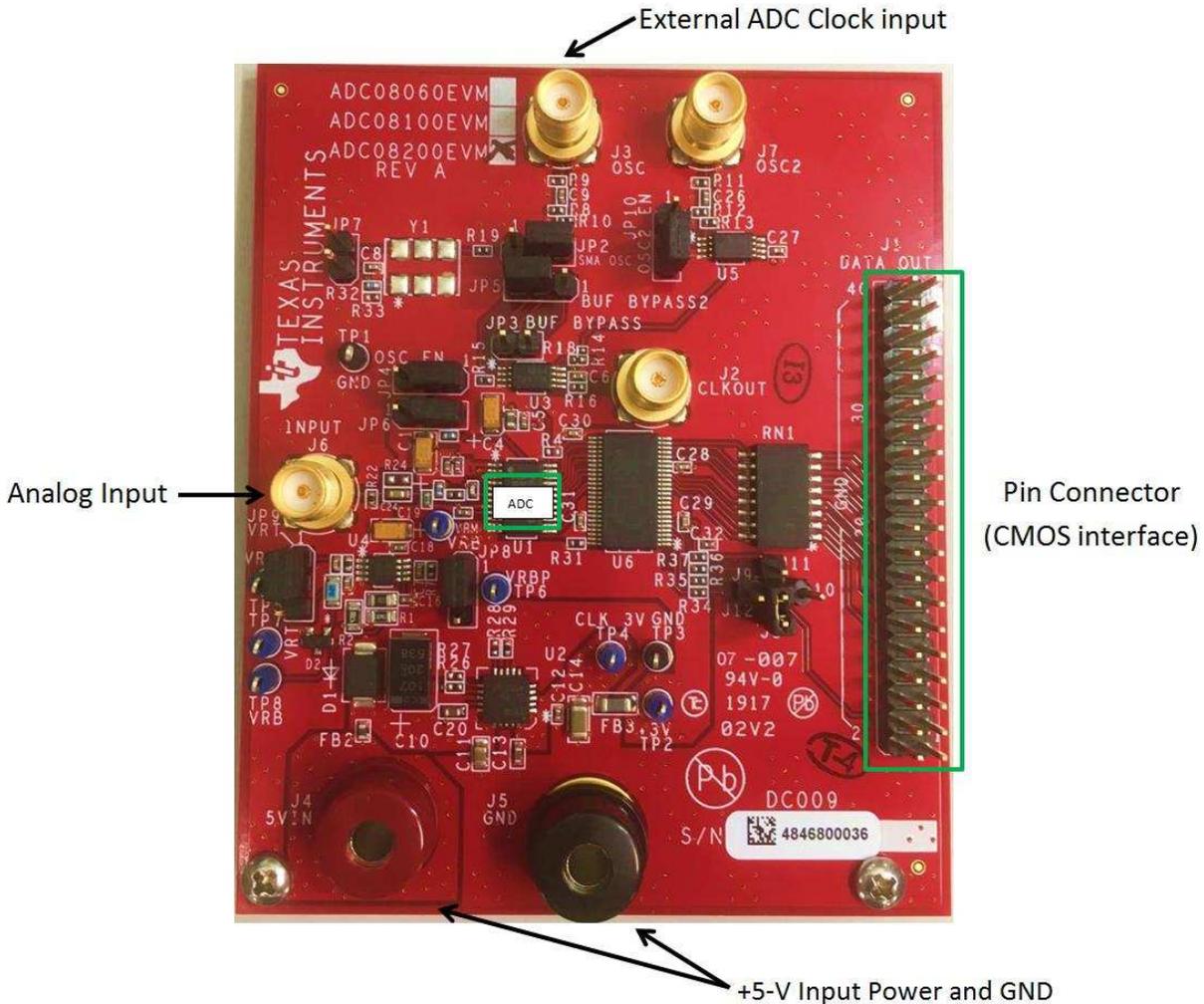
1.2 Required Software

The following software is required to operate the TSW1400EVM and is available online. See [References, Section 1.4](#) for links.

- High-Speed Data Converter Pro software

1.3 Evaluation Board Feature Identification Summary

The EVM features are labeled in Figure 1.



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Figure 1. EVM Feature Locations

1.4 References

- ADC08060 data sheet ([SNAS120](#)), available at www.ti.com/product/ADC08060
- ADC08100 data sheet ([SNAS060](#)), available at www.ti.com/product/ADC08100
- ADC08200 data sheet ([SNAS136](#)), available at www.ti.com/product/ADC08200
- TSW1400EVM User's Guide ([SLWU079](#)), available at www.ti.com/tool/TSW1400EVM
- High-Speed Data Converter Pro software ([SLWC107](#)) and User's Guide ([SLWU087](#)), available at www.ti.com/tool/dataconverterpro-sw

NOTE: Schematics, layout, and BOM are available on the [ADC08060EVM](#) product page on www.ti.com.

2 Quick-Start Guide

This section guides the user through the EVM test procedure to obtain a valid data capture from the ADC08xx0EVM using the TSW1400EVM capture card. This should be the starting point for all evaluations.

2.1 Software Installation

The proper software must be installed before beginning evaluation. See [Section 1.2](#) for a list of the required software. The [References](#) section of this document contains links to find the software on the TI website.

Important: The software must be installed before connecting the ADC08xx0EVM and TSW1400EVM to the computer for the first time.

2.1.1 High-Speed Data Converter Pro GUI Installation

The *High-Speed Data Converter Pro* (HSDC Pro) is used to control the TSW1400EVM and analyze the captured data. See the HSDC Pro user's guide ([SLWU087](#)) for more information.

1. Download HSDC Pro from the TI website. The [References](#) section of this document contains the link to find the software on the TI website.
2. Extract the files from the zip file.
3. Run *setup.exe* and follow the installation prompts.

2.2 Hardware Setup Procedure

A typical test setup using the ADC08xx0EVM and TSW1400EVM is shown in Figure 2. This is the test setup used for the quick-start procedure. The rest of this section describes the hardware setup steps.

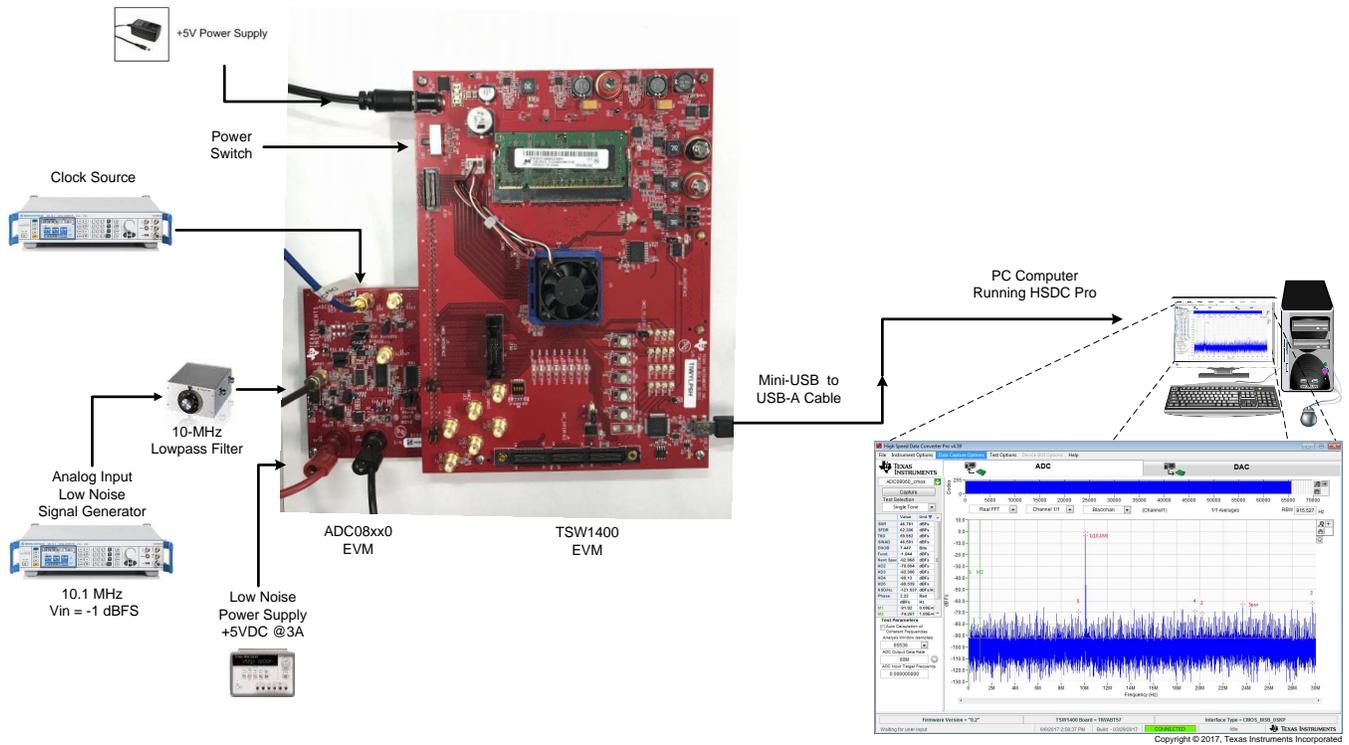


Figure 2. Quick-Start Test Setup

2.2.1 TSW1400EVM Setup

First, set up the TSW1400EVM using the following steps:

1. Connect the ADC08xx0EVM to the TSW1400EVM connecting pin 1 of the CMOS_INTERFACE (J1) to pin 1 of ADC08xx0EVM output data (J1).
2. Connect the power cable to connector J12 (5 V IN) to the TSW1400EVM.
3. Connect the mini-USB cable to the USB connector (J5).
4. Turn on the power supply. Flip the power switch (SW7) to the ON position. The board should draw around 0.5 A after power up. This will increase to around 1.7 A when loaded with firmware.

2.2.2 ADC08060EVM Setup

Next, setup the ADC08060EVM using the following:

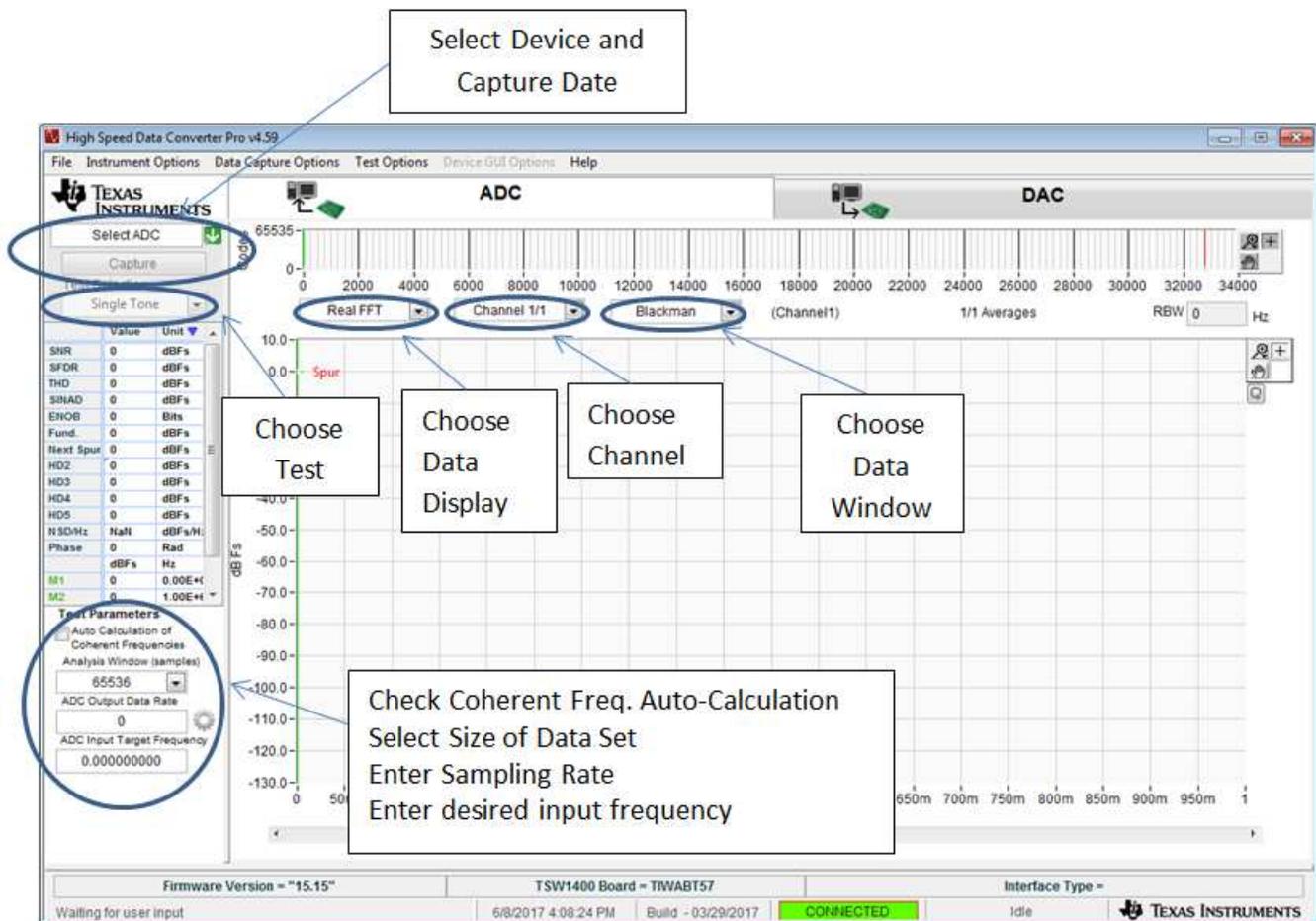
1. Connect the banana jack power-supply cables to the EVM. Connect the red wire to 5 VDC ± 0.1 VDC of a power supply rated for at least 3 A to connector J4. Connect the black wire to J5 (GND) of the power supply.
2. Turn on the power supply. The power draw should be around 0.220 A after the clock is supplied.
3. Provide a 60-MHz, -1 -dBm clock signal to J3.
4. Set the analog input signal generator for 10.1 MHz, -1 dB from full scale.
5. Place a 10-MHz bandpass filter at the output of the analog signal generator to remove noise and harmonics from the signal generator.
6. Connect the analog input signal generator to the EVM through SMA connector INPUT (J6) and provide a 10.1-MHz signal.

2.3 Software Setup Procedure

The software can be opened and configured once the hardware is properly set up.

2.3.1 HSDC Pro GUI Configuration

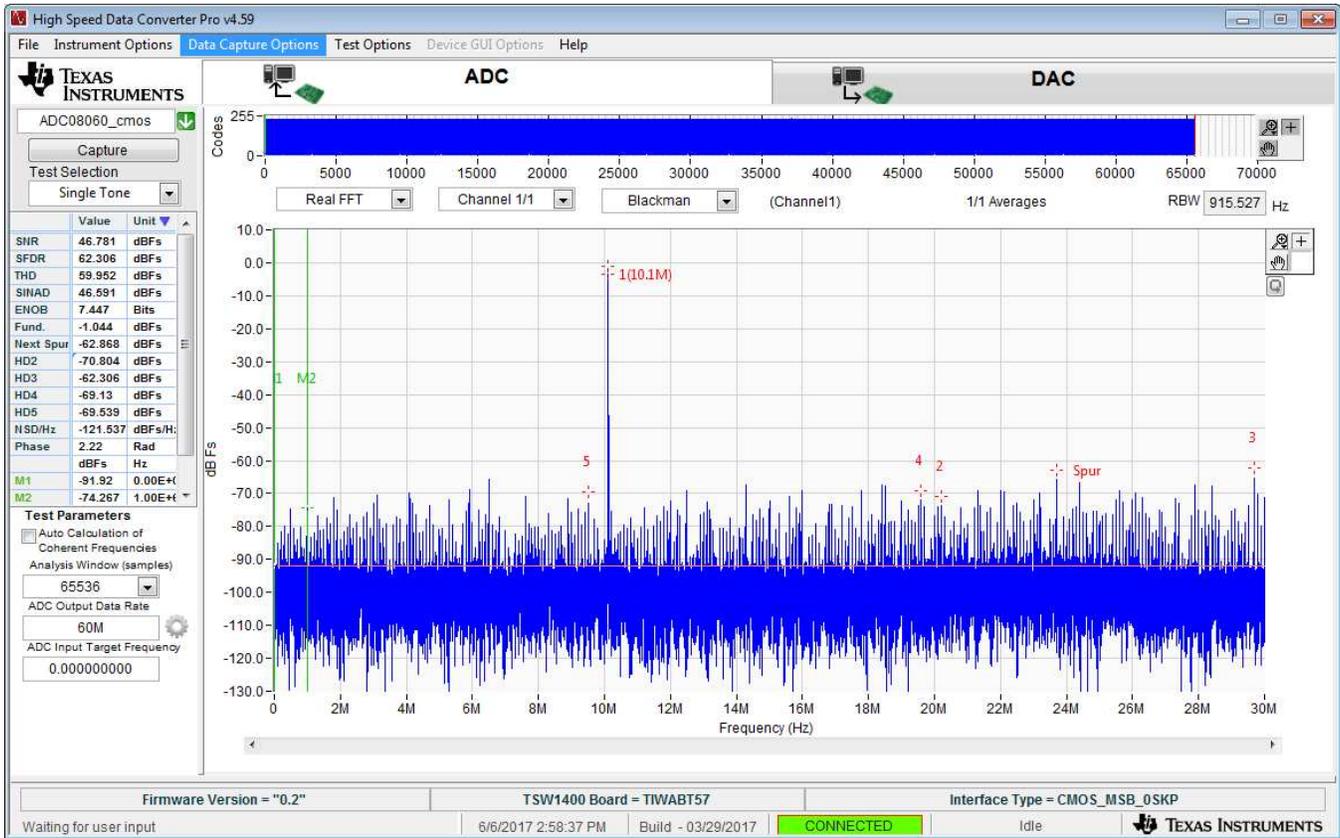
1. Open High Speed Data Converter Pro by going to *Start Menu* \rightarrow *All Programs* \rightarrow *Texas Instruments* \rightarrow *High Speed Data Converter Pro*. The GUI main page looks as shown in [Figure 3](#).



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Figure 3. HSDC Pro GUI Main Panel

2. When prompted to select the capture board, select the TSW1400 whose serial number corresponds to the serial number on the TSW1400EVM and click *OK*. This popup can be accessed through the *Instrument Options* menu.
3. If no firmware is currently loaded, there is a message indicating this. Click on *OK*.
4. Verify the *ADC* tab at the top of the GUI is selected.
5. Use the *Select ADC* drop-down menu at the top left corner to select *ADC08060_cmos*.
6. When prompted to update the firmware for the ADC, click *Yes* and wait for the firmware to download to the TSW1400. This takes a couple of seconds.
7. Enter “60M” into the *ADC Output Data Rate* field at the bottom left corner then click outside this box or press *Return* on the PC keyboard.
8. Click *Capture* in HSDC Pro to capture data from the ADC.
9. The results from the captured data of Channel 1 should look like [Figure 4](#) and the performance should be similar to [Table 1](#). If this result is not achieved, then see the [Quick Start Troubleshooting](#) section of this document.



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Figure 4. Data Capture Results for ADC08060 From Quick-Start Procedure

Table 1. Quick-Start Performance Measurements for ADC08060

Result	Measured Value	Units
SNR	46	dBFS
SFDR	62	dBFS

2.4 ADC08100EVM Setup

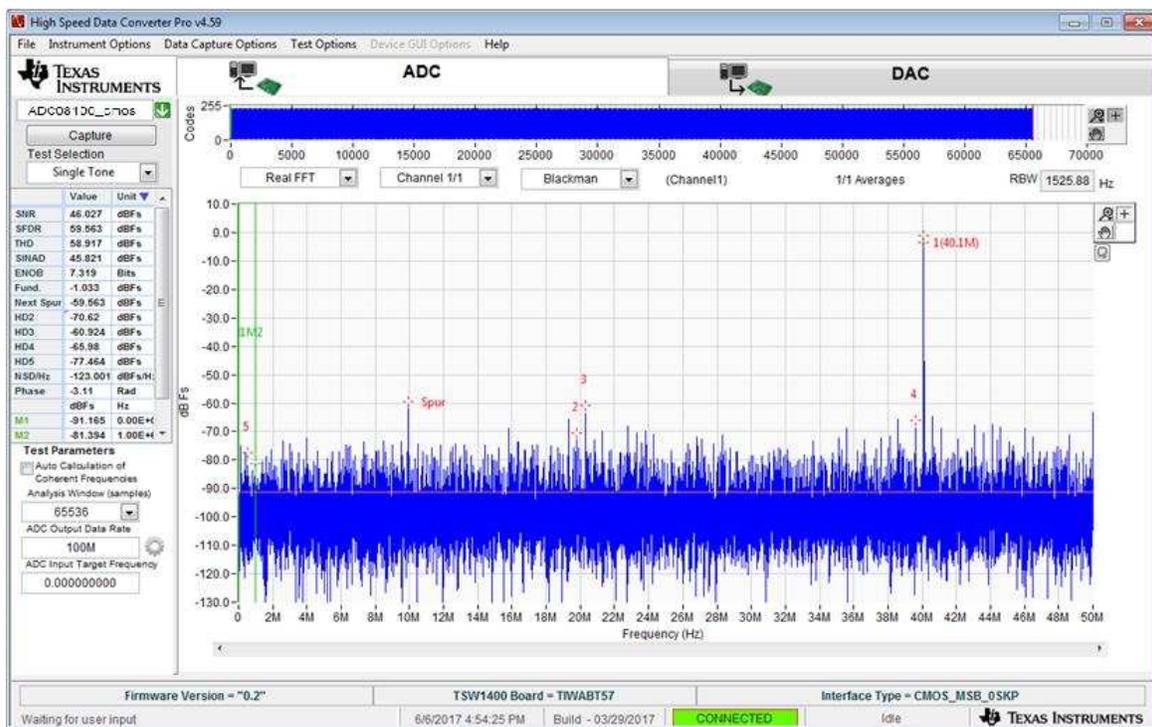
Next, setup the ADC08100EVM using the following:

1. Connect the banana jack power-supply cables to the EVM. Connect the red wire to 5 VDC ± 0.1 VDC of a power supply rated for at least 3 A to connector J4. Connect the black wire to J5 (GND) of the power supply.
2. Turn on the power supply. The power draw should be around 0.220 A after the clock is supplied.
3. Provide a 100-MHz, +5-dBm clock signal to J3.
4. Set the analog input signal generator for 40.1-MHz, -1 dB from full scale.
5. Place a 40-MHz bandpass filter at the output of the analog signal generator to remove noise and harmonics from the signal generator.
6. Connect the analog input signal generator to the EVM though SMA connector INPUT (J6) and provide a 40.1-MHz signal.

2.5 Software Setup Procedure

Follow the steps in [Section 2.3.1](#)

- When selecting the ADC in the *Select ADC* drop-down menu, make sure to select *ADC08100_cmos* and enter "100M" in *ADC Output Data Rate* field.
- The results from the captured data of Channel 1 should look like [Figure 5](#) and the performance should be similar to [Table 2](#). If this result is not achieved, then see the [Quick Start Troubleshooting](#) section of this document.



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Figure 5. Data Capture Results for ADC08100 From Quick-Start Procedure

Table 2. Quick-Start Performance Measurements for ADC08100

Result	Measured Value	Units
SNR	46	dBFS
SFDR	59	dBFS

2.6 ADC08200EVM Setup

Next, setup the ADC08200EVM using the following:

1. Connect the banana jack power-supply cables to the EVM. Connect the red wire to 5 VDC ± 0.1 VDC of a power supply rated for at least 3 A to connector J4. Connect the black wire to J5 (GND) of the power supply.
2. Turn on the power supply. The power draw should be around about 0.360 A after the clock is supplied.
3. Provide a 200-MHz, +12-dBm clock signal to J3.
4. Set the analog input signal generator for 55.1 MHz, -1 dB from full scale.
5. Place a 55-MHz bandpass filter at the output of the analog signal generator to remove noise and harmonics from the signal generator.
6. Connect the analog input signal generator to the EVM though SMA connector INPUT (J6) and provide a 55.1-MHz signal.

2.7 Software Setup Procedure

Follow the steps in [Section 2.3.1](#)

- When selecting the ADC in the *Select ADC* drop-down menu, make sure to select *ADC08200_cmos* and enter "200M" in *ADC Output Data Rate* field.
- The results from the captured data of Channel 1 should look like [Figure 6](#) and the performance should be similar to [Table 3](#). If this result is not achieved, then see the [Quick Start Troubleshooting](#) section of this document.

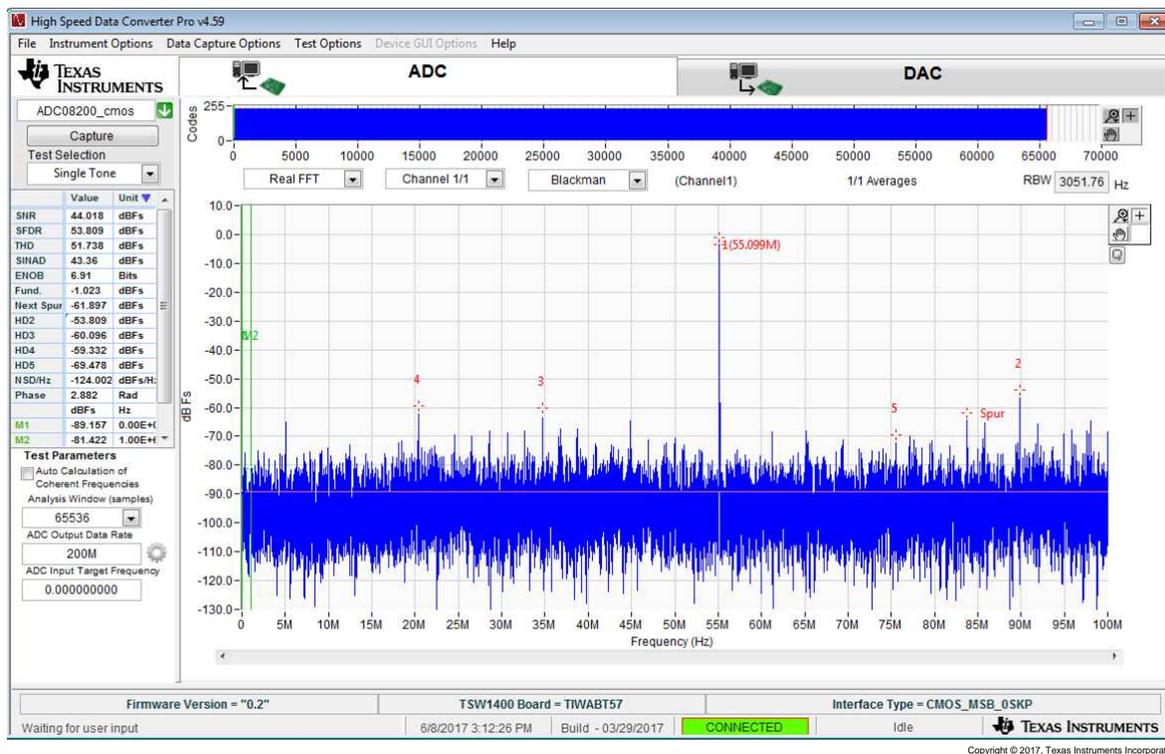


Figure 6. Data Capture Results for ADC08200 From Quick-Start Procedure

Table 3. Quick-Start Performance Measurements for ADC08200

Result	Measured Value	Units
SNR	44	dBFS
SFDR	53	dBFS

2.8 Quick-Start Troubleshooting

Use [Table 4](#) to assist with problems that may have occurred during the quick-start procedure.

Table 4. Troubleshooting Tips

Issue	Troubleshooting Tips
General problems	Verify the test setup shown in Section 2 and repeat the setup procedure as described in this document.
	Check power supplies to the EVMs. Verify that the power switches are in the ON position and supplies are drawing the appropriate current.
	Check signal and clock connections to the EVM.
	Check that all boards are properly connected together.
	Try power-cycling the external power supply to the EVM and reprogram the ADC devices.
TSW1400 LEDs are not correct: D2 – D9 OFF	Verify the settings of the configuration switches on the TSW1400EVM.
	Verify that the EVM configuration GUI is communicating with the USB and that the configuration procedure has been followed.
	Try capturing data in HSDC Pro to force an LED status update.
HSDC Pro software is not capturing good data or analysis results are incorrect.	Verify that the TSW1400EVM is properly connected to the PC with a mini-USB cable and that the board serial number is properly identified by the HSDC Pro software.
	Check that the proper ADC device is selected.
	Check that the analysis parameters are properly configured.
	Check that the fundamental power is no larger than -1 dBFs.
	Verify that the clock amplitude is correct for the particular device being used. If the issue persists, then increase the clock amplitude
HSDC Pro software gives a time-out error when capturing data	Restart HSDC Pro and reload the firmware.
	Verify that the ADC sampling rate is correct in the HSDC Pro software.
Sub-optimal measured performance	Measure test points to verify operating voltage ranges.
	Verify the jumper configurations are in default locations.
	Verify that filters are used in the clock and input signal paths and that low-noise signal sources are used.

3 Optimizing Evaluation Results

This section assists the user in optimizing the performance during evaluation of the product.

3.1 Clocking Optimization

The sampling clock provided to the ADC needs to have very low phase noise to achieve optimal results. The default EVM configuration uses a crystal oscillator to generate the sampling clock. Another option to improve the clock noise performance is bypassing the onboard clock in favor of an external clock. The clock must have very low noise and must use an external narrow pass-band filter to achieve optimal noise performance. The clock amplitude must be within the data sheet limits. See [Section 4](#) for more information regarding this setup.

3.2 Coherent Input Source

A *Rectangular* window function can be applied to the captured data when the sample rate and the input frequency are set precisely to capture an *integer* number of cycles of the input frequency (sometimes called coherent frequency). This may yield better SNR results. The clock and analog inputs must be frequency locked (such as through 10-MHz references) in order to achieve coherency.

3.3 HSDC Pro Settings

HSDC Pro has some settings that can help improve the performance measurements. These are highlighted in [Table 5](#).

Table 5. HSDC Pro Settings to Optimize Results

HSDC Pro Feature	Description
Analysis Window (Samples)	Selects the number of samples to include in the selected test analysis. Collect more data to improve frequency resolution of Fast-Fourier Transform (FFT) analysis. If more than 65,536 samples are required, increase the setting in the <i>Data Capture Options</i> to match this value.
Data Windowing Function	Select the desired windowing function applied to the data for FFT analysis. Select <i>Blackman</i> when sampling a non-coherent input signal or <i>Rectangle</i> when sampling a coherent input signal.
Test Options → Notch Frequency Bins	Select bins to be removed from the spectrum and back-filled with the average noise level. May also customize which Harmonics and Spurs are considered in SNR and THD calculations and select the method for calculating spur power.
Test Options → Bandwidth Integration Markers	Enable markers to narrow the <i>Single-Tone FFT</i> test analysis to a specific bandwidth.
Data Capture Options → Capture Options	Configure the number of contiguous samples per capture (capture depth). May also enable <i>Continuous Capture</i> and <i>FFT Averaging</i> .

4 Alternate Hardware Configurations

This section describes alternate hardware configurations in order to achieve better results or to more closely mimic the system configuration.

4.1 Clocking Options

The default clocking mode uses an external clock to generate the ADC sampling clock and FPGA clocks. An alternative option is described in the following section.

4.1.1 Onboard Oscillator Clock

An option to provide a clock source through an onboard oscillator is available. The pad on Y1 can be filled with a 6-pin SMD, no lead (7.00 mm x 5.00 mm) oscillator to provide the sampling clock for the ADC. For this option, SHUNT (JP7) to provide power to the VDD pin of the oscillator and bypass the external clock by changing the position of jumper (JP2) to SHUNT 1–2.

4.1.2 Separating the ADC and FPGA Clock

A separate clock can be provided to both the ADC and FPGA by removing R18 and adding R14. Also, SHUNT (JP10) to position 1-2 to provide power to the *Clock Buffer*. Now, J7 can be used to provide the clock signal for the FPGA, while J3 can be used to provide the clock to the ADC.

4.2 Delay Pins

Pins J8–J11 can be used to add a delay to the clock signal going into the FPGA. By default, pins J8 and J12 are SHUNT but the jumper can be positioned with any of the other J8–J11 pins. The default position of J8 and J12 adds about 0.5 ns to 1.7 ns of delay; the delay increases as the jumper is positioned with the other pins. In other words, the delay is 2× as much or 1.0 ns to 3.4 ns when J9 and J12 are SHUNT, 3× or 1.5 ns to 5.1 ns when J10 and J12 are SHUNT, and 4× or 2.0 ns to 6.8 ns when J11 and J12 are SHUNT.

4.3 Voltage Reference Options

The default configurations uses a LM8272 rail-to-rail precision op amp to drive the reference voltage. By default, the top reference voltage is set to 1.9 V and the bottom voltage is set to 0.3 V. Alternative options are described in the follow sections.

4.3.1 External Voltage Reference

An external voltage reference can be used to supply the reference voltage to the ADC. For this option, jumper VRT (JP9) and VRB (JP8) must be pulled out and left OPEN. Apply a top voltage reference at the test point VRTP (TP5) and bottom reference at VRBP (TP6). If the desired voltage references are 3 V and GND, change jumpers JP9 and JP8 to SHUNT 2-3.

4.3.2 Divider Resistor Modification

If the LM8272 is desired to drive the reference voltages, but at a different range, the divider resistors (R1 and R3) can be changed to suit the reference voltage needed. R1 and R3 are larger for easy soldering modifications.

Jumper and Connector Descriptions

A.1 Jumper Descriptions

The EVM jumpers are shown in [Table 6](#) as well as the default settings for the jumpers. Use this table to reset the EVM in the default configuration, in case of issues.

Table 6. Jumper Descriptions and Default Settings

Jumper	Description	Default Setting
JP2	Selects either onboard or external sample clock	Shunt pins 2-3
JP3	Option to bypass clock buffer	OPEN
JP4	Enable outputs from clock buffer (active high)	Shunt pins 1-2
JP5	Option to bypass clock buffer	Shunt pins 2-3
JP6	Powerdown mode for ADC08xx0 (default not in powerdown mode)	Shunt pins 2-3
JP7	Provides power to onboard clock	OPEN
JP8	Top reference voltage option (supplied by LM8272 by default)	Shunt pins 1-2
JP9	Bottom reference voltage option (supplied by LM8272 by default)	Shunt pins 1-2
JP10	Enable outputs from second clock buffer (active low)	Shunt pins 2-3
J8-J12	Option for adding delay to output clock signal	Shunt pins J8-J12

A.2 Connector Descriptions

The EVM connectors and their function are described in [Table 7](#).

Table 7. Connector Descriptions

Connector	Description
J1	CMOS pin header connector
J2	Clock output for ADC sampling and FPGA
J3	External ADC sample clock input
J4	5-V DC banana jack connector
J5	GND banana jack connector
J6	Single-ended SMA analog input
J7	Second clock output for ADC sampling and FPGA (Optional)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2017) to A Revision	Page
• Added support for the ADC08100EVM and ADC08200EVM to the user's guide globally.	1

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
 - 1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductor products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software
 - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
2. *Limited Warranty and Related Remedies/Disclaimers:*
 - 2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
 - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.
 - 2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.
3. *Regulatory Notices:*
 - 3.1 *United States*
 - 3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.
 - 3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3. 技術基準適合証明を取得後ご使用いただく。

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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