IPC-JESD204-B
ADS42JB49
IOT Report

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1 Introduction

The purpose of this document is to provide the reader with detailed understanding of how the Inter-Operability Testing has of the JESD204B receive and transmit IP cores against various hardware devices been carried out.

Each IOT setup shares a significant number of commonalities – which is the rationale behind incorporating them into a single document.

From an application point of view, the receiver and transmitter are totally separate cores – a project may utilize only one or several instances of each. However for sake of design simplicity a common RX+TX setup has been selected for the DUT.

2 Scope

This document is intended for a technical audience (engineering, marketing, customer support) with an understanding on serial interface protocols and RF systems. Engineering background on digital design is required.

The scope of this document is to present the hardware test bed setup and components, the test methodology and test cases as well as the test results. The scope is to provide integration engineers with sufficient knowledge to adapt and verify the cores in a customized environment and application.

3 Applicable and Reference Documents

Document ID	Title
JESD204B.01	Serial Interface for Data Converters (Revision of JESD204B, July 2011). Date January 2012
Avalon Spec	Avalon Interface Specification (rev. 13 May 2013). Altera (www.altera.com/literature/manual/mnl_avalon_spec.pdf)

4 Acronyms and Definitions

A/D = Analog to Digital

ASIC = Application Specific Integrated Circuit

ASSP = Application Specific Standard Product

CF = Control bits per frame

CS = Control Bits per sample

D/A = Digital to Analog

DC = Direct Current

F = Number of Octects

FPGA = Field Programmable Gate Array

HD = High Density

IC = Integrated Circuit

IP = Intellectual Property

L = Number of Lanes

M = Number of Converters

MCDA-ML = Multiple-Converter Device Alignment, Multiple-Lanes

N = Sample Resolution

N' = Sample Envelope

RTL = Register Transfer Logic

S = Samples per converter

SCR = Scrambler

VHDL = VHSIC Hardware Description Language

Names Convention:

- Generics Names = CAPITAL
- Registers Names = **CAPITAL BOLD**
- Signal Names = ***italic bold***

5 Arria V GT – ADS42JB49 Hardware IOT

5.1 ADS42JB49 Hardware Test Bed Components

The hardware test bed consists of the following items:

1. Arria V GT FPGA Development Kit (http://www.altera.com/products/devkits/altera/kit-arria-v-gt.html)
2. ADS42JB49 FMC Evaluation Card (http://www.ti.com/tool/ads42jb49evm)
3. USB cable x2, Power adapter x2

The ADS42JB49 EVM card is connected to the FMC port interfacing FPGA2 of the Arria board.

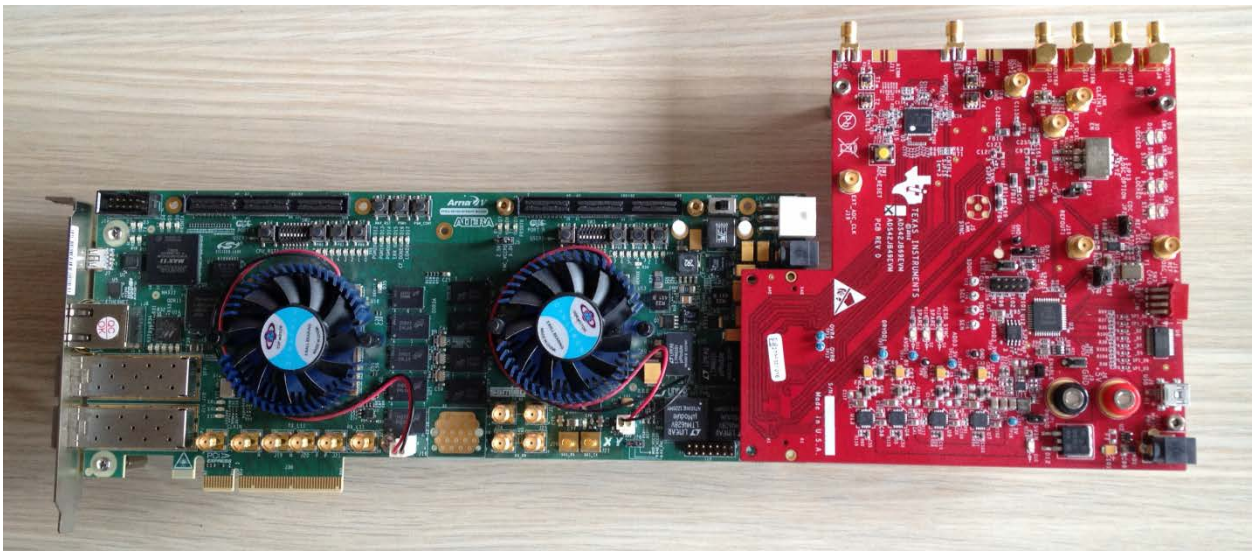

Figure 1 ADS42JB49 Hardware test bed Components

5.2 ADS42JB49 Hardware Test Bed Clocking

The clocks are generated by the LMK04828 device located on the ADS42JB49 EVM. The clock is distributed to the ADS42JB49 ADC and also to the MTI JESD204B IPC via the FMC connector. The Line rate for the tested configuration is 2.5G

The LMK configuration uses VCO 1 for reference and dividers on the DClk 2 used to clock the ADC and DClk 8 used as the clock for the MTI JESD IP serdes and device clock. The Clock received on the FMC by the IP Core is used directly as reference to the serdes. Then it is passed through a PLL and divided by a factor of 4 before being used as the device clock because the MTI JESD204B IP Cores utilize a 40bit serdes interface.

The serdes and device clocks are output on the HSMC card and can be monitored by using a HSMC-SMA breakout card and an oscilloscope.

The SYSREF is also generated by the LMK04828 and propagated to the MTI JESD204B IPC over the FMC connector and also used by the ADS42JB49.

5.3 ADS42JB49 Hardware Test Bed FPGA2 Pin Out

Node Name	Direction	Location	I/O Standard
clkina_50	Input	PIN_AP34	1.8 V
cpu1_resetn	Input	PIN_L6	2.5 V
fmc_clk_in_GTX	Input	PIN_AB9	LVDS
fmc_clk_in_GTX(n)	Input	PIN_AB8	LVDS
Fmc_led_jesdsync	Output	PIN_AU13	2.5 V (default)
fmc_rx_0	Input	PIN_AE1	2.5-V PCML
fmc_rx_0(n)	Input	PIN_AE2	2.5-V PCML
fmc_rx_1	Input	PIN_AA1	2.5-V PCML
fmc_rx_1(n)	Input	PIN_AA2	2.5-V PCML
fmc_rx_2	Input	PIN_U1	2.5-V PCML
fmc_rx_2(n)	Input	PIN_U2	2.5-V PCML
fmc_rx_3	Input	PIN_R1	2.5-V PCML
fmc_rx_3(n)	Input	PIN_R2	2.5-V PCML
fmc_spare_led_1	Output	PIN_AL14	2.5 V (default)
fmc_spare_led_2	Output	PIN_AK14	2.5 V (default)
fmc_sync_ads	Output	PIN_AP9	LVDS
fmc_sync_ads(n)	Output	PIN_AN9	LVDS
fmc_sysref	Output	PIN_AW15	LVDS
fmc_sysref(n)	Output	PIN_AW14	LVDS
fmc_tx_0	Output	PIN_AD3	1.5-V PCML
fmc_tx_0(n)	Output	PIN_AD4	1.5-V PCML
fmc_tx_1	Output	PIN_Y3	1.5-V PCML
fmc_tx_1(n)	Output	PIN_Y4	1.5-V PCML

fmc_tx_2	Output	PIN_T3	1.5-V PCML
fmc_tx_2(n)	Output	PIN_T4	1.5-V PCML
fmc_tx_3	Output	PIN_P3	1.5-V PCML
fmc_tx_3(n)	Output	PIN_P4	1.5-V PCML
hsmc_clkout_J25	Output	PIN_AE26	2.5 V (default)
hsmc_clkout_J27	Output	PIN_AD26	2.5 V (default)
user1_led_g[0]	Output	PIN_M19	2.5 V (default)
user1_led_g[1]	Output	PIN_L19	2.5 V (default)
user1_led_g[2]	Output	PIN_K19	2.5 V (default)
user1_led_g[3]	Output	PIN_J19	2.5 V (default)
user1_led_g[4]	Output	PIN_K20	2.5 V (default)
user1_led_g[5]	Output	PIN_J20	2.5 V (default)
user1_led_g[6]	Output	PIN_T20	2.5 V (default)
user1_led_g[7]	Output	PIN_R20	2.5 V (default)

Table 1 Pin Out for FPGA2 of the IOT test bed

5.4 ADS42JB49 Hardware Test Bed VHDL Setup

The test bed consist of a top level entity “jesd204b_eval_tiads42_top” which instantiates the nios processor and the core test bed “jesd204b_eval_core”, and also routes the two blocks together and to the In Out interfaces (clocks, HSMC, FMC, LEDs and pushbuttons).

The “jesd204b_eval_core” module instantiates the RX and TX IP Cores, they can be used back to back but in the ADS42JB49 test bed scenario only the RX core is utilized. It also instantiates the serdes modules and the required reset and reconfiguration blocks accompanying them. This module also controls the RX sample checking (data patterns validation) and sample captures.

The RX and TX cores do not include serdes modules but provide a multiple of 10bit wide interface to them. The width of this interface is controlled with a generic NO_SERDES_WORDS. In this test bed a 40 bit interface is used for the serdes. The IP cores also include a CPU interface to which the NIOS processor is connected allowing reading and writing of the internal register values during the CORE operation.

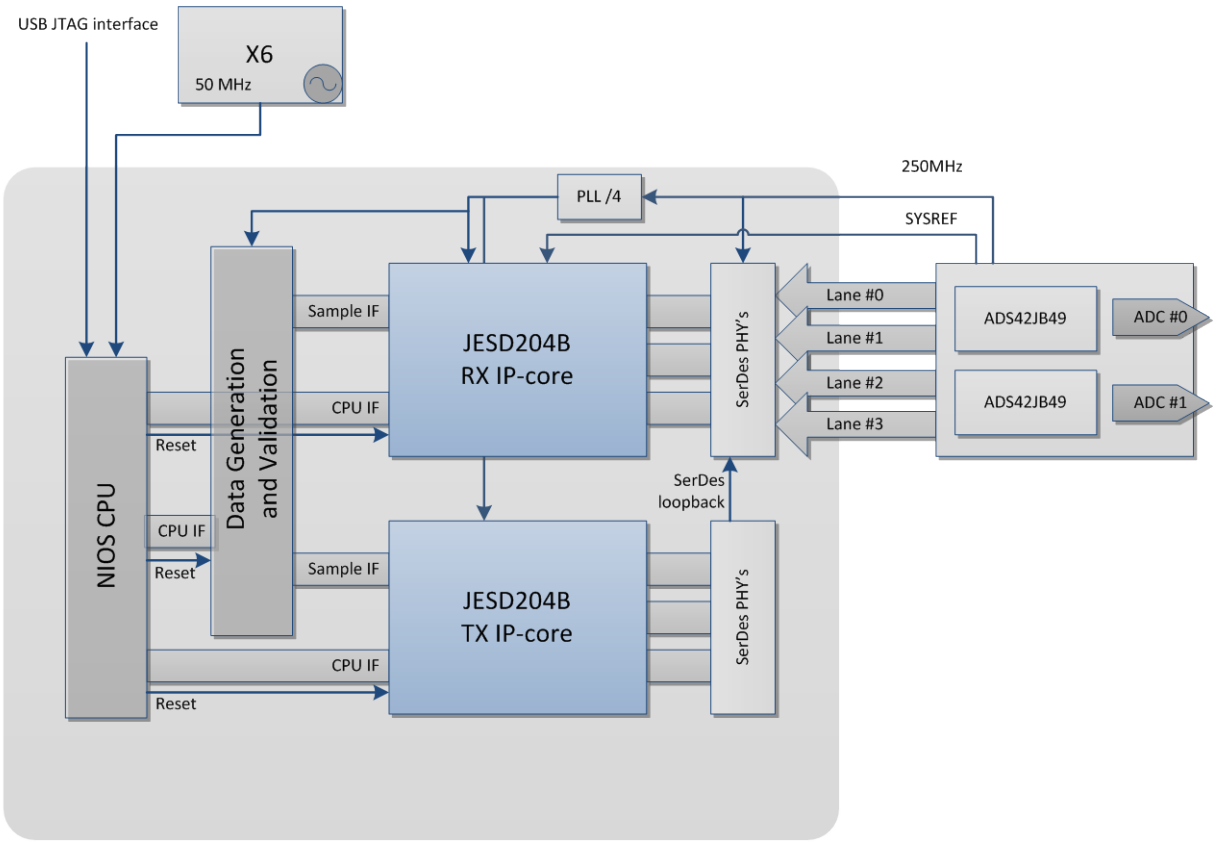

Figure 2 HW test bed diagram

5.5 ADS42JB49 Hardware Test Bed NIOS Software

The software running on the NIOS processor plays key role in the IOT test bed. It has access to the CPU interfaces of the TX and RX cores as well as the test bed core module. It is able to reconfigure on the fly the various operating parameters of the RX core. The ADS42JB49 device However must be configured manually through the GUI interface. This allows the software to control the test parameters, device configurations, and run times. It is also able to read out the test results from the data validator error indicators as well as the RX core error counters.

The NIOS software provides a console based interface allowing the user to initialize and monitor the automated test sequence as well as the IP core and serdes status. It provides direct access to the IP core and test bed registers. This allows full control of the IP core.

Command	Description
Main Menu	
c	Rx module status (enabled, scrambling)
d	Rx module configuration (enable, scrambling)
l, m	Run full ADS42JB49 IOT test sequence (l is used for LMF 421 and m for LMF 222 case SOF file)
r	Read Write registers
t	Evaluation test bed status (SerDes status, RX Error counters, Data Validators status)
y	Evaluation test bed configuration (Resets, Serdes Loopback)
Register sub menu (r)	
a	Set the command address
v	Set the value to write
r	Read from address set by (a)
w	Write value set in (v) to address set by (a)

Table 2 Relevant software commands for the ADS42JB49 IOT test bed

5.6 Device Configuration Overview

The ADS42JB49 evaluation card consists of an ADS42JB49 chip carrying data from 2 converters over 1 or 2 lanes. This adds up to a maximum of 2 converters over 4 lanes. It is however impossible to test scenarios of 2 converters over 1 lane.

The following device configurations have been found appropriate:

#	L	M	F	K	HD	SCR	S	N	N'	CF	CS
1	4	2	1	12,16,20,24,28,32	0	0,1	1	14	16	0	0
for four lanes carrying data from two converters over 1 frame											
2	2	2	2	8,12,16,20,24,28,32	0	0,1	1	14	16	0	0
for two lane carrying data from two converters over 2 frames											

Table 3 ADS42JB49 valid device configurations

Because the ADS42JB49 evaluation card hosts 2 separate devices it is not possible to test complex data mappings across all 4 lanes from both modules like L=1 M=2.

Due to clocking scheme differences between the two cases there are 2 separate Quartus projects available. When running the LMF 421 test bed, use the "l" software command. When running the LMF 222 test bed, use the "m" software command.

5.7 Test Cases Overview

There are 2 ADS42JB49 configuration scripts included for each test scenario (ADS_LMF_321 and ADS_LMF_222). These can be loaded into the ADS42JBx9 GUI and uploaded to the device.

The following test cases have been devised for the IOT.

1. **K28.5 test** – A continuous sequence of /K28.5/ characters for code group synchronization. This test can be configured in the following manner:
   On the ADS42JBx9 GUI:
   a. For the JESD_SETTINGS panel set the LINK LAYER TESTMODE dropdown to K28.5
   On the MTI RX IPC test bed:
   b. Read each of the registers in the **ERRORCOUNTER** group 0x00A0 to reset the error counters (There is an error counter register for each lane at address 0xA0+4*i where i=Lane Number)
   c. Wait for the test time duration
   d. Read the register group **ERRORCOUNTER** to recover the test errors (The error counters count LCV errors from the 8b10b decoded and indicate the amount of occurring errors.)
   The Data checker in this case resides in the RX core in the 8b10b device. Whenever a 8b10b encoding error is detected the **ERRORCOUNTER** register is incremented.

2. **Incremental Pattern test** – A test pattern where each consecutive sample is an increment of the previous one. This test can be configured in the following manner:
   On the ADS42JB49:
   a. For the JESD_SETTINGS panel set the LINK LAYER TESTMODE dropdown to NORMAL ADC DATA
   On the MTI RX IPC test bed:
   b. Write to the **TOP_SAMPLE_CTRL** register 0x2058 value 0x0000 to set up incremental test validation (The validator outputs the test results via the **TOP_CHECK** register 0x2000)
   c. Read the **TOP_CHECK** register 0x2000 to reset the error sticky bits
   d. Wait for the test time duration
   e. Read the **TOP_CHECK** register 0x2000 to recover the test results (The register contents are as follow:
      - Bit[0] – Converter 0 current data received valid
      - Bit[1] – Converter 0 error hold (read and clear)
      - Bit[2] – Converter 1 current data received valid
      - Bit[3] – Converter 1 error hold (read and clear)
      - Bit[4] – Converter 2 current data received valid
      - Bit[5] – Converter 2 error hold (read and clear)

- Bit[6] – Converter 3 current data received valid
- Bit[7] – Converter 3 error hold (read and clear)

Valid test result for 1 lane is 0x03 for 4 lanes 0x55, there are no error counters just a valid and error indication)

The Data checker in this case resides outside of the RX core in the core test bed module. The checker will monitor the sample interface of the RX for data and validate if the data sequence matches the settings, in this case if it is an incremental data sequence for each de-mapped converter.

Note: These test case configuration sequences assume the ADS42JB49 and MTI JESD204B RX modules have been configured with the correct and matching L,M,F,N,N',K,SCR,S,CS,HD,CF values.

5.8 Test Results

Each row in the table contains test results of the 3 test cases for a specific device configuration. Each test was run for 30 seconds at the rate of 3G and 5G, a detailed explanation of the test results is provided in the following chapter.

Test no.	L	M	F	K	SCR	K28.5	Incremental
1	4	2	1	12	0	PASS	PASS
2	4	2	1	12	1	PASS	PASS
3	4	2	1	16	0	PASS	PASS
4	4	2	1	16	1	PASS	PASS
5	4	2	1	20	0	PASS	PASS
6	4	2	1	20	1	PASS	PASS
7	4	2	1	24	0	PASS	PASS
8	4	2	1	24	1	PASS	PASS
9	4	2	1	28	0	PASS	PASS
10	4	2	1	28	1	PASS	PASS
11	4	2	1	32	0	PASS	PASS
12	4	2	1	32	1	PASS	PASS
13	2	2	2	12	0	PASS	PASS
14	2	2	2	12	1	PASS	PASS
15	2	2	2	16	0	PASS	PASS
16	2	2	2	16	1	PASS	PASS
17	2	2	2	20	0	PASS	PASS
18	2	2	2	20	1	PASS	PASS
19	2	2	2	24	0	PASS	PASS
20	2	2	2	24	1	PASS	PASS

21	2	2	2	28	0	PASS	PASS
22	2	2	2	28	1	PASS	PASS
23	2	2	2	32	0	PASS	PASS
24	2	2	2	32	1	PASS	PASS

Table 4 ADS42JB49 Test Results

PASS – no errors detected, FAIL – at least 1 error occurred.

5.9 Test Results Interpretation

For tests marked as PASS there were 0 errors observed while the test was running.

5.10 Quick Setup Guide

This chapter describes the necessary steps required to reproduce the test results.

1) Synthesize the ADS42JB49 IPC test bed. This step will require generation of the NIOS core in QSYS.

   Or use the provided .sof file

2) Build the IOT HW test bed from the components listed in the beginning of this chapter
3) Compile the NIOS software project
4) Upload the SOF and run the NIOS software
5) The default configuration prepared for quick IOT testing, use the “l” command to start the IOT for LMF 421. If running the LMF 222 configuration, use the “m” command to start the IOT.
6) During the testing configure the ADS42JB49 according to the instructions displayed by the test bed. Press Enter after each configuration step to continue the testing.

To interpret the results, if a test passes it will receive a PASS text, if it fails the content of the error counters for the k28.5 test or the **TOP_CHECK** register will be output to the console as the test result.

Sample of expected output:

```
Select Choice (a-y): [Followed by <enter>] l
Configure the ADC for each step and press any key.
Configure: L=4 M=2 F=1 SCR=0 K=11 SYSREF_div=288
SYSREFDEL=26

Set the LINK LAYER TESTMODE to K28.5 on the ADS42JBx9 GUI. Press enter
 285: PASS

Set the LINK LAYER TESTMODE to NORMAL ADC DATA on the ADS42JBx9 GUI. Press enter
 Inc: PASS
```

```
Press enter
```

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