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3-Wire RTD Measurement System Reference Design, -200°C to 850°C

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Circuit Description

This ratiometric temperature acquisition system accurately measures temperature over a wide range of -200°C to 850°C. The design uses a resistance temperature detector (RTD) in a 3-wire configuration to minimize the errors introduced by the lead resistances of a remotely located RTD. A 24-bit delta-sigma (ΔΣ) analog-to-digital converter (ADC) is used in this design which features two integrated precision current sources that excite the 3-wire RTD. The differential voltage that develops across the RTD is converted into a digital output code and translated into a final temperature result.

Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
ADS1247	Product Folder
TPS7A4901	Product Folder

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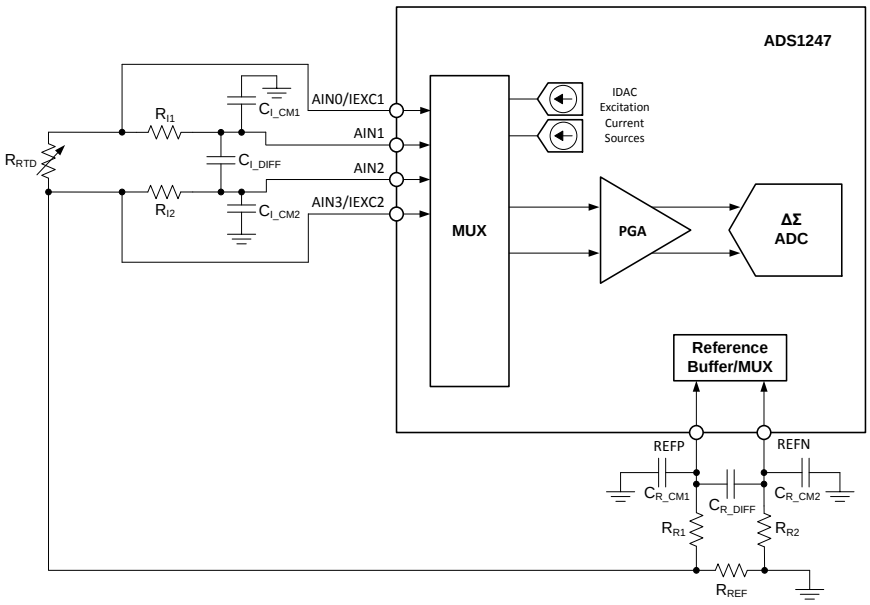

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1 Design Summary

The design requirements are as follows:

- RTD Type: 3-Wire Pt100
- Temperature Measurement Range: -200°C to 850°C
- Temperature Measurement Accuracy: ±0.05°C at T_A = 25°C
- System Supply Voltage (VDUT): 5 V
- ADC Supply Voltage (AVDD): 3.3 V

The design goals and performance are summarized in Table 1. Figure 1 depicts the measurement accuracy of the design.

Table 1. Comparison of Design Goals and Measured Performance

	Goal	Calculated	Measured
Unadjusted Resistance Measurement Accuracy	±0.1 Ω	±0.082 Ω	±0.096 Ω
Calibrated Resistance Measurement Accuracy	±0.01925 Ω	±0.0049 Ω	±0.00415 Ω
Calibrated Temperature Measurement Accuracy	±0.05°C	±0.013°C	±0.0106°C

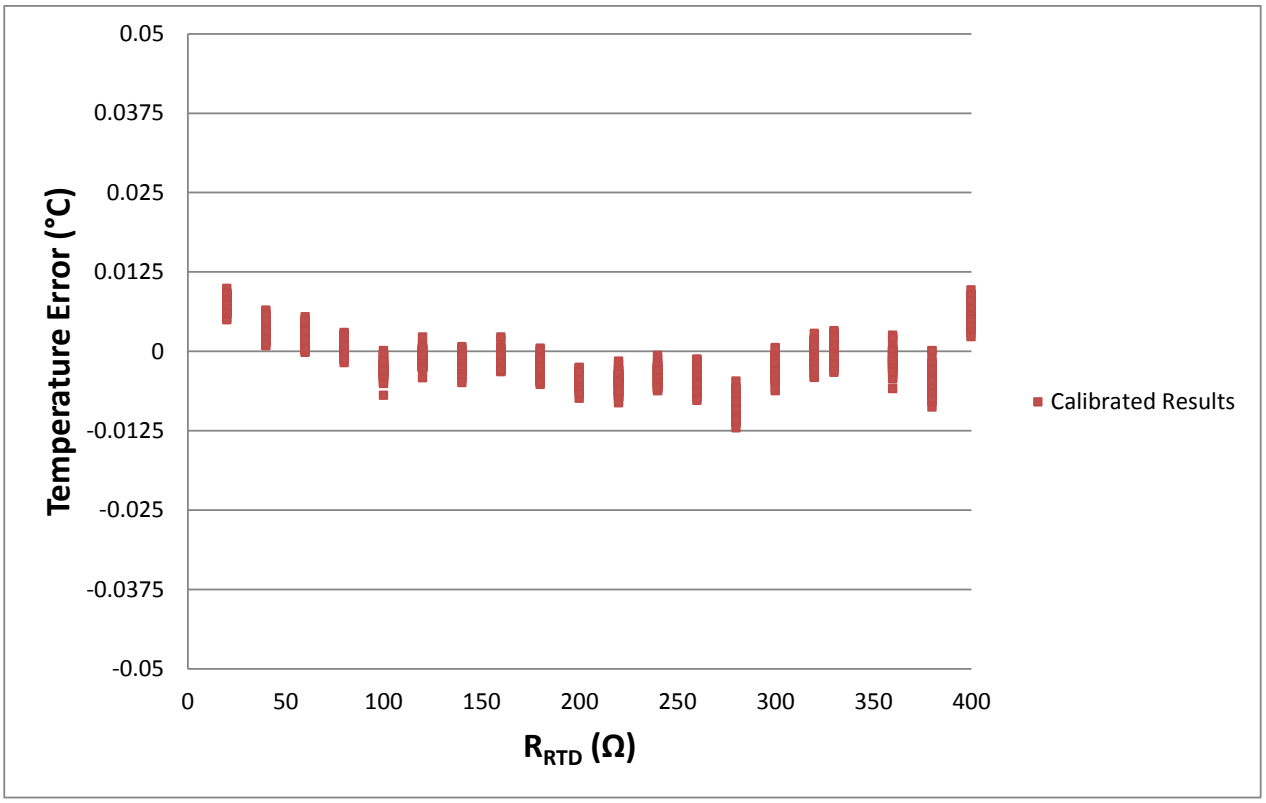

Figure 1. Measured Temperature Accuracy with Resistive Input Representing -200°C to 850°C

2 Theory of Operation

2.1 Resistance Temperature Detector (RTD) Overview

An RTD is a sensing element made of a metal with predictable resistance characteristics over temperature. The temperature of an RTD can therefore be calculated by measuring the resistance. RTD sensors offer wide temperature ranges, good linearity, and excellent long-term stability and repeatability, making them suitable for many precision measurement applications.

The relationship between resistance and temperature of an RTD is defined by the Callendar-Van Dusen (CVD) equations which can be found in Appendix A.4.

Compared to a thermocouple, the main disadvantages of RTD sensors are their cost and required excitation source. The small change in resistance of an RTD over temperature also places demands on the accuracy of the acquisition circuit requiring a precision signal chain. Thermistors have larger changes in resistance over temperature but are much less linear, reducing their effectiveness at measuring wider temperature ranges.

2.2 RTD Resistance Measurement

Most RTD applications use a current source as excitation for the RTD element. By driving a known current through the RTD, a voltage potential is developed that is proportional to the resistance of the RTD and the excitation current. This voltage potential is amplified and then fed to the inputs of an ADC, which converts the voltage into a digital output code that can be used to calculate the RTD resistance.

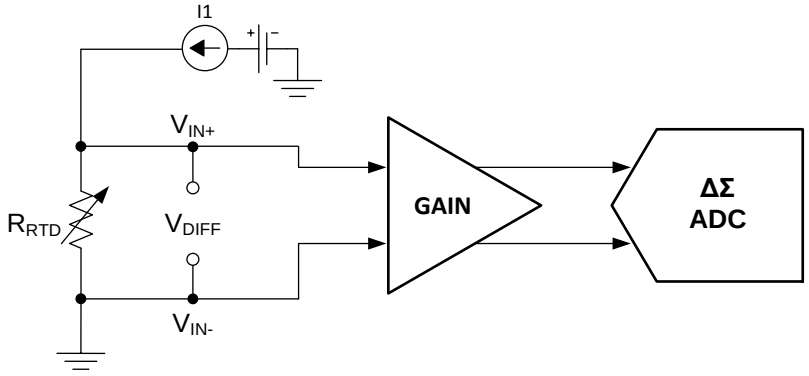

Figure 2. Simplified RTD Application

$$V_{DIFF} = V_{IN+} - V_{IN-} = I_1 \times R_{RTD} \quad (1)$$

2.2.1 Ratiometric Measurements

An ADC requires a reference voltage to convert the input voltage into a digital output. In most applications, this reference is fixed and either internally generated or externally applied to the ADC. This 3-wire RTD system uses what is known as a ratiometric configuration to create the reference voltage, increasing system accuracy.

In the ratiometric configuration shown in Figure 3, the excitation current that flows through the RTD returns to ground through a low-side reference resistor, R_{REF}. The voltage potential developed across R_{REF}, V_{REF}, is fed into the positive and negative reference pins (REFP and REFN) of the ADC. V_{REF} serves three purposes in this design: it sets the input common-mode voltage (V_{CM}), the differential ADC input range (typically $\pm V_{REF}$), and it is also used to convert the input voltage into digital output codes. See Equations (2) – (6).

Setting V_{REF} to mid-supply results in optimal input circuit performance for the ADC. R_{REF} should be selected with low tolerance and low drift since errors in the reference voltage will directly translate into errors in the conversion result.

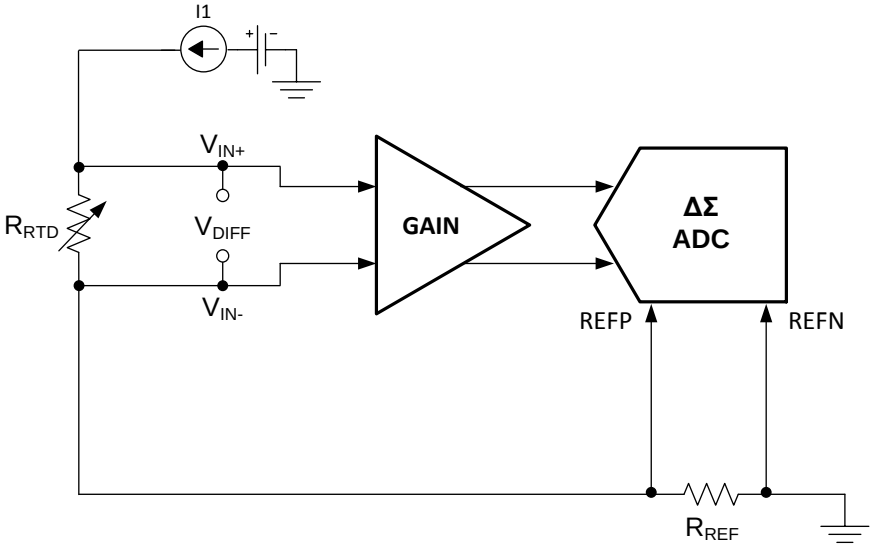

Figure 3. Ratiometric RTD Measurement

$$V_{REF} = V_{CM} = I_1 \times R_{REF} \quad (2)$$

$$\frac{-V_{REF}}{Gain} \le V_{DIFF} \le \frac{+V_{REF}}{Gain} \quad (3)$$

The voltage drop across the RTD and R_{REF} resistors is produced by the same excitation source in a ratiometric configuration as shown in Equations (4) - (5). Therefore, any changes in the excitation source are reflected in both the RTD differential voltage and the reference voltage. Since the ADC output code is a relationship between the input voltage and the reference voltage, the final conversion result is simply a ratio of the RTD and R_{REF} resistances as shown in Equation (6). Consequently, inaccuracies due to magnitude, temperature drift, and noise of the current source cancel without affecting the final conversion result. The ratiometric configuration also helps reduce the effects of external noise that appears common to both the inputs and the reference because it should cancel as well.

$$V_{DIFF} = V_{RTD} = I_1 \times R_{RTD} \quad (4)$$

$$V_{REF} = I_1 \times R_{REF} \quad (5)$$

$$Code_{IDEAL} = Codes_{TOTAL}\left(\frac{V_{DIFF} \times Gain}{2 \times V_{REF}}\right) = Codes_{TOTAL}\left(\frac{R_{RTD} \times Gain}{2 \times R_{REF}}\right) \quad (6)$$

2.2.2 Current Sources

Two precision current sources are typically used in 3-wire RTD applications to provide an easy way to cancel the RTD lead resistances (R_{LEAD}) as shown in Figure 4. This technique works best when the two current sources are well-matched, both in initial accuracy and temperature drift. For additional information on other RTD configurations, refer to Reference 2.

Equations (7) – (10) derive the final differential input voltage and prove that R_{LEAD} is excluded from the final result.

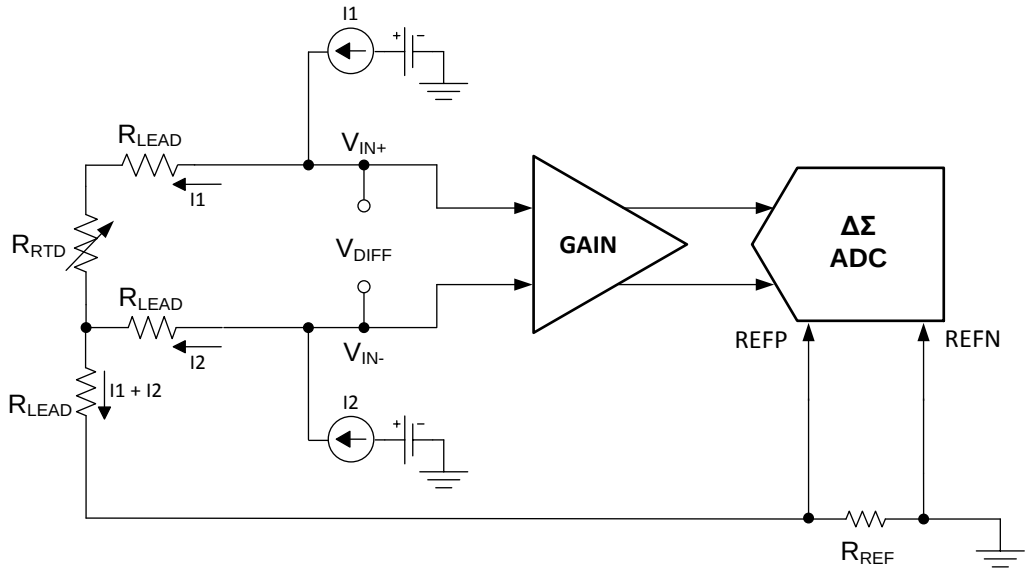

Figure 4. 3-Wire RTD Lead Resistances Canceled by Excitation Currents

$$I_1 = I_2 = I \quad (7)$$

$$V_{IN+} = I \times (R_{LEAD} + R_{RTD}) + 2 \times I \times (R_{LEAD} + R_{REF})$$
$$V_{IN+} = 3 \times I \times R_{LEAD} + 2 \times I \times R_{REF} + I \times R_{RTD} \quad (8)$$

$$V_{IN-} = I \times R_{LEAD} + 2 \times I \times (R_{LEAD} + R_{REF})$$
$$V_{IN-} = 3 \times I \times R_{LEAD} + 2 \times I \times R_{REF} \quad (9)$$

$$V_{DIFF} = V_{IN+} - V_{IN-} = I \times R_{RTD} \quad (10)$$

With two current sources flowing through R_{REF} in this 3-wire RTD system, the V_{REF} voltage doubles as shown in Equation (11). Therefore, the final conversion result transfer function also changes as shown in Equation (12).

$$V_{REF} = 2 \times I \times R_{REF} \quad (11)$$

$$Code_{OUTPUT} = Codes_{TOTAL} \left(\frac{R_{RTD} \times Gain}{4 \times R_{REF}} \right) \quad (12)$$

The magnitude of the current sources directly affects the magnitude of the RTD voltage. While maximizing the magnitude of the excitation current would seem desirable, higher excitation currents create a concern for violating the compliance voltage of the current source as well as errors due to self-heating.

The current sources will have a compliance voltage limitation based on the topology and supply voltage. The voltage on the positive input (V_{IN+}) must be limited to a level below the compliance voltage for the current sources as defined by Equation (13).

$$V_{IN+} = V_{CM} + (I_1 \times R_{RTD}) \leq V_{Compliance} \quad (13)$$

The power-dissipation in the RTD leads to self-heating errors that cannot be easily corrected and should be kept lower than 25% of the total error budget as a general practice. Keeping the excitation current small will also minimize the heat produced in other signal path components, reducing drift and other additional measurement errors. Figure 5 displays the self-heating errors in degrees Celsius versus applied excitation current for both small and large RTD elements. The typical range of RTD self-heating coefficients is 2.5 mW/°C for small, thin-film elements (shown in blue) and 65 mW/°C for larger, wire-wound elements (shown in red).

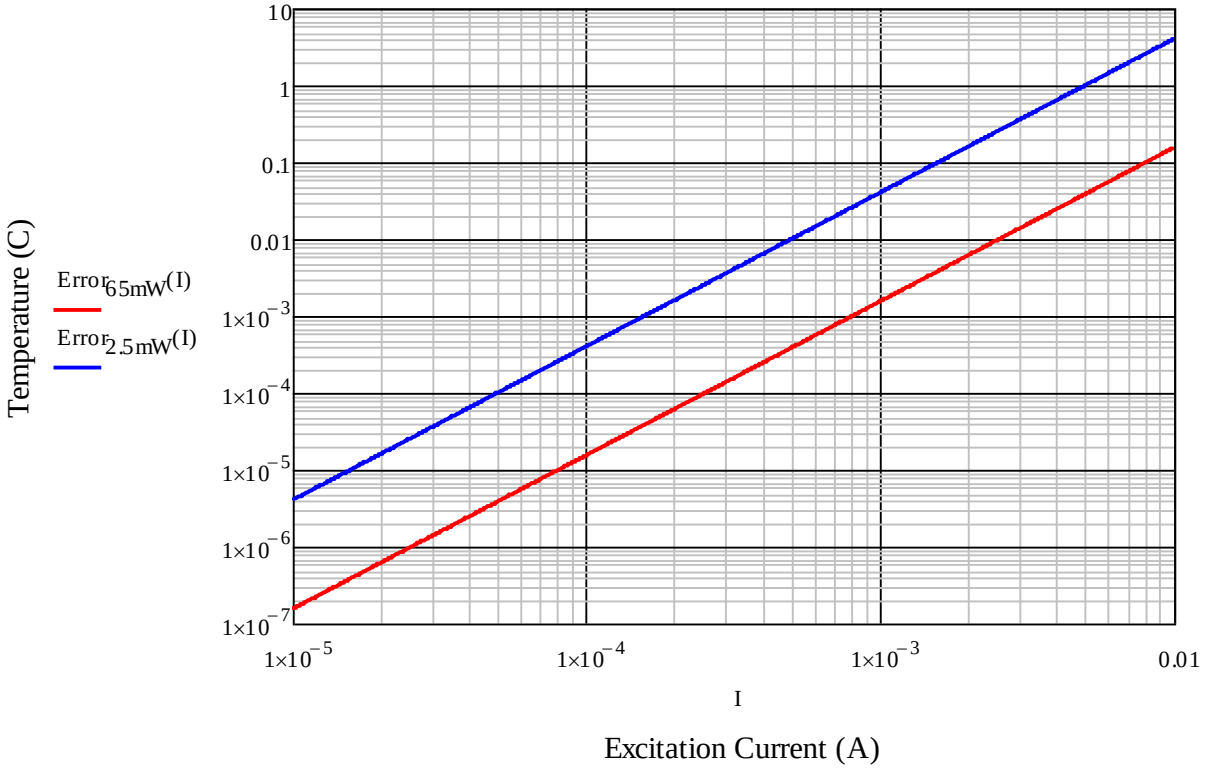

Figure 5. RTD Self-Heating vs. Excitation Current for Different RTD Types

The effects of self-heating on measurement accuracy are also based on the placement of the RTD in the application. The effects of self-heating are reduced if the RTD is placed in a moving fluid medium because the moving fluid will keep the RTD close to the temperature of the fluid. However, in open-air temperature measurements, or other applications where the RTD is surrounded by an insulator, the RTD will self-heat and cause errors.

2.2.3 Amplification Stage

The full-scale input range of an ADC is bounded by the reference voltage, V_{REF}. By choosing a smaller value for the excitation current to reduce self-heating, the RTD produces a smaller change in voltage over the span of the temperature measurement that will not use the full ADC input range. Therefore, a gain stage is required to amplify the RTD voltage to a level that utilizes more of the range of the full-scale ADC input, V_{IN_ADC}, and maximizes the measurement resolution.

$$V_{IN\_ADC} = I_1 \times R_{RTD} \times \text{Gain} \quad (14)$$

The gain must be selected such that neither the full-scale input voltage nor the common-mode input voltage is violated. Both limitations are typically found in the device specifications section of the data converter datasheet.

2.2.4 Input and Reference Low-Pass Filters

Using differential and common-mode low-pass filters at the input and reference paths improves the cancellation of excitation and environmental noise. However, it is important to note that the corner frequency of the two differential filters must be well-matched as stated in Reference 1. The input and reference filters are shown in Figure 6.

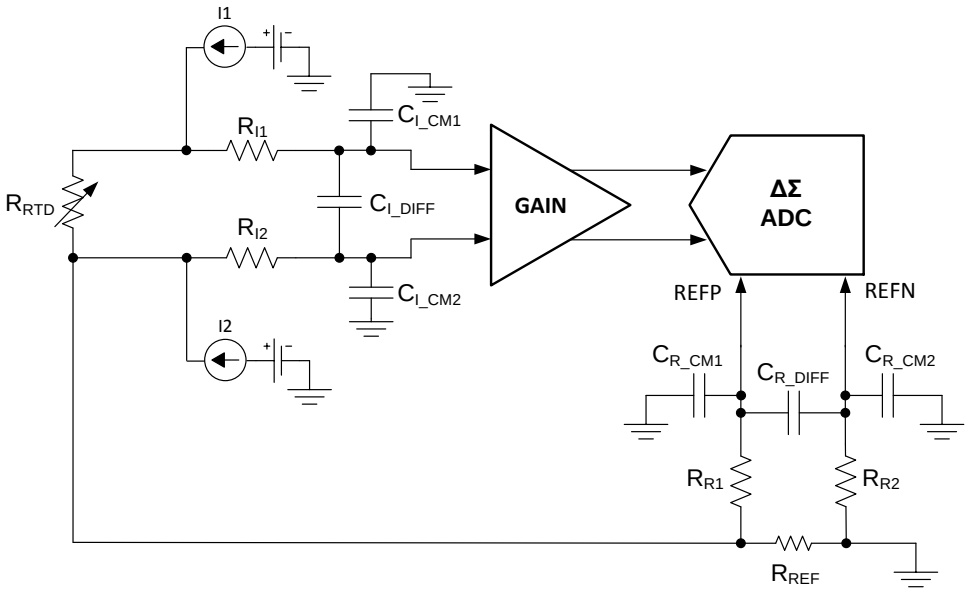

Figure 6. Input and Reference Low-Pass Filtering

3 Component Selection

3.1 ADC – ADS1247

As shown in Figure 7, the ADC chosen for this application is the ADS1247. This device not only has the resolution and accuracy needed to achieve the aforementioned design goals, but also features all the internal sub-circuits required to realize the design.

The ADS1247 is a 24-bit, delta-sigma (ΔΣ) ADC that offers a complete front-end solution for RTD applications. It comes from a product family of highly integrated precision data converters, featuring a low-noise programmable gain amplifier (PGA), a precision ΔΣ modulator, a digital filter, an internal oscillator, and two digitally controlled precision current sources (IDACs). It is a popular industry choice for precision temperature measurement applications. Other popular choices listed in Table 10 and Table 11 showcase similar functionality and performance.

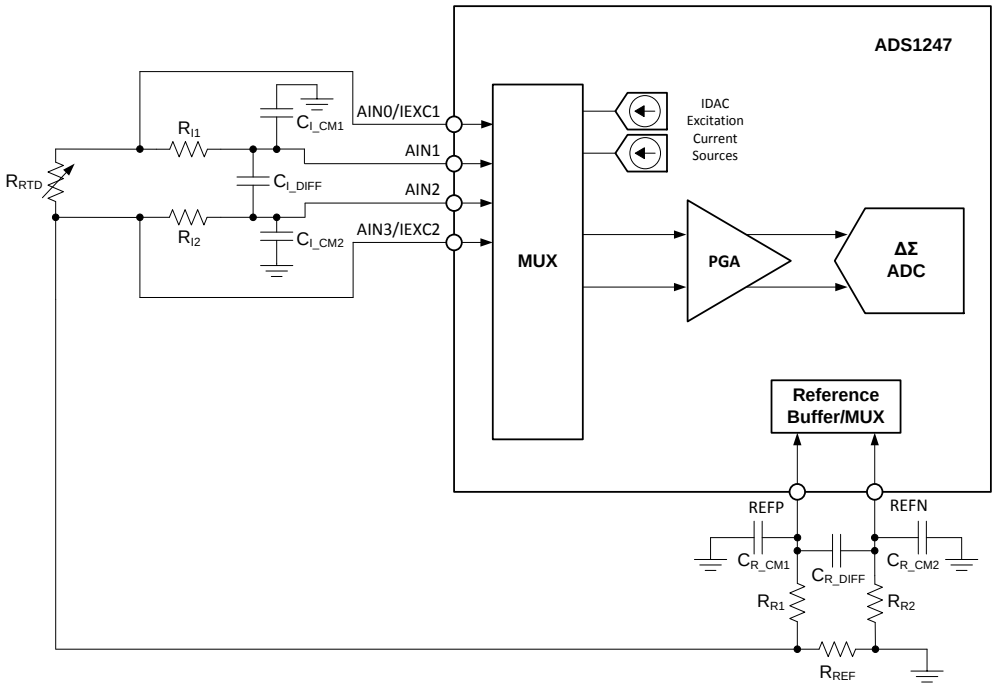

Figure 7. Ratiometric RTD System Featuring the ADS1247

3.1.1 Current Source (IDAC) Configuration

The ADS1247 features two IDAC current sources capable of outputting currents from 50 µA to 1.5 mA. Based on Figure 5, the excitation currents will be set to 1 mA to maximize the RTD sensor output while keeping the errors due to self-heating less than the desired goal of 0.05°C.

The internal reference voltage must be on while using the IDACs, even if an external ratiometric reference is used for ADC conversions. Table 2 displays the required register settings to set the IDACs to 1 mA and configure them for the proper output channels.

Table 2. Register Settings for Current Sources

Register (Address)	Register Bits	Bits Name	Bit Values	Comment
MUX1 (02h)	MUX1[6:5]	VREFCON[1:0]	01	Internal Reference ON
IDAC0 (0Ah)	IDAC0[2:0]	IMAG[2:0]	110	IDACs = 1 mA
IDAC1 (0Bh)	IDAC1[7:4]	I1DIR[3:0]	0000	IDAC1 → AIN0
IDAC1 (0Bh)	IDAC1[3:0]	I2DIR[3:0]	0011	IDAC2 → AIN3

3.1.2 IDAC Multiplex Chopping

As the equations in Section 2.2.2 show, the two current sources must be exactly matched to successfully cancel the lead resistances of the RTD wires. While initial matching of the current sources is important, any remaining mismatch in the two sources can be minimized by using a multiplexer to swap, or "chop," the two current sources between the two inputs. Taking measurements in both configurations and averaging the readings will greatly reduce the effects of mismatched current sources. This design uses the digitally-controlled multiplexer in the ADS1247 to realize this technique. The multiplexer also affords the user some additional flexibility when routing the input voltage signals and excitation current sources on their printed circuit board (PCB) layout.

3.1.3 Programmable Gain Amplifier (PGA) Configuration

In this application, the ADC uses a 3.3 V supply for both the analog (AVDD) and digital (DVDD) power supplies. The excitation currents and R_{REF} have been selected to produce a 1.64 V reference, allowing for a differential input signal range of ±1.64 V into the ΔΣ modulator. The maximum allowable PGA gain setting is based on the reference voltage, the RTD resistance change, and the excitation current as shown in Equations (15) – (17).

$$R_{RTD@850°C} = 390.48\ \Omega \quad (15)$$

$$V_{IN\_MAX} = R_{RTD@850°C} \times I_{IDAC} = 390.48\ \Omega \times 1\ mA$$
$$V_{IN\_MAX} = 390.48\ mV \quad (16)$$

$$Gain_{MAX} = \frac{V_{REF}}{V_{IN\_MAX}} = \frac{1.64\ V}{0.39048\ V} = 4.2\ \frac{V}{V} \quad (17)$$

The PGA gain is set to the closest ADS1247 PGA gain that is below the maximum value calculated in Equation (17). The PGA will be set to 4 V/V, as shown in Table 3.

Table 3. Register Settings for PGA

Register (Address)	Register Bits	Bits Name	Bit Values	Comment
SYS0 (03h)	SYS0[6:4]	PGA[2:0]	010	PGA = 4 V/V

3.2 Passive Components

3.2.1 R_{REF}

The value of R_{REF} is selected based on the IDAC setting and the desired V_{REF} voltage of 1.64 V, as shown in Equations (18) – (19).

$$R_{REF} = \frac{V_{REF}}{2 \times I_{IDAC}} \quad (18)$$

$$R_{REF} = \frac{1.64\ V}{2 \times 1\ mA} = 820\ \Omega \quad (19)$$

An 820 Ω R_{REF} resistor was chosen based on the results of Equation (19). Since the voltage across the R_{REF} sets the reference voltage for the ADC, the tolerance and temperature drift of R_{REF} directly affect the measurement gain error as shown in Section 4.2.2.1 and Appendix A.5.1. To meet the un-calibrated accuracy requirement of 0.1 Ω (or 0.027% of the full-scale resistance range), a resistor with 0.02% maximum tolerance was selected.

Note that, as with any amplifier, it is necessary to ensure that the input voltage stays within the specified common-mode input range listed in the device datasheet specification table. The common-mode input voltage (V_{CM}) to the PGA must stay within the range shown in Equation (20) based on the maximum RTD voltage.

$$AVSS + 0.1\ V + \frac{V_{IN\_MAX} \times Gain}{2} \le V_{CM} \le AVDD - 0.1\ V - \frac{V_{IN\_MAX} \times Gain}{2}$$

$$881\ mV \le V_{CM} \le 2.42\ V \quad (20)$$

For the IDACs to remain operational, the AIN0 and AIN3 inputs of the ADS1247 must satisfy the IDAC compliance voltage found in the ADS1247 datasheet (see Equation (21)). The largest voltage will be seen at AIN0 as it equals the sum of the common-mode voltage and the maximum RTD voltage shown in Equation (22).

$$AIN0 \le AVDD - 0.7\ V = 2.6\ V \quad (21)$$

$$AIN0 = V_{CM} + V_{IN\_MAX} = 1.64\ V + 390.48\ mV = 2.03\ V \quad (22)$$

In this ratiometric configuration, V_{REF} sets the input common-mode voltage at 1.64 V, satisfying the requirements for both the input common-mode voltage and the IDAC compliance voltage of the ADS1247.

3.2.2 Input and Reference Low-Pass Filters

The differential filters chosen for this application were designed to have a -3 dB corner frequency at least 10 times larger than the bandwidth of the ADC. The selected ADS1247 sampling rate of 20 SPS results in a -3dB bandwidth of 14.8 Hz. The -3dB filter corner frequency was set to be roughly 250 Hz at mid-scale measurement resistance. For proper operation, the differential cutoff frequencies of the reference and input low-pass filters must be well matched. This can be difficult because as the resistance of the RTD changes over the span of the measurement, the filter cutoff frequency changes as well. To mitigate this effect, the two resistors used in the input filter (R_{I1} and R_{I2}) were chosen to be two orders of magnitude larger than the RTD. Input bias currents of the ADC will cause a voltage drop across the filter resistors that will show up as a differential offset error if the bias currents and/or filter resistors are not equal. Limiting the resistors to at most 20 kΩ will reduce dc offset errors due to input bias current.

$$R_{I1} = R_{I2} = 9.09\ k\Omega \quad (23)$$

The input filter differential capacitor (C_{I_DIFF}) can be calculated as shown in Equation (24).

$$f_{-3dB\_DIFF} = \frac{1}{2 \times \pi \times C_{I\_DIFF} \times (R_{I1} + R_{RTD} + R_{I2})} \quad (24)$$

$$C_{I\_DIFF} \approx 33 \text{ nF}$$

To ensure that mismatch of the common-mode filtering capacitors is not translated to a differential voltage, the common-mode capacitors (C_{I_CM1} and C_{I_CM2}) were chosen to be ten times smaller than the differential capacitor, making them 3.3 nF each. This results in a common-mode cutoff frequency that is roughly twenty times larger than the differential filter, making the matching of the common-mode cutoff frequencies less critical.

$$C_{I\_CM1} = C_{I\_CM2} = 3.3 \text{ nF} \quad (25)$$

$$f_{-3dB\_CM+} = \frac{1}{2 \times \pi \times C_{I\_CM1} \times (R_{I1} + R_{RTD} + R_{REF})} \quad (26)$$

$$f_{-3dB\_CM+} = 4.76 \text{ kHz}$$

$$f_{-3dB\_CM-} = \frac{1}{2 \times \pi \times C_{IN\_CM2} \times (R_{I2} + R_{REF})} \quad (27)$$

$$f_{-3dB\_CM-} = 4.87 \text{ kHz}$$

The differential reference filter is designed to have a -3 dB corner frequency of 250 Hz to match the differential input filter. The two reference filter resistors were selected to be 20 kΩ, several times larger than the value of R_{REF}. The reference filter resistors should not be sized larger than 20 kΩ or dc bias errors will become significant.

$$R_{R1} = R_{R2} = 20 \text{ k}\Omega \quad (28)$$

The differential capacitor for the reference filter can be calculated as shown in Equation (29).

$$f_{-3dB\_DIFF} = \frac{1}{2 \times \pi \times C_{R\_DIFF} \times (R_{R1} + R_{REF} + R_{R2})} \quad (29)$$

$$C_{R\_DIFF} \approx 15 \text{ nF}$$

To ensure that mismatch of the common-mode filtering capacitors is not translated to a differential voltage, the reference common-mode capacitors (C_{R_CM1} and C_{R_CM2}) were chosen to be ten times smaller than the reference differential capacitor, making them 1.5 nF each. Again, the resulting cutoff frequency for the common-mode filters is roughly twenty times larger than the differential filter, making the matching of the cutoff frequencies less critical.

$$C_{R\_CM1} = C_{R\_CM2} = 1.5 \text{ nF} \quad (30)$$

$$f_{-3dB\_CM+} = \frac{1}{2 \times \pi \times C_{R\_CM1} \times (R_{R1} + R_{REF})} \quad (31)$$

$$f_{-3dB} = 5.10 \text{ kHz}$$

$$f_{-3dB\_CM-} = \frac{1}{2 \times \pi \times C_{R\_CM2} \times R_{R2}} \quad (32)$$

$$f_{-3dB} = 5.31 \text{ kHz}$$

3.3 Low-Dropout (LDO) Linear Regulator

The RTD acquisition board in this design interfaces with an external PC GUI through a USB interface board to post-process the ADC digital output and display the temperature result. Power for the acquisition board comes from the USB power supply rail (V_{DUT}). This supply may be passed through a high-PSRR low-dropout regulator (LDO) to create the AVDD and DVDD supplies and to avoid inaccuracies due to power supply noise.

The TPS7A4901 comes from a series of high-voltage, ultra-low noise LDOs that are ideal for precision applications. A resistor divider at the LDO output sets the output voltage (V_{LDO_OUT}) proportional to the LDO's internal reference voltage (V_{LDO_REF}). For this device, V_{LDO_REF} = 1.188 V. In order to set V_{LDO_OUT} to the desired output voltage of 3.3 V, the resistor divider components are selected using Equation (33).

$$V_{LDO\_OUT} = V_{LDO\_REF}\left(1 + \frac{R1}{R2}\right) \quad (33)$$

$$R1 = 140 \text{ k}\Omega$$

$$R2 = 78.7 \text{ k}\Omega$$

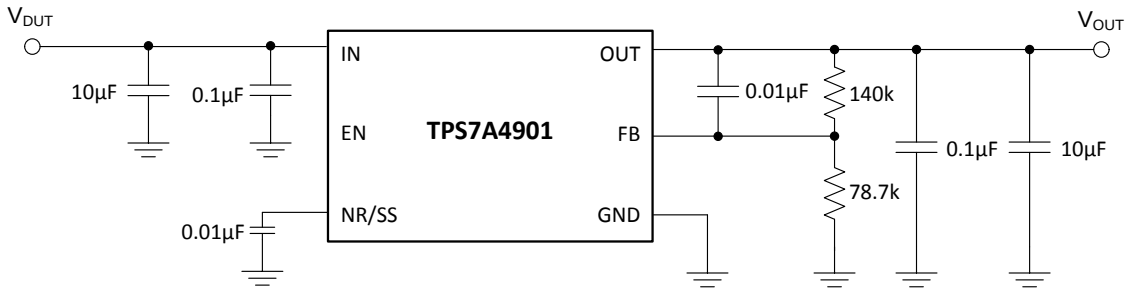

Figure 8. LDO Configuration for +3.3 V Output

4 Simulation and Error Calculation

4.1 Simulation

Figure 9 shows the TINA-TI™ circuit used to simulate the behavior of the RTD, input filtering, and PGA in this system. The RTD has been modeled with a Pt100 macromodel that converts an input voltage representative of the RTD temperature into the correct output resistance using the CVD equations. The simplified ADS1247 PGA does not accurately represent the internal circuitry to the ADC; however, it does represent the ideal behavior of the internal PGA.

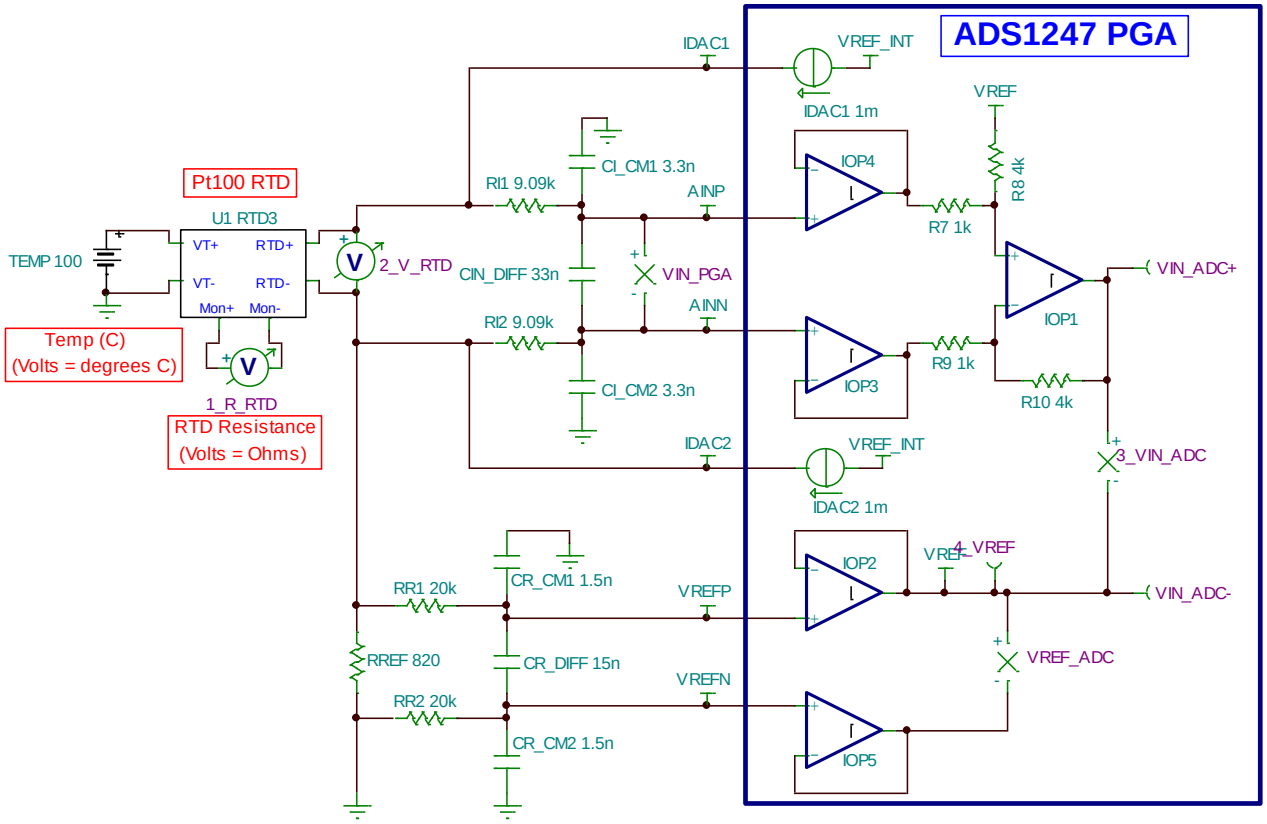

Figure 9. TINA-TI™ Simulation Circuit for the RTD and ADS1247 Inputs

4.1.1 RTD Transfer Function

Figure 10 displays the RTD resistance, RTD voltage, ADC input voltage, and the V_{REF} voltage as the RTD temperature is swept from -200°C to 850°C. The results are displayed on the image for the minimum, mid-scale, and maximum temperatures. The RTD voltage spans from 18.51 mV to 390.48 mV and with the PGA set to 4 V/V, the differential ADC input is from 74.03 mV to 1.56 V. The V_{REF} voltage is also displayed and is the expected value of 1.64 V.

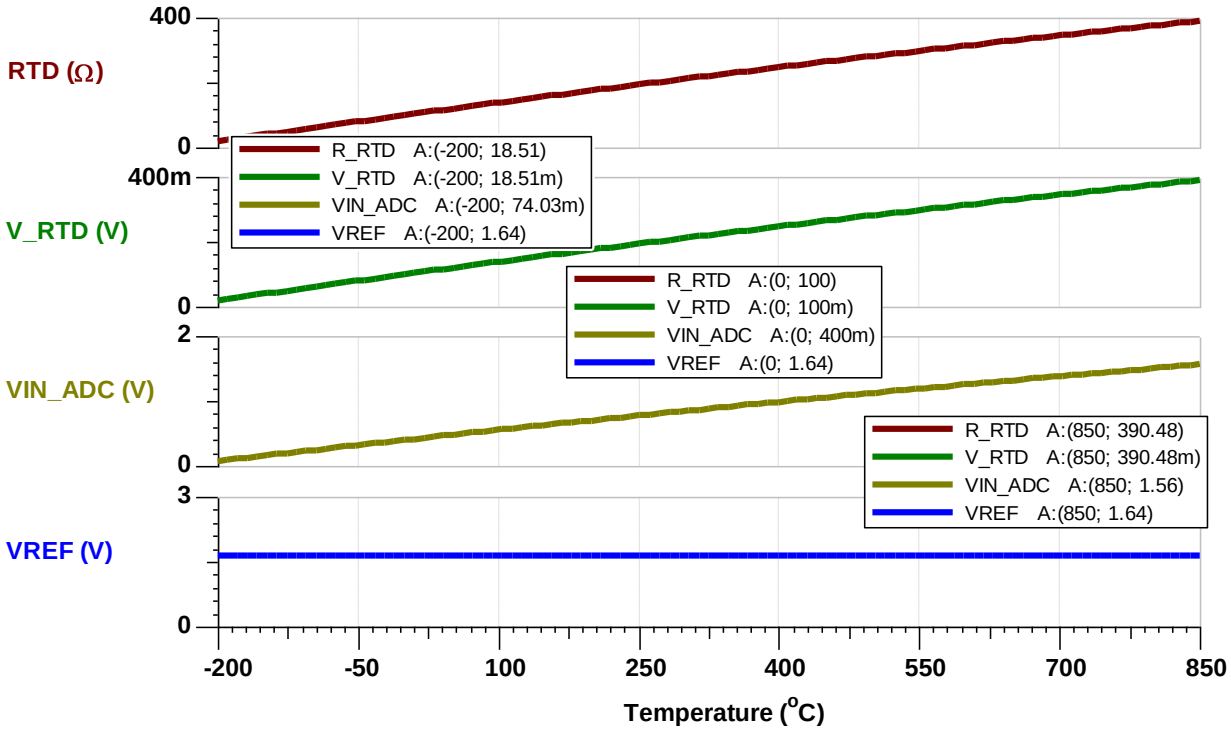

Figure 10. RTD, ADC, and V_{REF} from -200°C to 850°C

4.1.2 Low-pass Filter Response

The frequency response of the input and reference filters was tested using an ac current generator in place of the IDAC1 source and is shown in Figure 11. The -3 dB cutoff frequency of the filters is roughly 20 Hz different when the RTD is at the maximum value near 390 Ω. The dc magnitude of the results is based on the current-to-voltage transfer function (I*R) as the excitation currents pass through the passive resistors in the signal chain.

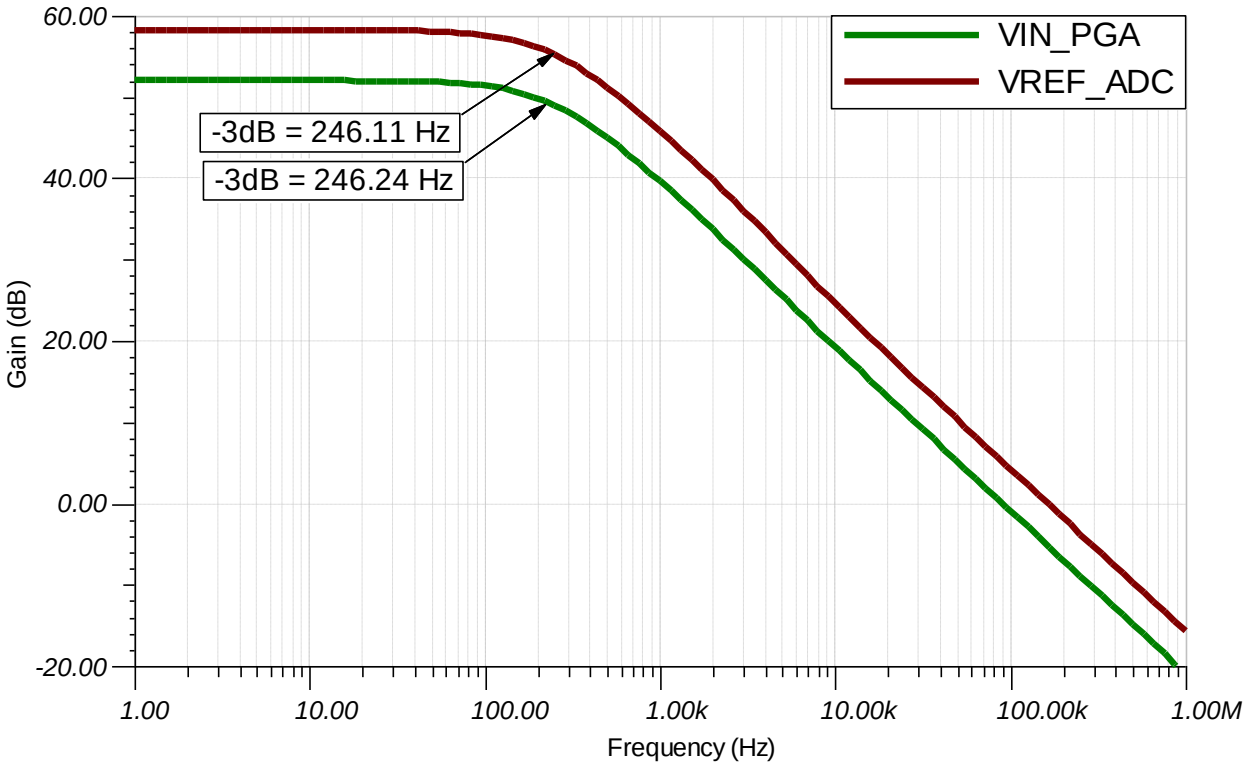

Figure 11. Simulated Filter Frequency Response

4.2 Error Calculations

4.2.1 Measurement Resolution

The smallest signal an n-bit data converter can theoretically resolve is given by its LSB size (least-significant bit). An increase in input voltage by one LSB will increment the ADC output by one code. Equation (34) calculates the weight of one LSB referred to the input of the PGA using V_{REF}, Gain, and the number of codes.

$$LSB(V) = \frac{2 \times V_{REF}}{Gain \times 2^n} = \frac{2 \times 1.64\ V}{4\ \frac{V}{V} \times 2^{24}} = 48.88\ nV \quad (34)$$

To calculate the theoretical achievable code step size in terms of resistance, divide the LSB size by the excitation current used to excite the RTD, as shown in Equation (35).

$$LSB(\Omega) = \frac{LSB(V)}{I_{IDAC}} = \frac{48.88\ nV}{1\ mA} = 48.88\ \mu\Omega \quad (35)$$

Since the input-referred peak-to-peak noise of the ADS1247 at 20 SPS and Gain = 4 V/V is greater than one LSB, a more appropriate resolution calculation replaces the converter LSB weight with the input-referred noise specification. The ADC datasheet will typically provide the input-referred noise (in μV_{PP} or μV_{RMS}) for different supply voltages, reference voltages, data rates, and gain settings.

The ADS1247 input-referred noise specification for the closest configuration to this system is 5.94 μV_{PP} (see Table 5 in the ADS1247 datasheet). Equation (36) calculates the ADC resistance measurement resolution based on the input-referred peak-to-peak noise ($Noise_{RTI\_pp}$). The $Noise_{RTI\_pp}$ value is divided by factor of two to show the resolution as a deviation from the mean value.

$$ADC_{RES}(\Omega) = \pm\frac{(Noise_{RTI\_pp}/2)}{I_{IDAC}} = \pm\frac{(5.94\ \mu V_{PP}/2)}{1\ mA} = \pm 2.97\ m\Omega \quad (36)$$

The expected temperature resolution in degrees Celsius can be calculated by dividing the expected resistance resolution by the RTD sensitivity (α) as shown in Equation (37). Appendix A.4 explains how the value of α changes over the RTD measurement temperature, ranging from 0.4323 Ω/°C at -200°C to 0.2927 Ω/°C at 850°C. Therefore, the temperature resolution will vary over the RTD temperature range, even though the resistance measurement resolution will remain constant.

Equation (37) calculates the ADC resolution in degrees Celsius using the Pt100 sensitivity at 0°C.

$$ADC_{RES@0°C}(°C) = \frac{ADC_{RES}(\Omega)}{\alpha_{@0°C}} = \frac{\pm 2.97\ m\Omega}{0.39083\ \frac{\Omega}{°C}} = \pm 0.0076°C \quad (37)$$

4.2.2 Measurement Accuracy

The expected accuracy of the design can be calculated using the specifications of the components selected in Section 3. The units associated with these specifications range from volts, to percent full-scale range (%FSR), to parts-per-million of full-scale (ppm). In order to calculate the total error, these different errors sources must be converted to a common unit of measurement. In the following calculations, all specifications will be converted to volts referred to the input (RTI) of the ADS1247.

Gain errors will be referenced to the maximum differential input voltage, V_{IN_MAX} = 390.48 mV (calculated in Equation (16) in Section 3.1.3), to properly calculate the input-referred voltage errors.

4.2.2.1 Errors due to R_{REF}

The tolerance of R_{REF} will produce gain errors in the ADC transfer function as derived in Appendix A.6.

Assuming the tolerance is specified as a percentage, the transfer function gain error from the R_{REF} tolerance can be calculated from Equations (38) – (39).

$$R_{REF\ Tol}(\%) = 0.02\% \quad (38)$$

$$\text{Gain Error}_{R_{REF}\ Tol}(\%) = \frac{R_{REF\ Tol}(\%)}{R_{REF\ Tol}(\%) + 100} \times 100 = \frac{0.02}{0.02 + 100} \times 100 = 0.019996\% \quad (39)$$

The error in volts due to the R_{REF} tolerance can be calculated from the gain error and the maximum input voltage.

$$\text{Gain Error}_{R_{REF}\ Tol}(V) = \frac{\text{Gain Error}_{R_{REF}\ Tol}(\%)}{100} \times V_{IN\_MAX} \quad (40)$$

$$\text{Gain Error}_{R_{REF}\ Tol}(V) = \frac{0.019996}{100} \times 390.48 mV = 78.0804\ \mu V$$

4.2.2.2 Errors due to ADS1247

The ADS1247 will cause errors due to the offset voltage, offset voltage drift, gain error, gain error drift, integral nonlinearity (INL), and IDAC matching.

Offset voltage error and offset voltage error drift are commonly specified in an input-referred voltage and can be directly entered from the device performance datasheet, if provided.

$$\text{Offset Error}_{ADC}(V) = 15\ \mu V \quad (41)$$

Gain errors are usually specified as a percentage of the full-scale ADC input range (%FSR), so the input-referred voltage error can be calculated by multiplying by V_{IN_MAX}. Equation (42) uses the typical gain error of the ADS1247, but similar errors can be calculated using the maximum specifications as well.

$$\text{Gain Error}_{ADC}(V) = \frac{\text{Gain Error}_{ADC}(\%)}{100} \times V_{IN\_MAX} = \frac{0.005}{100} \times 390.48\ mV = 19.524\ \mu V \quad (42)$$

The INL is typically specified in either number of ADC codes or in ppm FSR. Because INL is not a gain error, it must be multiplied by the full-scale input voltage of the ADC rather than V_{IN_MAX}, as shown in Equation (43).

$$\text{INL Error}_{ADC}(V) = \frac{\text{INL}}{1{,}000{,}000} \times \frac{2 \times V_{REF}}{\text{Gain}} = \frac{6 \text{ ppm}}{1{,}000{,}000} \times \frac{2 \times 1.64 \text{ V}}{4 \frac{\text{V}}{\text{V}}} = 4.92 \text{ µV} \quad (43)$$

The final errors considered for this system are caused by the mismatching of the IDAC current sources which introduce a gain error in the transfer function as derived in Appendix A.7.

$$\text{Gain Error}_{IDAC}(\%) = \frac{I_{IDAC\ Mismatch}(\%)}{I_{IDAC\ Mismatch}(\%) + 200} \times 100 = \frac{0.15}{0.15 + 200} \times 100 = 0.07494\% \quad (44)$$

$$\text{Gain Error}_{IDAC}(V) = \frac{\text{Gain Error}_{IDAC}(\%)}{100} \times V_{IN\_MAX} = \frac{0.07494}{100} \times 390.48 \text{ mV} = 292.626 \text{ µV} \quad (45)$$

The errors from the mismatch of the IDAC sources are the largest errors in the system. This reinforces the importance of chopping the two IDAC current sources to remove these errors as described in Section 3.1.2.

4.2.2.3 Total Error

With all of the input-referred errors calculated in volts, the total error can be calculated by taking the root-sum-of-square of all of the uncorrelated error terms. A similar calculation can be performed for the maximum error by replacing the typical specifications with the maximum specifications. For cases where a typical specification is not available, the maximum specification is used.

$$\text{Error}_{Total}(V) = \sqrt{\begin{matrix}\text{Gain Error}_{R_{REF}\ Tol}^{\ 2} + \text{Offset Error}_{ADC}^{\ 2} + \text{Gain Error}_{ADC}^{\ 2} \\ + \text{INL Error}_{ADC}^{\ 2} + \text{Gain Error}_{IDAC}^{\ 2}\end{matrix}} \quad (46)$$

$$\text{Error}_{Total}(V) = 303.903 \text{ µV}$$

The system errors and their resulting input-referred error in µV are summarized in Table 4.

Table 4. Summary of Error Sources and Resulting Voltage Error RTI

Error Source	Value		Error RTI (µV)	
	Typ	Max	Typ	Max
R_{REF} Errors				
R_{REF} Tolerance	-	0.02%	-	78.1
ADS1247 Errors				
Integrated Nonlinearity (INL)	6 ppm	15 ppm	4.92	12.3
Offset Voltage	-	15 µV	-	15
Gain Error	0.005%	0.02%	19.52	78.1
IDAC Mismatch	-	0.15%	-	292.6

After removing the IDAC mismatch errors with chopping, a two-point gain and offset calibration can remove the errors from the R_{REF} tolerance, offset voltage, and gain error, leaving only the error from INL. Table 5 compares the original unadjusted error with the errors after IDAC chopping and a two-point calibration.

Table 5. Total Error Voltage RTI

	Total Error RTI (µV)	
	Typ	Max
Unadjusted Error at 25°C	303.9	313.4
Unadjusted Error at 25°C with IDAC Chop	82.02	112.1
Calibrated Error at 25°C	4.92	12.3

The magnitude of the IDAC source can be used to convert the calculated voltage error into a calculated resistance error as shown in Equation (47). The results from Table 5 have been converted to resistance accuracy in Table 6.

$$\text{Error } (\Omega) = \frac{\text{Error } (\mu V)}{I_{IDAC}\ (\mu A)} \quad (47)$$

Table 6. Total Error Resistance

	Total Error RTI (Ω)	
	Typ	Max
Unadjusted Error at 25°C	0.304	0.313
Unadjusted Error at 25°C with IDAC Chop	0.082	0.112
Calibrated Error at 25°C	0.0049	0.012

The temperature accuracy can be calculated by dividing the resistance accuracy by the RTD sensitivity (α) at the desired calibration temperature. The RTD sensitivity is worst at 850°C (see Appendix A.4). The results in Table 7 display the Total Error in degrees Celsius at 0°C.

$$\text{Error } (°C) = \frac{\text{Error } (\Omega)}{\alpha_{@\,0°C}} \quad (48)$$

Table 7. Total Error Temperature

	Total Error (°C)	
	Typ	Max
Unadjusted Error at 25°C	0.778	0.801
Unadjusted Error at 25°C with IDAC Chop	0.21	0.287
Calibrated Error at 25°C	0.013	0.031

Table 8 compares the calculated performance with the design goals from Table 1. It is necessary to chop the IDAC sources to meet the desired un-calibrated precision resistance measurement accuracy.

Table 8. Comparison of Design Goals and Calculated Performance

	Goal	Calculated
Unadjusted Resistance Measurement Accuracy	±0.1 Ω	±0.082 Ω
Calibrated Resistance Measurement Accuracy	±0.01925 Ω	±0.0049 Ω
Calibrated Temperature Measurement Accuracy	±0.05°C	±0.013°C

5 PCB Design

Providing proper power supply decoupling, grounding, and minimizing cross-over between the analog and digital circuitry return currents is required to achieve optimal performance in all mixed-signal PCB designs. In addition to standard practices, minimizing or balancing PCB trace resistance is a primary concern because the design is based on accurately measuring the resistance of the RTD. Implementing a 4-wire Kelvin connection at the RTD and R_{REF} resistors help to minimize PCB resistance in series with the sense elements by separating the measurement sense and excitation current paths.

As discussed in Section 2.2.2, the lead resistances of the 3-wire RTD are effectively cancelled when they are equal and the magnitude of the excitation current sources are also equal. The same theory applies to PCB trace resistance in series with the three RTD leads. Therefore, the PCB trace resistances connecting the IDAC and ADS1247 inputs to the RTD must be balanced, otherwise additional differential signals will be formed. The resistance of the trace between the terminal block and the R_{REF} resistor is common to both the positive and negative inputs and is cancelled by taking a differential measurement. Balancing the RTD trace resistance is accomplished by creating traces of equal length between the terminal block and the ADS1247connection points. Figure 12 displays these critical PCB layout areas. The full PCB layout is shown in Figure 13.

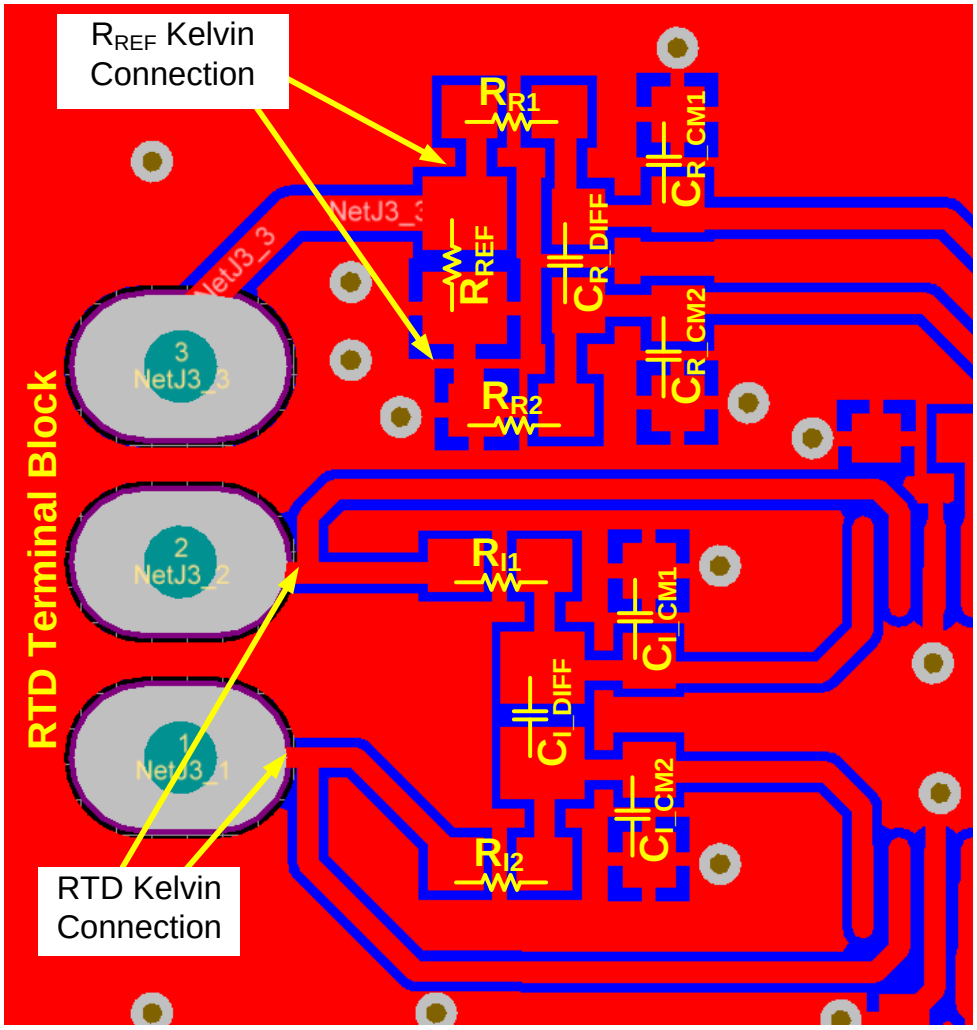

Figure 12. PCB Layout Highlighting Important PCB Layout Concerns

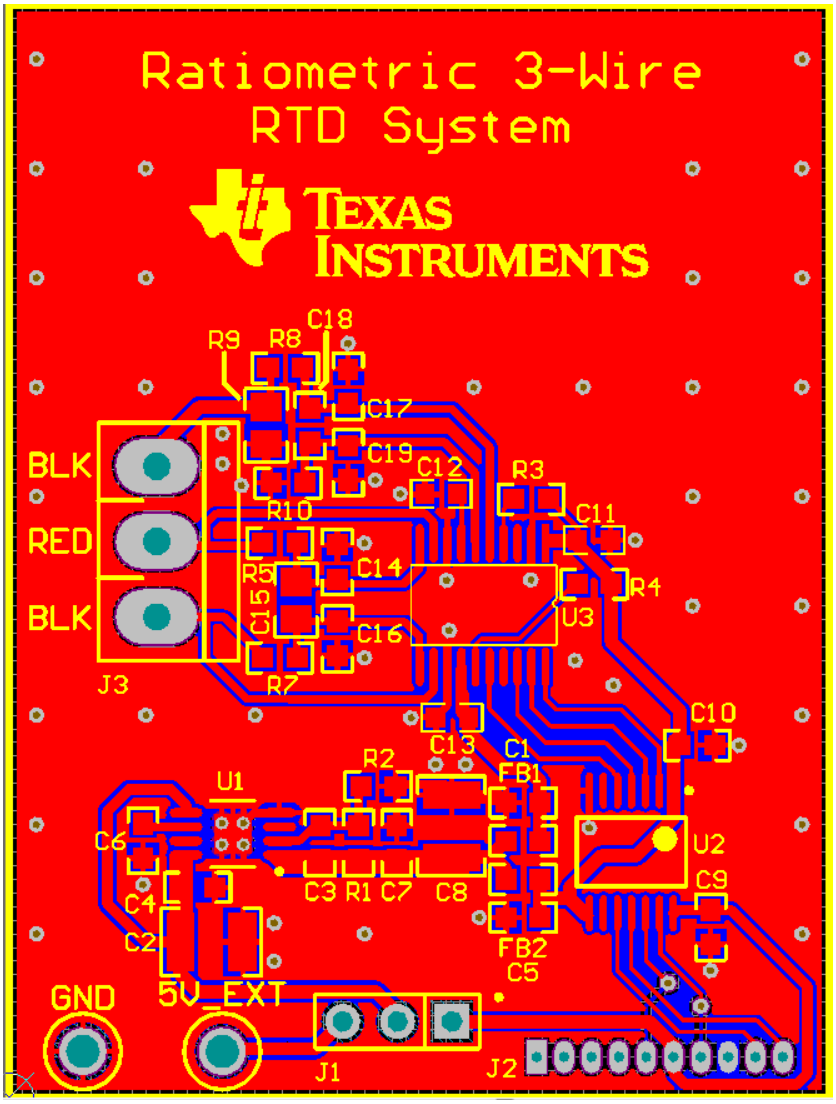

Figure 13. Full PCB Layout

6 Verification & Measured Performance

6.1 Measured Transfer Function with Precision Resistor Input

To test the accuracy of only the acquisition circuit, a series of calibrated high-precision discrete resistors were used as the input to the system. Figure 14 displays the unadjusted resistance measurement accuracy of the system over an input span from 20 Ω to 400 Ω. The offset error can be attributed to the offset of the ADC, while the gain error can be attributed to the accuracy of the R_{REF} resistor and the ADC. A linear curve-fit has been applied to the results yielding the system gain and offset errors displayed in Figure 14.

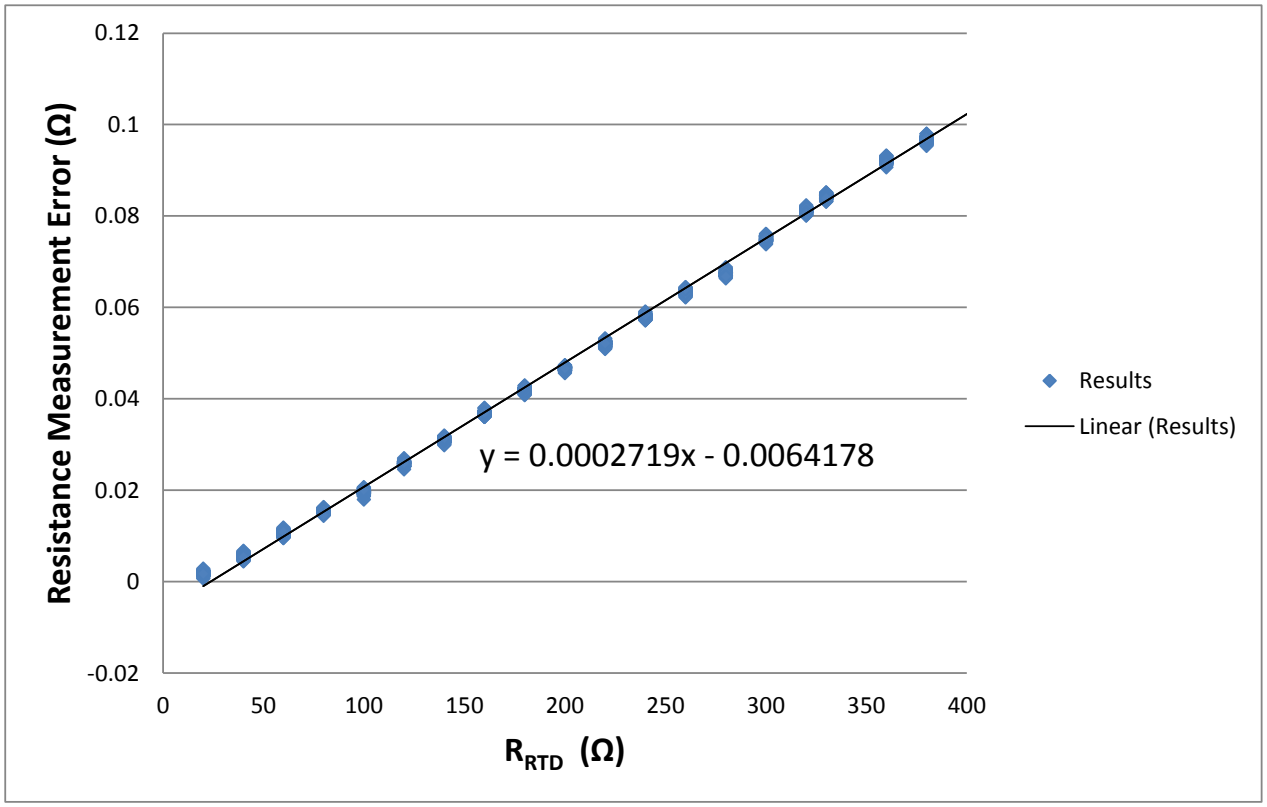

Figure 14. Resistance Measurement Results with Precision Resistors Before Calibration

Precision temperature measurement applications are typically calibrated to remove the effects of gain and offset errors, which generally dominate the total system error. The simplest calibration method is a linear, or two-point, calibration which applies an equal and opposite gain and offset term to cancel the measured system gain and offset errors. Applying a gain and offset calibration yields the calibrated results shown in Figure 15. More information regarding calibration can be found in Reference 5.

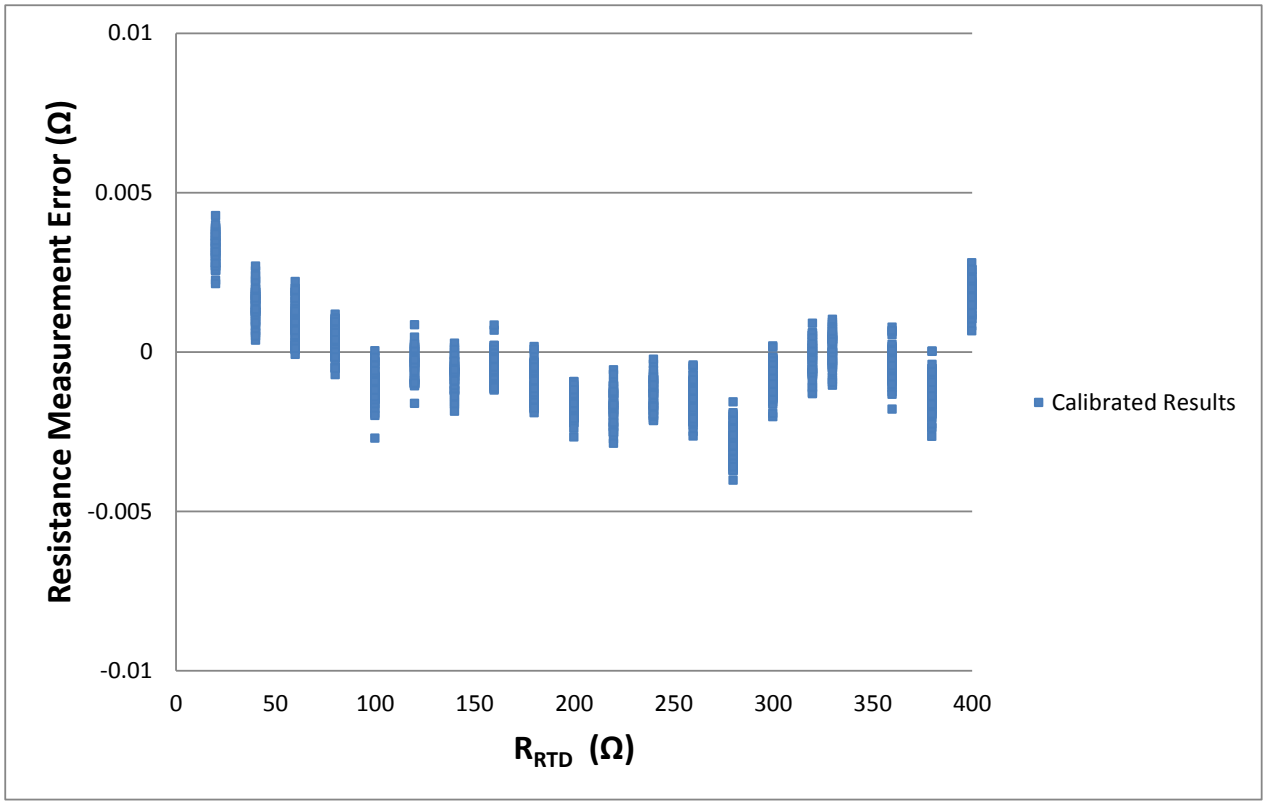

Figure 15. Resistance Measurement Results with Precision Resistors after Calibration

The results in Figure 15 can be converted to temperature accuracy by dividing the results by the RTD sensitivity (α) at the measured resistance. Over the full resistance input range, the maximum total measured error is ±0.00415 Ω. Equation (49) uses this measurement and the RTD sensitivity at 0°C to calculate the measured temperature accuracy.

$$\text{Error } (^{\circ}\text{C}) = \frac{\text{Error } (\Omega)}{\alpha_{@0^{\circ}\text{C}}} = \frac{\pm 0.00415\ \Omega}{0.39083\ \frac{\Omega}{^{\circ}\text{C}}} = \pm 0.0106^{\circ}\text{C} \quad (49)$$

Figure 16 displays the calculated temperature accuracy of the circuit, not including any linearization related errors of the RTD.

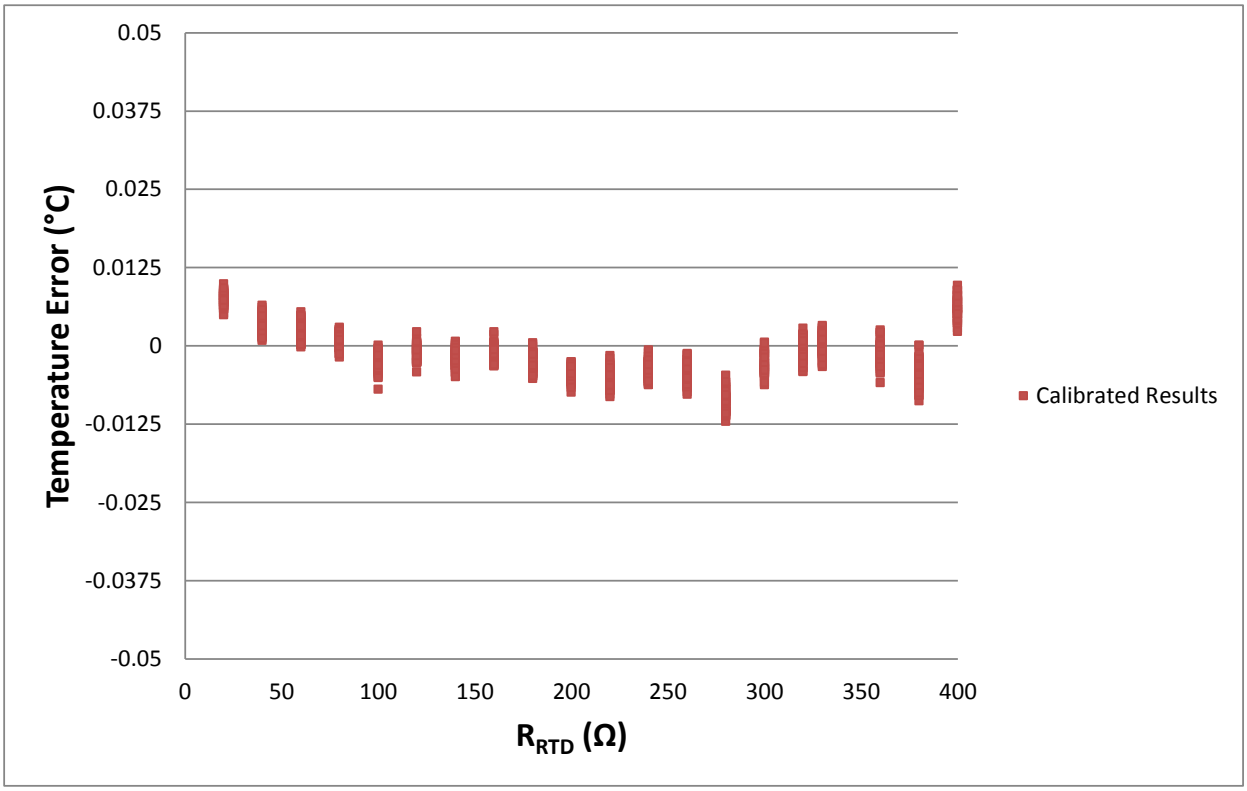

Figure 16. Calculated Temperature Error from Resistance Measurement Error

6.2 Noise Histogram

The peak-to-peak noise of the acquisition system can be approximated from an output code histogram. The RTD was replaced with a 220 Ω, 0.01% 0.05ppm/°C precision resistor, to represent the RTD resistance near mid-scale. Then 1,000 samples were recorded to generate the histogram plot shown in Figure 17. The peak-to-peak voltage deviation in the histogram is roughly 3.45 μV_{PP}. The measured noise is less than the value specified in the ADS1247 datasheet of 5.94 μV_{PP} for a 3.3 V supply and a 2.048 V internal reference; however, the datasheet specifications do not exactly match this configuration.

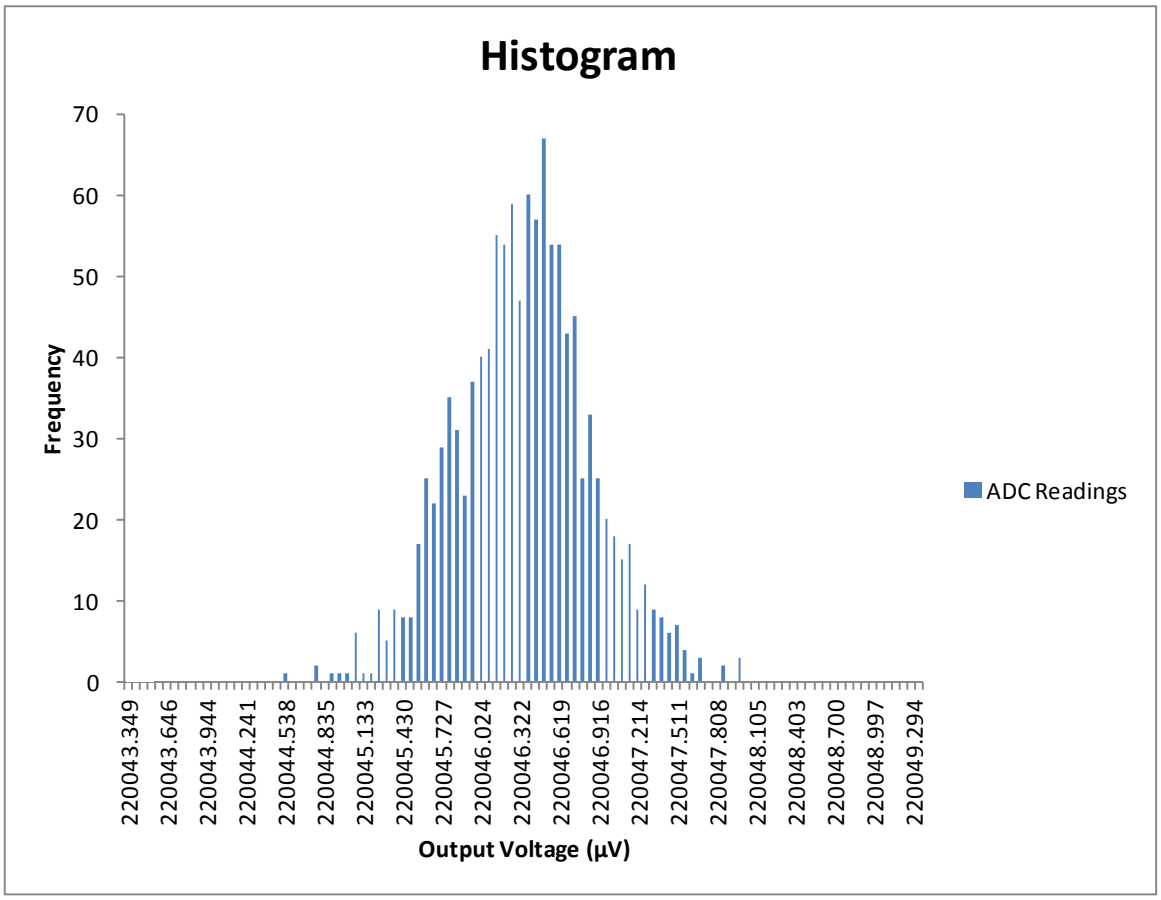

Figure 17. Histogram with R_{RTD} = 220 Ω

Enter the measured input-referred noise into Equation (50) to determine the measured resolution in Ohms.

$$ADC_{RES}(\Omega) = \pm\frac{(Noise_{RTI\_pp}/2)}{I_{IDAC}} = \pm\frac{(3.45\ \mu V_{PP}/2)}{1\ mA} = \pm 1.725\ m\Omega \quad (50)$$

The expected temperature resolution in degrees Celsius can be calculated by dividing the expected resistance resolution by the RTD sensitivity (α) at 0°C as shown in Equation (51).

$$ADC_{RES@0°C}(°C) = \frac{ADC_{RES}(\Omega)}{\alpha_{@0°C}} = \frac{\pm 1.725\ m\Omega}{0.39083\ \frac{\Omega}{°C}} = \pm 0.0044°C \quad (51)$$

The temperature resolution falls well within the accuracy goal of ±0.05°C and can be observed in the results in Figure 16. The noise can be further reduced by applying additional averaging or filtering in software.

Table 9 compares the measured performance with the calculated performance and design goals from Table 8. It is necessary to chop the IDAC sources to meet the desired un-calibrated precision resistance measurement accuracy.

Table 9. Comparison of Design Goals, Calculated, and Measured Performance

	Goal	Calculated	Measured
Unadjusted Resistance Measurement Accuracy	±0.1 Ω	±0.082 Ω	±0.096 Ω
Calibrated Resistance Measurement Accuracy	±0.01925 Ω	±0.0049 Ω	±0.00415 Ω
Calibrated Temperature Measurement Accuracy	±0.05°C	±0.013°C	±0.0106°C

7 Modifications

This design can be easily modified for other RTD types and temperature ranges by changing the IDAC, PGA, and R_{REF} selections using the equations shown in the theory and component selection sections.

There are a few other fully integrated products available from TI that offer the same required building blocks as the ADS1247 but feature different performance, channel count, and cost. Several of these devices are listed in Table 10.

Table 10. Alternate Fully-Integrated ADC Solutions

ADC	Resolution	Differential Inputs	PGA Range	IDACs Magnitude	Noise	Power Consumption
ADS1147(1)	16	2	1 – 128 V/V	50 µA – 1.5 mA	15.63 μV_{RMS}	1.4 mW
ADS1247(1)	24	2	1 – 128 V/V	50 µA – 1.5 mA	1.07 μV_{RMS}	1.4 mW
ADS1148(1)	16	4	1 – 128 V/V	50 µA – 1.5 mA	15.63 μV_{RMS}	1.4 mW
ADS1248(1)	24	4	1 – 128 V/V	50 µA – 1.5 mA	1.07 μV_{RMS}	1.4 mW
ADS1120(1)	16	2	1 – 128 V/V	10 µA – 1.5 mA	15.63 μV_{RMS}	1.4 mW
ADS1220(1)	24	2	1 – 128 V/V	10 µA – 1.5 mA	1.15 μV_{RMS}	1.4 mW
LMP90100(2)	24	4	1 – 128 V/V	100 µA – 1 mA	4.29 μV_{RMS}	5.1 mW

(1) AVDD = 3.3 V, AVSS = 0 V, Internal Reference = 2.048 V, Data Rate = 20 SPS, PGA = 4 V/V

(2) AVDD = 3 V, AVSS = 0 V, Internal Reference = 3 V, Data Rate = 13.42 SPS, PGA = 4 V/V

Table 11 features other suitable ADC solutions that offer integrated PGAs.

Table 11. Alternate ADC + PGA Solutions

ADC	Resolution	Differential Inputs	PGA Range	Noise	Power Consumption
ADS1146(1)	16	1	1 – 128 V/V	15.63 μV_{RMS}	1.4 mW
ADS1246(1)	24	1	1 – 128 V/V	1.07 μV_{RMS}	1.4 mW
LMP90099(2)	24	4	1 – 128 V/V	4.29 μV_{RMS}	5.1 mW

(1) AVDD = 3.3 V, AVSS = 0 V, Internal Reference = 2.048 V, Data Rate = 20 SPS, PGA = 4 V/V

(2) AVDD = 3 V, AVSS = 0 V, Internal Reference = 3 V, Data Rate = 13.42 SPS, PGA = 4 V/V

Discrete current sources could be comprised of an integrated device such as the REF200 or a circuit such as the designs featured in TIPD101 or TIPD107.

8 About the Authors

Ryan Andrews is an applications engineer with the Precision Analog Delta-Sigma ADC team at Texas Instruments, where he supports industrial and medical products and applications. Ryan received his BS in Biomedical Engineering and his BA in Spanish from the University of Rhode Island.

Collin Wells is an applications engineer in the Precision Linear group at Texas Instruments where he supports industrial products and applications. Collin received his BSEE from the University of Texas, Dallas.

9 Acknowledgements & References

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2. *Robert Burnham and Nagaraj Ananthapadamanabhan, "Example Temperature Measurement Applications Using the ADS1247 and ADS1248" SBAA180, January 2011.*
3. *Collin Wells, "Signal Conditioning and Linearization of RTD Sensors" 2011 Texas Instruments Technology Day Presentation.*
4. *Omega ®, "The Omega ® Temperature Measurement Handbook™ and Encyclopedia, Vol MMXIV™, 7th Edition.*
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Appendix A.

A.1 Electrical Schematic

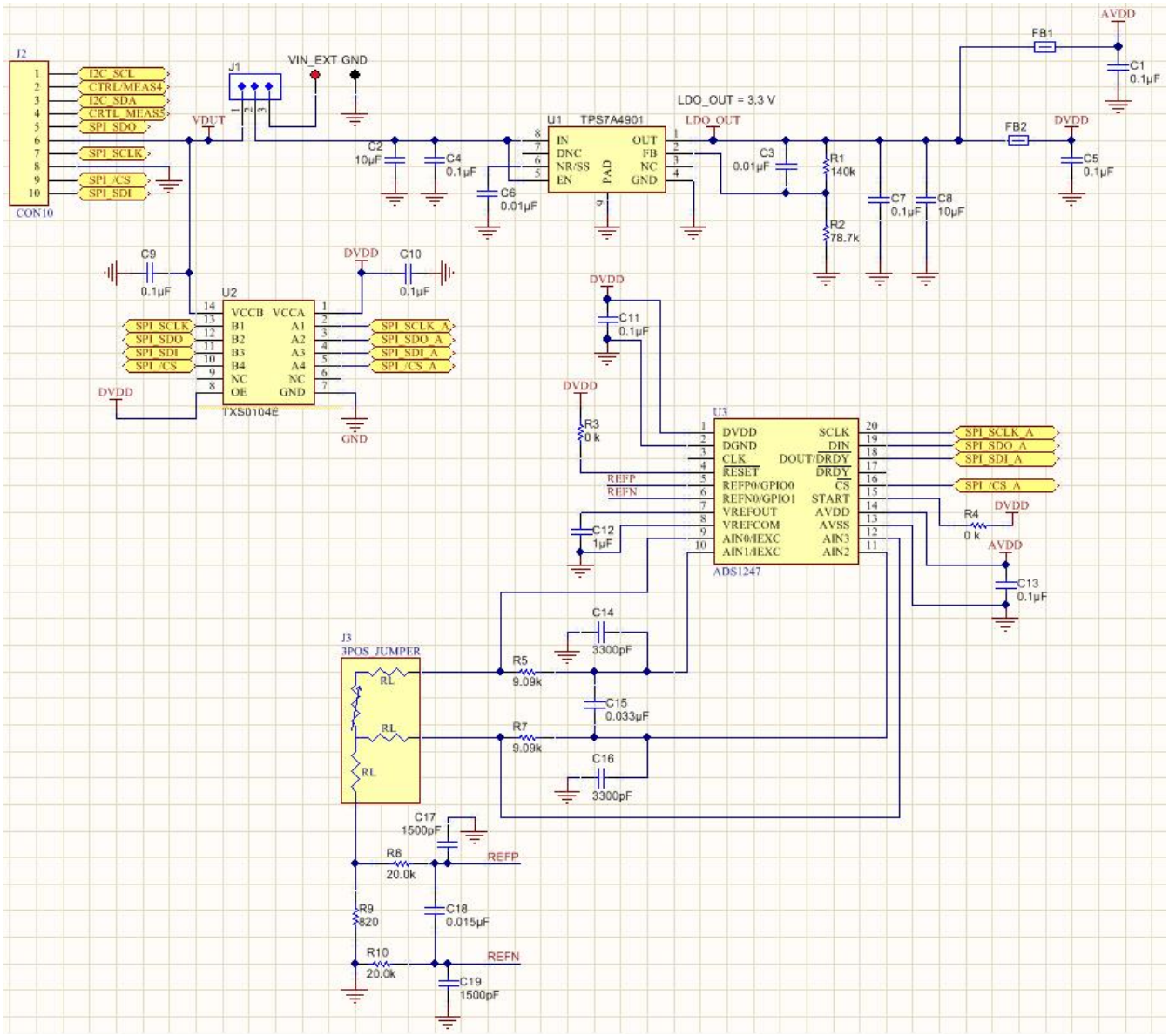

Figure 18. Electrical Schematic

A.2 Bill of Materials

Texas Instruments

Bill of Materials

TI DESIGNS

TIPD120: Ratiometric 3-Wire RTD Acquisition System

Item #	Quantity	Designator	Value	Description	Manufacturer	Part Number
1	8	C1, C4, C5, C7, C9, C10, C11, C13	0.1 µF	CAP CER 0.1UF 50V 10% X7R 0603	MuRata	GRM188R71H104KA93D
2	2	C2, C8	10 µF	CAP CER 10UF 25V 20% X7R 1210	TDK	C3225X7R1E106M250AC
3	2	C3, C6	0.01 µF	CAP CER 10000PF 25V 5% NP0 0603	TDK	C1608C0G1E103J080AA
4	1	C12	1 µF	CAP CER 1UF 25V 10% X7R 0603	Taiyo Yuden	TMK107B7105KA-T
5	2	C14, C16	3300 pF	CAP CER 3300PF 25V 5% NP0 0603	Samsung Electro-Mech	CL10C332JA8NNNC
6	1	C15	0.033 µF	CAP CER 0.033UF 25V 5% NP0 0805	TDK	C2012C0G1E333J125AA
7	2	C17, C19	1500 pF	CAP CER 1500PF 25V 5% NP0 0603	MuRata	GRM1885C1E152JA01D
8	1	C18	0.015 µF	CAP CER 0.015UF 25V 5% NP0 0603	Kemet	C0603C153J3GACTU
9	2	FB1, FB2		FERRITE CHIP 600 OHM 200MA 0603	MuRata	BLM18HG601SN1D
10	1	J1		CONN HEADER 3POS .100" SGL GOLD	Samtec, Inc.	TSW-103-07-G-S
11	1	J2		CONN SOCKET 50PIN .050 R/A SNGL	Mill-Max Manufacturing	851-43-050-20-001000
12	1	J3		TERMINAL BLOCK 3.5MM 3POS PCB	On Shore Technology Inc	ED555/3DS
13	1	R1	140k	RES, 140k ohm, 0.1%, 0.1W, 0603	Yageo America	RT0603BRD07140KL
14	1	R2	78.7k	RES, 78.7k ohm, 0.1%, 0.1W, 0603	Yageo America	RT0603BRD0778K7L
15	2	R3, R4	0	RES 0.0 OHM 1/10W JUMP 0603 SMD	Panasonic Electronic	ERJ-3GEY0R00V
16	2	R5, R7	9.09k	RES, 9.09k ohm, 0.1%, 0.1W, 0603	Susumu Co Ltd	RG1608P-9091-B-T5
17	2	R8, R10	20 k	RES, 20.0k ohm, 0.1%, 0.1W, 0603	Susumu Co Ltd	RG1608P-203-B-T5
18	1	R9	820	RES 820 OHM 1/8W .02% 0805	Susumu	RG2012V-821-P-T1
19	1	TP1		Test Point, TH, Compact, Red	Keystone	5005
20	1	TP2		Test Point, TH, Compact, Black	Keystone	5006
21	1	U1		IC REG LDO ADJ 0.15A 8MSO	Texas Instruments Inc	TPS7A4901DGNR
22	1	U2		IC 4BIT NON-INV TRANSLTR 14TSSOP	Texas Instruments Inc	TXS0104EPWR
23	1	U3		IC ADC 24BIT DEL/SIG LN 20TSSOP	Texas Instruments Inc	ADS1247IPW

Figure 19. Bill of Materials

A.3 ADS1247 Register Settings

Table 12 lists the complete register settings for the ADS1247 used in this design. Registers with values marked as “xx” change based on the internal calibration results specific to every ADS1247.

Table 12. ADS1247 Register Settings

Address	Name	Hex Value
00h	MUX0	0A
01h	VBIAS	00
02h	MUX1	20
03h	SYS0	22
04h	OFC0	xx
05h	OFC1	xx
06h	OFC2	xx
07h	FSC0	xx
08h	FSC1	xx
09h	FSC2	xx
0Ah	IDAC0	96
0Bh	IDAC1	03
0Ch	GPIOCFG	00
0Dh	GPIODIR	00
0Eh	GPIODAT	00

A.4 Pt100 RTD Information

The Pt100 RTD is a platinum-based RTD sensor. Platinum is a noble metal and offers excellent performance over a wide temperature range. Platinum also features the highest resistivity of commonly used RTD materials, requiring less material to create desirable resistance values. The Pt100 RTD has an impedance of 100 Ω at 0°C and roughly 0.385 Ω of resistance change per 1°C change in temperature. The resistance is 18.51 Ω at -200°C and 390.48 Ω at 850°C. Higher-valued resistance sensors, such as Pt1000 or Pt5000, can be used for increased sensitivity and resolution.

Class-A RTDs are a good choice for this application to provide good pre-calibration accuracy and long-term stability. A Class-A RTD will have less than 0.5°C of error at 100°C without calibration and the long-term stability makes accurate infrequent calibration possible. Table 13 displays the tolerance, initial accuracy and resulting error at 100°C for the five main classes of RTDs.

Table 13. RTD Class Tolerance Information

Tolerance Class (DIN-IEC 60751)	Tolerance Values (°C)	Resistance at 0°C (Ω)	Error at 100°C (°C)
AAA(1)	+/- (0.03 + 0.0005*t)	100 +/- 0.012	+/- 0.08
AA	+/- (0.01 + 0.0017*t)	100 +/- 0.04	+/- 0.27
A	+/- (0.15 + 0.002*t)	100 +/- 0.06	+/- 0.35
B	+/- (0.3 + 0.005*t)	100 +/- 0.12	+/- 0.8
C	+/- (0.6 + 0.01*t)	100 +/- 0.24	+/- 1.6

(1) AAA is not included in the DIN-IEC 60751 specification but is an industry accepted tolerance for performance demanding applications.

For positive temperatures the CVD equations is a 2nd-order polynomial Equation (52).

$$RTD(T) = R_0 \times [1 + A(T) + B(T)^2] \quad (52)$$

For negative temperatures from -200°C to 0°C, the CVD equation expands to a 4th-order polynomial shown in Equation (53).

$$RTD(T) = R_0 \times [1 + A(T) + B(T)^2 + C(T)^3 \times (T - 100)] \quad (53)$$

The coefficients in the Calendar Van-Dusen equations are defined by the IEC-60751 standard. R_0 is the resistance of the RTD at 0°C. For a European standard Pt100 RTD the coefficients are:

$$R_0 = 100\ \Omega$$

$$\begin{aligned} A &= 3.9083 \times 10^{-3}\ °C \\ B &= -5.775 \times 10^{-7}\ °C \\ C &= -4.183 \times 10^{-12}\ °C \end{aligned} \quad (54)$$

The change in resistance of a Pt100 RTD from -200°C to 850°C is displayed in Figure 20.

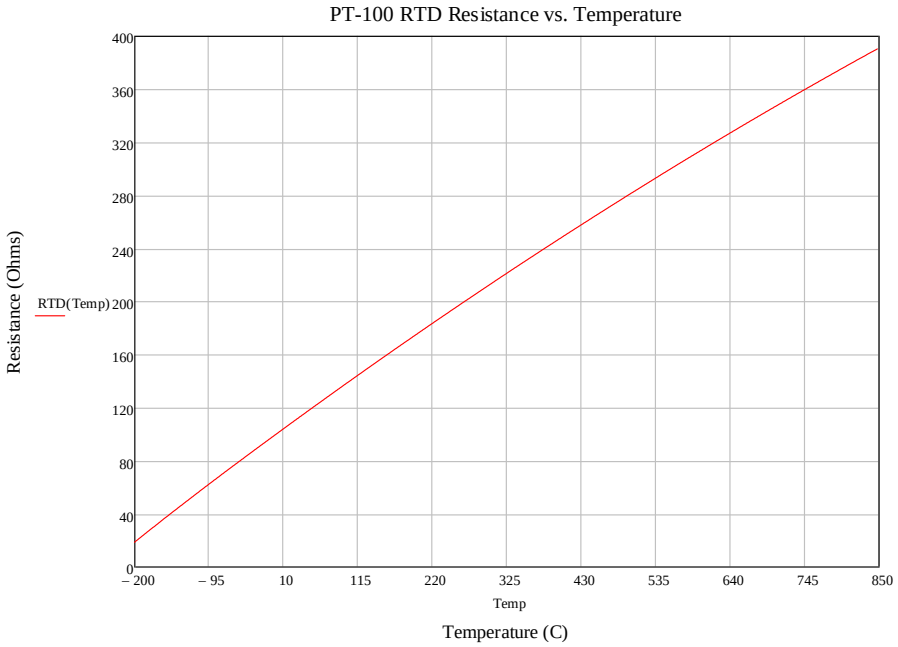

Figure 20. Pt100 RTD Resistance from -200°C to 850°C

While the change in RTD resistance is fairly linear over small temperature ranges, Figure 21 displays the resulting non-linearity if an end-point fit is made to the curve shown in Figure 20. The results show almost 4.5% non-linearity, or greater than 16°C, illustrating the need for digital calibration.

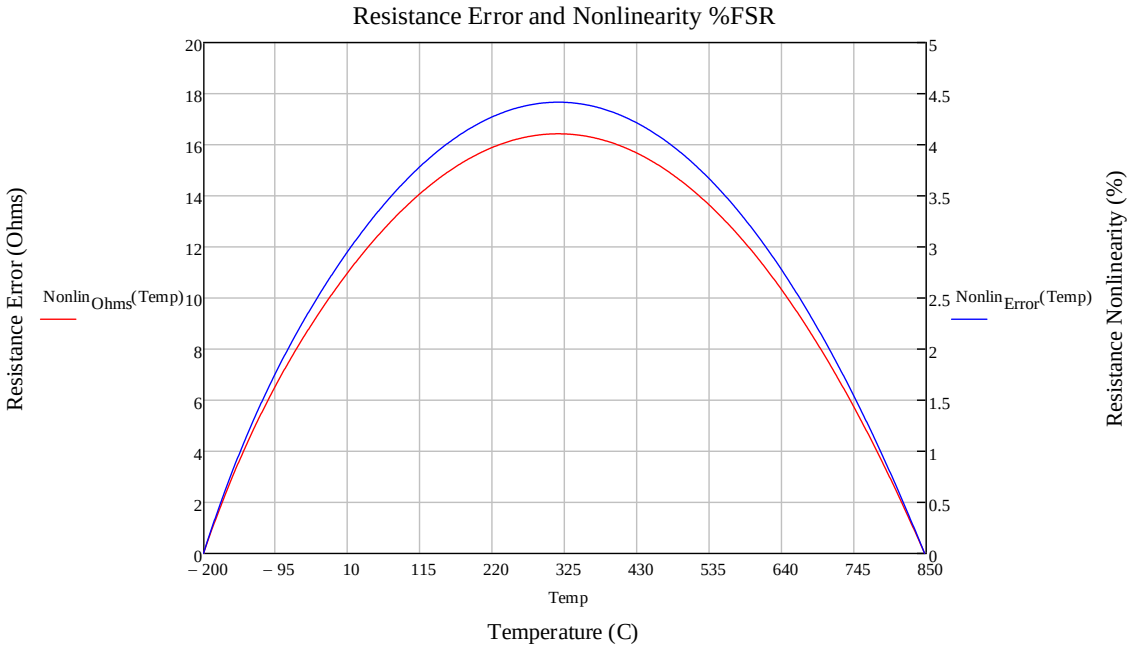

Figure 21. Pt100 RTD Non-Linearity from -200°C to 850°C

Figure 22 displays the change in the sensitivity (α) of the RTD over the full temperature measurement range.

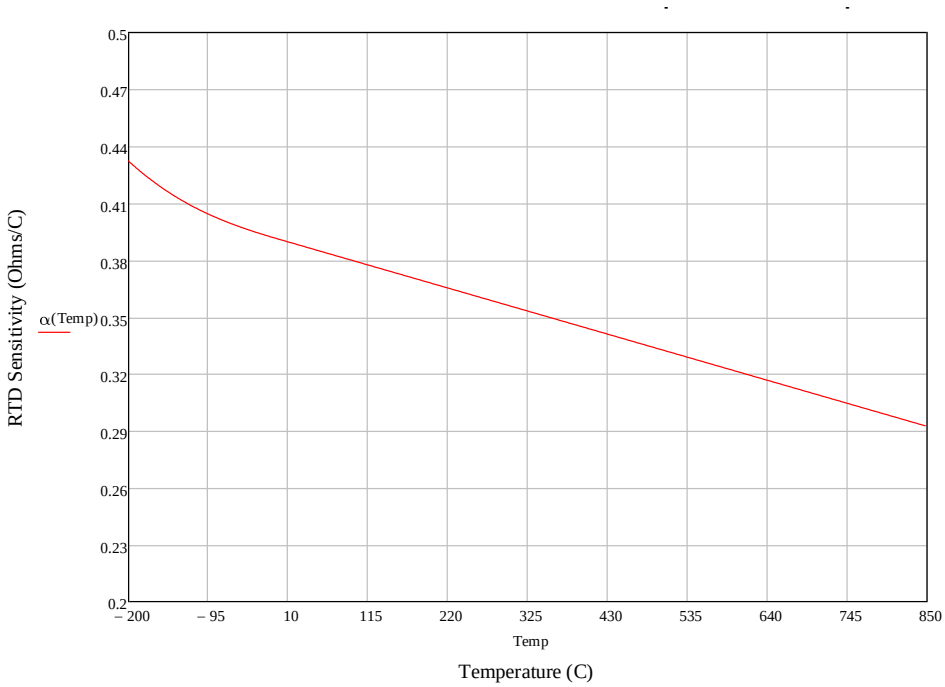

Figure 22: RTD Sensitivity (α) vs. Temperature

The sensitivity of the RTD at a few selected temperatures over the full operating range is listed in Table 14.

Table 14. RTD Sensitivity at Selected Temperatures

Temperature (°C)	α (Ω/°C)
-200	0.43233
-100	0.40531
0	0.39083
100	0.37928
200	0.36773
400	0.34463
600	0.32153
850	0.29266

A.5 Error Calculations Including Temperature Drift

The calculations shown in this section are provided in supplement to the room temperature calculations shown in Section 4.2.2. The calculations are performed over an operating temperature range of -40°C to +85°C. The largest errors due to temperature drift occur at the operating temperature furthest from the ambient temperature of 25°C as shown in Equation (55).

$$\Delta T_{MAX} = 25°C - (-40°C) = 65°C \quad (55)$$

A.5.1 Errors caused by R_{REF} Temperature Drift

The R_{REF} drift specification must be multiplied by the temperature change and converted to a percentage before performing the same calculations used for the R_{REF} tolerance.

$$R_{REF\ Drift}\left(\frac{ppm}{°C}\right) = 2\frac{ppm}{°C} \quad (56)$$

$$R_{REF\ Drift}\ (ppm) = R_{REF\ Drift}\left(\frac{ppm}{°C}\right) \times \Delta T_{MAX} = 2\frac{ppm}{°C} \times 65°C = 130\ ppm \quad (57)$$

$$R_{REF\ Drift}\ (\%) = \frac{R_{REF\ Drift}\ (ppm)}{1{,}000{,}000} \times 100 = \frac{130}{1{,}000{,}000} \times 100 = 0.013\% \quad (58)$$

$$Gain\ Error_{R_{REF}\ Drift}(\%) = \frac{R_{REF\ Drift}(\%)}{R_{REF\ Drift}(\%) + 100} \times 100 = \frac{0.013}{0.013 + 100} \times 100 = 0.01299\% \quad (59)$$

The error in volts due to the R_{REF} drift can be calculated by multiplying the gain error in percent by V_{IN_MAX}.

$$Gain\ Error_{R_{REF\ Drift}}(V) = \frac{Gain\ Error_{R_{REF\ Drift}}(\%)}{100} \times V_{IN\_MAX} = \frac{0.01299}{100} \times 390.48\ mV \quad (60)$$

$$Gain\ Error_{R_{REF\ Drift}}(V) = 50.7234\ \mu V$$

A.5.2 Errors due to ADS1247 Temperature Drift

As the ambient temperature changes, the ADS1247 will produce errors due to offset drift, gain error drift, and IDAC mismatch drift.

Offset error drift is commonly specified as an input-referred voltage and can be directly entered from the device performance datasheet. The largest offset drift error will be at a system ambient temperature of -40°C (See Figure 15 in the ADS1247 datasheet).

$$Offset\ Error_{ADC\ Drift}(V) = 1\ \mu V \quad (61)$$

If offset drift is specified in µV/°C then it will first be multiplied by ΔT_{MAX} to determine the final offset voltage due to temperature drift.

Like gain error, gain error drift in the ADS1247 datasheet is specified as %FSR. The largest gain drift error will be at a system ambient temperature of -40°C (See Figure 23 in the ADS1247 datasheet).

$$\text{Gain Error}_{\text{ADC Drift}}(\text{V}) = \frac{\text{Gain Error}_{\text{ADC Drift}}(\%)}{100} \times V_{IN\_MAX} = \frac{0.01}{100} \times 390.48\ \text{mV} = 39.048\ \mu\text{V} \quad (62)$$

If gain error drift is specified in ppm/°C, then it must first be converted into Gain $\text{Error}_{\text{ADC Drift}}$ (%) similar to the conversion performed in Equations (56) – (58).

The IDAC mismatch drift is commonly specified in ppm/°C. First, calculate the IDAC mismatch in %FSR based on the drift specification and ΔT_{MAX}.

$$I_{\text{IDAC Mismatch Drift}}(\%) = \frac{I_{\text{IDAC Mismatch Drift}}(\text{ppm})}{1{,}000{,}000} \times \Delta T_{MAX} \times 100 \quad (63)$$

$$I_{\text{IDAC Mismatch Drift}}(\%) = \frac{10}{1{,}000{,}000^{\circ}\text{C}} \times 65^{\circ}\text{C} \times 100 = 0.065\%$$

The gain error caused by the IDAC mismatch drift can be calculated in %FSR using the same calculations shown in Appendix A.7 and then converted to volts.

$$\text{Gain Error}_{\text{IDAC Mismatch Drift}}(\%) = \frac{I_{\text{IDAC Mismatch Drift}}(\%)}{I_{\text{IDAC Mismatch Drift}}(\%) + 200} \times 100 = \frac{0.065}{0.065 + 200} \times 100 \quad (64)$$

$$\text{Gain Error}_{\text{IDAC Mismatch Drift}}(\%) = 0.03249\%$$

$$\text{Gain Error}_{\text{IDAC Mismatch Drift}}(\text{V}) = \frac{\text{Gain Error}_{\text{IDAC Mismatch Drift}}(\%)}{100} \times V_{IN\_MAX} = \frac{0.03249}{100} \times 390.48\ \text{mV} \quad (65)$$

$$\text{Gain Error}_{\text{IDAC Drift}}(\text{V}) = 126.9\ \mu\text{V}$$

The error from the IDAC mismatch drift can be removed if the IDAC sources are chopped as described in Section 3.1.2.

A.5.3 Total Error over Temperature

With all of the input-referred errors calculated in volts, the total error can be calculated by taking the root-sum-of-square of all of the uncorrelated ambient temperature and temperature drift error terms.

$$\text{Error}_{\text{Total}}(V) = \sqrt{\begin{array}{l}\text{Gain Error}_{R_{REF}\ \text{Tol}}{}^2 + \text{Gain Error}_{R_{REF}\ \text{Tol Drift}}{}^2 + \text{Offset Error}_{\text{ADC}}{}^2 \\ + \text{Offset Error}_{\text{ADC Drift}}{}^2 + \text{Gain Error}_{\text{ADC}}{}^2 + \text{Gain Error}_{\text{ADC Drift}}{}^2 \\ + \text{INL Error}_{\text{ADC}}{}^2 + \text{Gain Error}_{\text{IDAC}}{}^2 + \text{Gain Error}_{\text{IDAC Mismatch Drift}}{}^2\end{array}} \quad (66)$$

$$\text{Error}_{\text{Total}}(V) = 303.9\ \mu V$$

The system errors over temperature and their resulting input-referred errors in µV are summarized in Table 15.

Table 15. Summary of Error Sources and Resulting Voltage Error RTI over Temperature

Error Source	Value		Input-Referred Error (µV)	
	Typ	Max	Typ	Max
R_{REF} Errors				
R_{REF} Tolerance	-	0.02%	-	164
R_{REF} Drift	-	2 ppm/°C	-	106.6
ADS1247 Errors				
Integrated Nonlinearity (INL)	6 ppm	15 ppm	4.92	12.3
Offset Voltage	-	15 µV	-	15
Offset Voltage Drift		1 µV		1
Gain Error	0.005%	0.02%	19.52	78.1
Gain Error Drift	0.01%	0.015%	39.05	58.57
IDAC Mismatch	-	0.15%	-	292.6
IDAC Mismatch Drift	-	10 ppm/°C	-	126.9

The IDAC mismatch errors can be removed by chopping the IDAC sources as described in Section 3.1.2. A two-point gain and offset calibration can remove the errors from the R_{REF} tolerance, offset voltage, gain error, and IDAC mismatch leaving only the error from INL and temperature drift errors. Table 16 compares the unadjusted error with the error after chopping the IDAC sources and performing a two-point gain and offset calibration at 25°C and over temperature.

Table 16. Total Error Voltage RTI over Operating Temperature

	Total Error (µV)	
	Typ	Max
Unadjusted Error at 25°C	303.9	313.4
Unadjusted Error at 25°C with IDAC Chop	82.02	112.1
Calibrated Error at 25°C	4.92	12.3
Unadjusted Error over Temp	335.5	346.9
Unadjusted Error over Temp with IDAC Chop	104.1	136.3
Calibrated Error over Temp	142.2	149.2
Calibrated Error over Temp with IDAC Chop	64.2	78.5

The magnitude of the IDAC source can be used to convert the calculated voltage error into a calculated resistance error in Ohms as shown in Equation (47). The results from Table 16 have been converted to resistance accuracy in Table 17.

Table 17. Total Resistance Error over Operating Temperature

	Total Error (Ω)	
	Typ	**Max**
Unadjusted Error at 25°C	0.304	0.313
Unadjusted Error at 25°C with IDAC Chop	0.082	0.112
Calibrated Error at 25°C	0.0049	0.012
Unadjusted Error over Temp	0.335	0.347
Unadjusted Error over Temp with IDAC Chop	0.104	0.136
Calibrated Error over Temp	0.142	0.149
Calibrated Error over Temp with IDAC Chop	0.064	0.079

With the resistance accuracy known, the final temperature accuracy can be calculated by dividing the resistance accuracy by the change in the RTD resistance per degree Celsius. The results in Table 18 use the sensitivity at 0°C of 0.3908Ω/°C.

Table 18. Total Temperature Error over Operating Temperature

	Total Error (°C)	
	Typ	**Max**
Unadjusted Error at 25°C	0.778	0.802
Unadjusted Error at 25°C with IDAC Chop	0.21	0.287
Calibrated Error at 25°C	0.013	0.031
Unadjusted Error over Temp	0.858	0.887
Unadjusted Error over Temp with IDAC Chop	0.266	0.349
Calibrated Error over Temp	0.364	0.382
Calibrated Error over Temp with IDAC Chop	0.164	0.201

A.6 Derivation of the Errors from R_{REF} Tolerance

The ideal transfer function will be compared to a modified transfer function to determine the effects of R_{REF} tolerance on the system accuracy. The ideal transfer function is shown again in Equation (67).

$$Code_{IDEAL} = Codes_{TOTAL}\left(\frac{R_{RTD}}{4 \times R_{REF}}\right) \quad (67)$$

If R_{REF} is substituted with (R_{REF}+R_{REF}*Δ) in the ideal transfer function, then it simplifies to Equation (68).

$$Code_{R_{REF}\ Error} = Codes_{TOTAL}\left(\frac{R_{RTD}}{4 \times (R_{REF} + \Delta \times R_{REF})}\right) \quad (68)$$

Equation (69) calculates the gain error caused by the R_{REF} tolerance by comparing the calculated error transfer function to the ideal transfer function.

$$Gain\ Error_{R_{REF}\ Tol}(\%) = \frac{Code_{R_{REF}\ Error} - Code_{IDEAL}}{Code_{IDEAL}} = -\frac{\Delta}{\Delta + 1} \quad (69)$$

If R_{REF} is substituted with R_{REF}-R_{REF}*Δ to calculate the effects of a decrease in R_{REF}, the polarity of the gain error will be positive.

Assuming the tolerance is specified in %, the gain error can be calculated as shown:

$$\text{Gain Error}_{R_{REF}\ Tol}(\%) = \frac{R_{REF\ Tol}(\%)}{R_{REF\ Tol}(\%) + 100} \quad (70)$$

A.7 Derivation of the Errors from IDAC Mismatch

The ideal transfer function will be compared to a modified transfer function to determine the effects of a mismatch in the IDAC current sources on the system accuracy. The ideal transfer function is shown again in Equation (71).

$$\text{Code}_{IDEAL} = \text{Codes}_{TOTAL}\left(\frac{R_{RTD}}{4 \times R_{REF}}\right) \quad (71)$$

However, if I_2 is set equal to (I_1+ I_1*Δ) in Equation (7), the transfer function simplifies to Equation (72).

$$\text{Code}_{IDAC\ Mismatch\ Error} = \text{Codes}_{TOTAL}\left(\frac{R_{RTD}}{4 \times R_{REF} + 2 \times \Delta}\right) \quad (72)$$

Equation (73) calculates the gain error caused by the IDAC mismatch by comparing the calculated error transfer function to the ideal transfer function.

$$\text{Gain Error}_{IDAC\ Mismatch\ Drift}(\%) = \frac{\text{Code}_{IDAC\ Mismatch\ Error} - \text{Code}_{IDEAL}}{\text{Code}_{IDEAL}} = -\frac{\Delta}{\Delta + 2} \quad (73)$$

If I_1 is substituted with I_2+ I_2*Δ, the polarity of the gain error will be positive.

Assuming the IDAC mismatch is specified in %FSR, the gain error can be calculated as shown in Equation (74).

$$\text{Gain Error}_{IDAC\ Mismatch\ Drift}(\%) = \frac{I_{IDAC\ Mismatch\ Drift}(\%)}{I_{IDAC\ Mismatch\ Drift}(\%) + 200} \quad (74)$$

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