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TI Precision Designs: Verified Design

18 bit, 10kSPS Data Acquisition (DAQ) Block Optimized for Ultra Low Power < 1 mW

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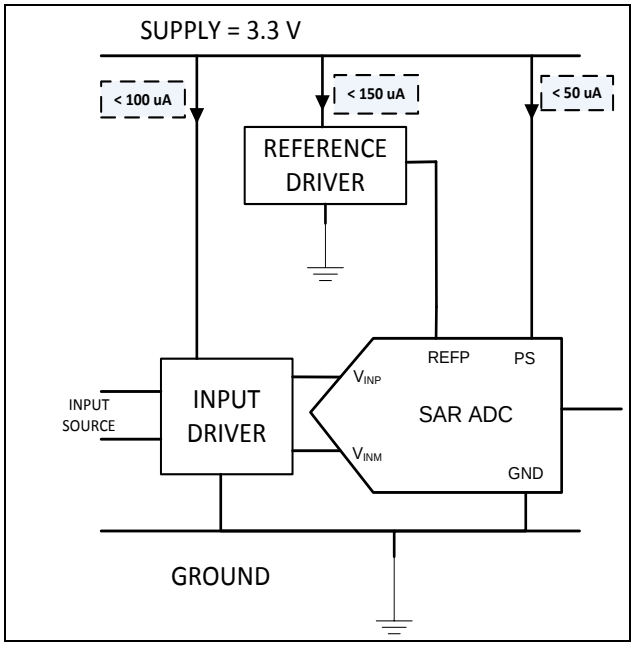
Design Resources

Design Archive	All Design files
TINA-TI™	SPICE Simulator
OPA313	Product Folder
OPA2333	Product Folder



Circuit Description

This 1 mW, 18bit, 10kSPS DAQ block has been optimized for low throughput applications that need to extend battery life.

The ultra-low power DAQ system consists of a reference driver, input driver, and the ADS8881 SAR ADC. Careful attention is paid not only in reducing system power consumption but also in improving the overall noise performance of the driver by making the ADC noise to be the dominant source and the driver noise to be negligible.

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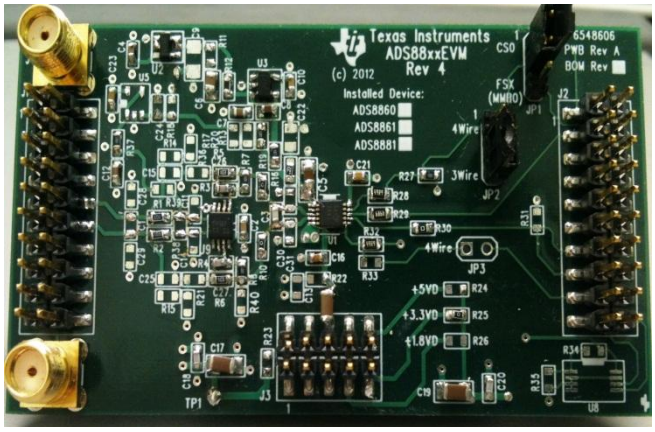


1 Design Summary

This design involves selecting optimum active and passive components for the reference drive and input drive circuitry. ADS8881 is used in conjunction with the drive circuitry to run on less than 1 mW of power for low throughput applications. The design requirements include:

- Total power consumption: < 1 mW dc
- Throughput: <10 kSPS
- Input range: - 2.5 V to 2.5 V dc
- Supply voltage: 3.3 V dc

The design goals and performance are summarized in Table 1. Figure 1 shows the measured ac performance of this design.

Table 1: Comparison of design goals, simulation and measured performance

Parameter	Goal	Simulated	Measured
Total Power	< 1 mW	0.40 mW	0.56 mW
System noise*	35.35 uV_{RMS} (ADC_{RMS_Noise})	37.56 uV_{RMS}	31.28 uV_{RMS}
Effective resolution**	17.11 BIT	17.03 BIT	17.28 BIT
Integral Non-Linearity (INL)	< 3 LSB	NA	-2.4 LSB, 0.78 LSB

* Square root of sum of square of ADC_{RMS_Noise}, and input drive noise

** Resolution taking RMS_Noise into consideration

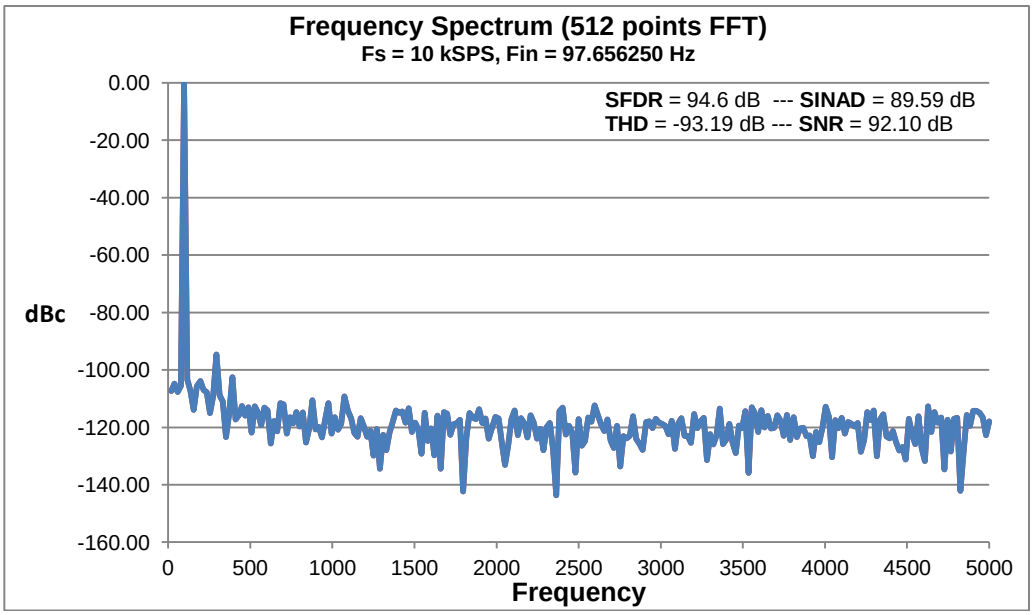


Figure 1: AC Performance (Measured)

2 Theory of Operation

One of the ways to reduce overall system power consumption in low throughput applications, such as ECG monitoring, is by running a faster ADC at low throughput. ADS8881 is an 18 bit, 1MSPS, differential input ADC that can support external reference (REF) from 2.5 V – 5 V. It can convert unipolar, true differential input voltages from –REF to REF. This device is designed for low voltage operation up to 3.6 V which can significantly cut down the overall system power.

The power consumption of ADS8881 is around 5.5 mW at 1 MSPS and scales down linearly with throughput. For applications below 10kSPS throughput, the power consumed by ADC is around 55 uW. With such low power consumption, it becomes critical for the drive circuitry around ADS8881 to be optimized for minimal power consumption as well.

As shown in the block diagram in Figure 2, the drive circuitry is optimized in 2 stages. Reference driver and the input driver are designed and simulated independently and superimposed on to each other to verify the overall system performance.

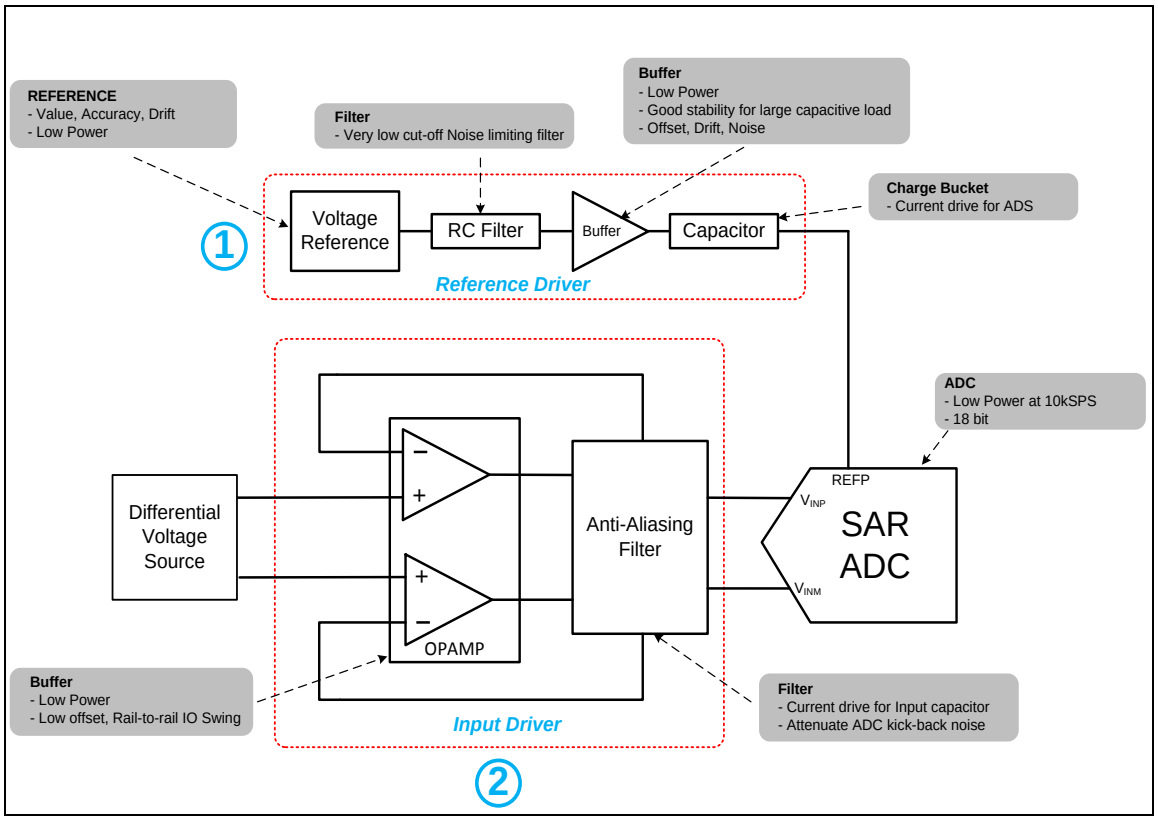


Figure 2: Reference and Input drive circuit elements for low power

2.1 Reference Drive

Designing the reference drive circuitry is a 4 step optimization process that involves,

1. Identifying a reference that is suitable for low power applications
2. Designing a filter that limits the Broadband noise from the reference
3. Estimating the capacitor value needed for providing the reference drive current
4. Identifying an op-amp that is suitable for low power that can recharge the capacitor.

2.1.1 Reference

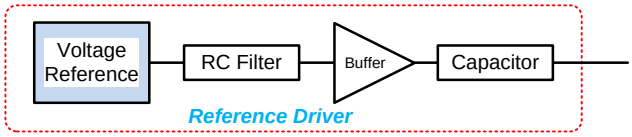


Figure 3: External voltage reference for the converter

ADC's compare an input to a known reference and its binary scaled weights to estimate an equivalent digital code. For accurate digital conversion of the input signal, a highly accurate, low drift reference that has low noise at the output is required. For capacitor based ADC reference input, the load at the reference pin spikes out every time a bit value is estimated. Not only does reference current transient multiple times within a conversion cycle but also the magnitude of the transient current varies between conversions.

An ideal ADC is one that gives the same digital code for a given input. However, a noisy reference shows up as variation of code out at the output of the ADC for a fixed input. It also degrades the linearity, THD and SNR. A good system design should ensure good noise performance at low reference voltages which translates to a good performance at higher reference voltages. This design optimizes reference drive circuit at the lowest supported reference voltage where it is most demanding. The lowest reference voltage ADS8881 can run on is 2.5 V.

There are two types of noise that a reference can introduce. Flicker noise is the noise dominant at low frequencies and broadband noise dominates at high frequencies. The broadband noise, in particular, can be of the order of 100's of microvolts and can easily exceed the 10's of microvolts of rms noise of the converter. Typically, flicker noise is specified on the datasheet as peak-to-peak noise up to 10 Hz. This has to be scaled down by a factor of 6.6 to convert it into rms noise. Broadband spectral noise density on the other hand may not be specified on the datasheet and for a bandgap reference this will be of the order of 0.1 $uV_{RMS}/\sqrt{Hz}$ to 10 $uV_{RMS}/\sqrt{Hz}$ in magnitude. It is inversely proportional to the square root of the quiescent current of the reference. If it is not specified, a good approximation is given by Equation 1 below.

$$\text{REF}_{\text{Broadband\_Noise\_Density}} \approx \frac{10{,}000\text{nV}}{\sqrt{\text{Hz}}} \times \frac{\sqrt{\mu\text{A}}}{\sqrt{2 * \text{I}_{\text{Q\_REF}}(\text{in } \mu\text{A})}} \quad (1)$$

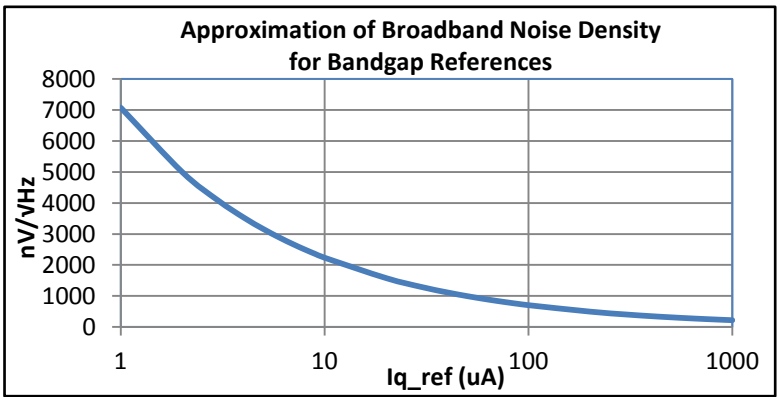


Figure 4: Broadband Noise Density vs. Reference Quiescent current

As seen from Figure 4, noise and power are inversely related. A reference with low I_Q inherently comes with higher noise.

2.1.2 RC Filter

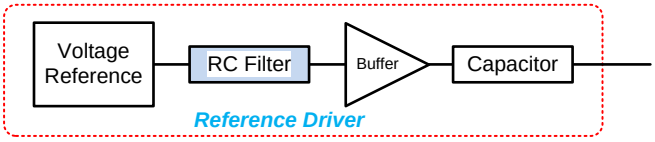


Figure 5: RC Filter for limiting broadband noise of reference

Because of the tradeoff between power and noise, it is important to add a filter block to limit the broadband noise at the output of the reference. Ideal scenario would be to eliminate the reference noise completely. For practical purposes, the rms reference broadband noise should be made insignificant compared to the rms noise of the converter. For this design, the broadband reference noise is limited to less than a third of the rms noise of the ADC[1].

$$\mathrm{REF}_{\mathrm{Broadband\_RMS\_Noise}} \leq \frac{1}{3} \times \mathrm{ADC}_{\mathrm{RMS\_Noise}} \tag{2}$$

A low pass filter with a cutoff frequency of $f_{filter-cutoff}$ limits the broadband noise as shown in Equation 3.

$$\mathrm{REF}_{\mathrm{Broadband\_RMS\_Noise}} = \mathrm{REF}_{\mathrm{Broadband\_RMS\_Density}} \times \sqrt{\frac{\pi}{2} \times (f_{filter-cutoff} - 10\ \mathrm{Hz})} \tag{3}$$

Combining the two equations above, we get the following limiting condition that can be used for designing the filter.

$$\mathrm{REF}_{\mathrm{Broadband\_RMS\_Density}} \times \sqrt{\frac{\pi}{2} \times (f_{filter-cutoff} - 10\ \mathrm{Hz})} \leq \frac{1}{3} \times \mathrm{ADC}_{\mathrm{RMS\_Noise}} \tag{4}$$

$$f_{filter-cutoff} \leq 10 + \frac{2}{9\pi} \times \left(\frac{\mathrm{ADC}_{\mathrm{RMS\_Noise}}}{\mathrm{REF}_{\mathrm{Broadband\_RMS\_Density}}} \right)^2 \tag{5}$$

2.1.3 Capacitor as charge bucket

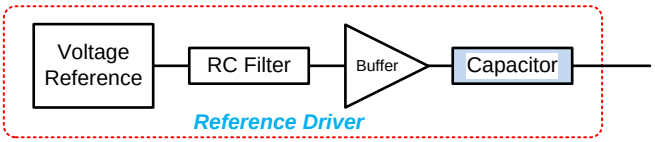


Figure 6: Capacitor for providing charges (reference drive)

The input impedance of the reference pin of the converter is dynamic in nature. It exhibits very high impedance during acquisition time and varies during conversion time. This capacitor can deliver the net charge during conversion time, then a buffer recharges this capacitor during acquisition time.

Net charge that the capacitor needs to deliver can be estimated based on the average reference current and throughput rate as seen on the datasheet using the Equation 6.

$$\Delta Q = I_{REF} \times T_{Throughput} \tag{6}$$

Every time the reference capacitor delivers charge, the voltage across it droops. The net change in voltage across the capacitor during conversion time should be limited to less than half a Least Significant Bit (LSB) of change. For high resolution converters, special attention has to be paid to this capacitance as the capacitive load creates a pole at the output of the buffer. Equations below can be used to provide a starting value for the capacitor.

$$\Delta V \leq \frac{1}{2} LSB \tag{7}$$

$$\frac{\Delta Q}{C} \leq \frac{1}{2} \times \left[\frac{2 \times V_{REF}}{2^N}\right] \quad \ldots\ldots\ldots (\text{Input range is } \pm V_{REF}) \tag{8}$$

$$\frac{I_{REF} \times T_{Throughput}}{C} \leq \frac{1}{2} \times \left[\frac{2 \times V_{REF}}{2^N}\right] \tag{9}$$

2.1.4 Buffer

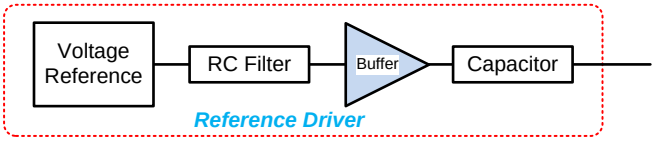


Figure 7: Buffer for recharging the capacitor

An op-amp is needed to recharge the capacitor above. Some of the micro-power op-amps that meet the design goal of 1 mW are OPA333, OPA336 and OPA313.

Additional noise introduced by the buffer, should be minimized while selecting this op-amp. However, this is less of a concern because unlike references where output noise density is of the order of a few uV/$\sqrt{Hz}$, the same will be in the range of 10 nV/$\sqrt{Hz}$ to100 nV/$\sqrt{Hz}$ for op-amps. The broadband noise gets further band-limited by the isolation resistor and the capacitor following the buffer.

Flicker and broadband noise introduced by the op-amp should be verified for it to be significantly smaller (< one third) than the reference noise before finalizing on the op-amp. As done in the design before, reducing the buffer noise to less than a third of the reference noise makes the op-amp noise term insignificant when it gets added to the reference noise (square root of summation of squares). Flicker noise is specified on the datasheet as peak-to-peak noise up to 10 Hz. This has to be scaled down by a factor of 6.6 to convert it into rms noise. Also, broadband noise density specified on the datasheet has to be scaled due to the filter as shown below. The total noise introduced by the op-amp is the square root of sum of squares of the flicker noise and broadband rms noise.

$$OPA_{Broadband\_RMS\_Noise} = OPA_{Broadband\_RMS\_Density} \times \sqrt{\frac{\pi}{2} \times (f_{filter-cutoff} - 10\ Hz)} \tag{10}$$

$$OPA_{Broadband\_RMS\_Noise} = OPA_{Broadband\_RMS\_Density} \times \sqrt{\frac{\pi}{2} \times (\frac{1}{2\pi RC} - 10\ Hz)} \tag{11}$$

CAUTION:

High resolution converters cause the size of the capacitor in the charge bucket to become too large causing stability issues in most of the op-amps. This can be addressed with a series isolation resistor at the cost of the bandwidth of the op-amp. Choosing the right capacitor, op-amp and an isolation resistor is an iterative process that has to be verified by simulation [2,3,4,5]. During this process the capacitance might require minimal adjustments from the starting value taking stability, voltage drop and cutoff frequency into consideration.

2.2 Input Drive

Designing the input stage is a 2 step optimization process. It includes,

1. Selecting a noise rejection input capacitor that charges the sample-hold capacitor (C_{SH})
2. Identifying an op-amp that can consume low power and recharge the input capacitor.

2.2.1 Input capacitor (C_{FLT})

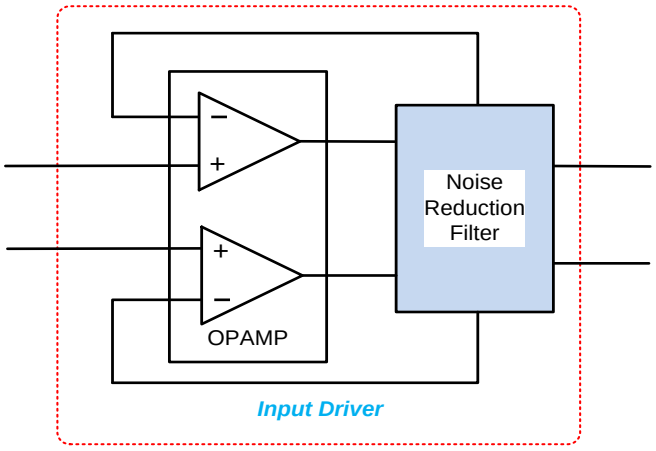


Figure 8: Noise reduction input capacitor

The noise reduction filter block consists of a differential capacitor, C_{FLT}, which is added between the two input pins as shown in Figure 9. This helps minimize noise by attenuating the kick-back noise from the ADC and also by band-limiting the broadband noise of the op-amp.

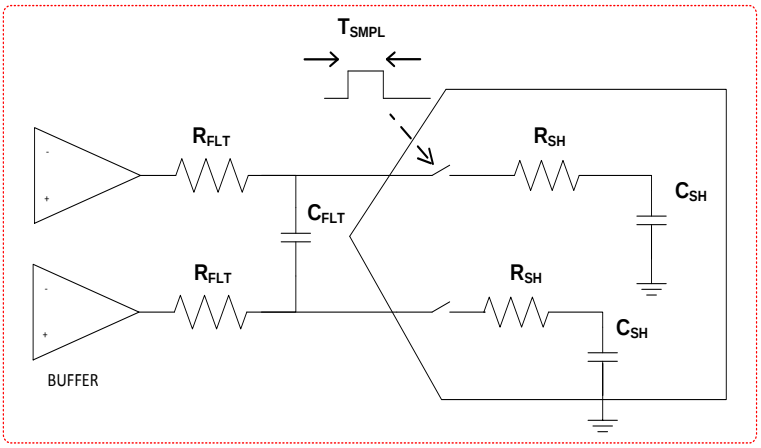


Figure 9: Input capacitor for attenuating noise

This fly-wheel capacitor also acts as a charge reservoir by providing the charges to C_{SH} during acquisition time. The op-amp delivers charges to the capacitor to bring it up to the input voltage, V as shown in Figure 10. This capacitor should be large enough to charge or discharge the sample-hold capacitor during acquisition time and retain 95% of its initial voltage.

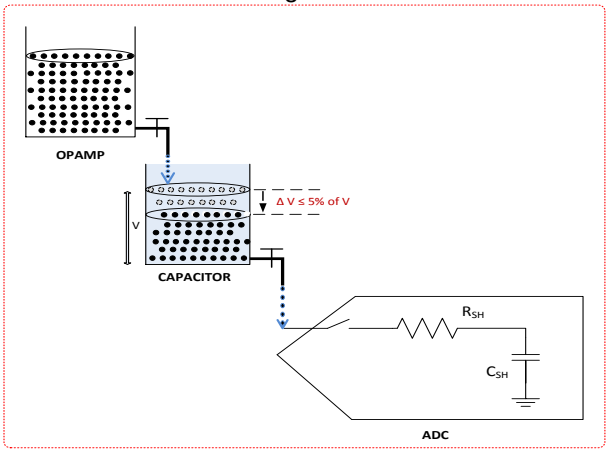


Figure 10: Fly-wheel capacitor delivering charges to C_{SH}

The sampling capacitor inside ADS8881 has a typical value of 60pF. When the input is at its maximum, C_{SH} has to be charged to entire V_{REF} during the sampling time. The corresponding charge needed is approximately 150 pC (60 pF x 2.5 V). While delivering 150 pC to C_{SH}, the voltage across this capacitor should not droop below 5% of its initial voltage, i.e. V_{REF} to keep the op-amp in its linear operating region (no slew).

2.2.2 Op-amp

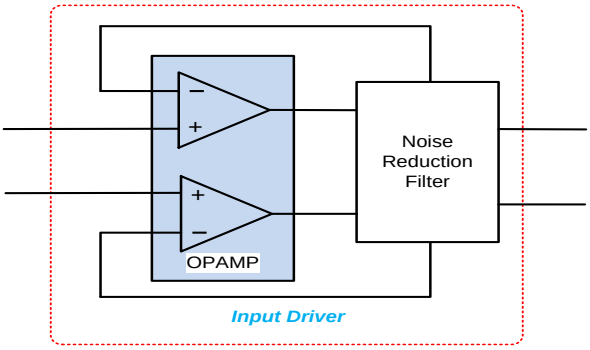


Figure 11: Buffer driving the input

In order to drive a differential input signal, a dual op-amp is used in a modified buffer configuration. It is critical that the op-amp has low power consumption such as OPA333, OPA336, OPA313 etc. The typical operating current for these is below 100 uA. A simple buffer may be unstable as this has to drive the input capacitor explained above. A series resistor might be needed at the output of the op-amp to make it stable. This resistor may introduce an additional drop which can be corrected with dual feedback. As done before, flicker and broadband noise introduced by the op-amp should be verified using,

$$\text{OPA}_{\text{Broadband\_RMS\_Noise}} = \text{OPA}_{\text{Broadband\_RMS\_Density}} \times \sqrt{\frac{\pi}{2} \times (f_{\text{filter-cutoff}} - 10\ \text{Hz})} \quad (12)$$

$$\text{OPA}_{\text{Broadband\_RMS\_Noise}} = \text{OPA}_{\text{Broadband\_RMS\_Density}} \times \sqrt{\frac{\pi}{2} \times (\frac{1}{2\pi R_{FLT} C_{FLT}} - 10\ \text{Hz})} \quad (13)$$

3 Component Selection

For a 3.3 V system, 1 mW of power translates to approximately 300 uA of total current that has to be shared between the reference driver, input driver and the converter. The reference driver is the most critical section for meeting noise and linearity performance, so 50% of the current budget is assigned to it. The goal is to make sure that reference driver section consumes below 150 uA.

The remaining 150 uA is shared between the input driver (100 uA) and ADC (50 uA).

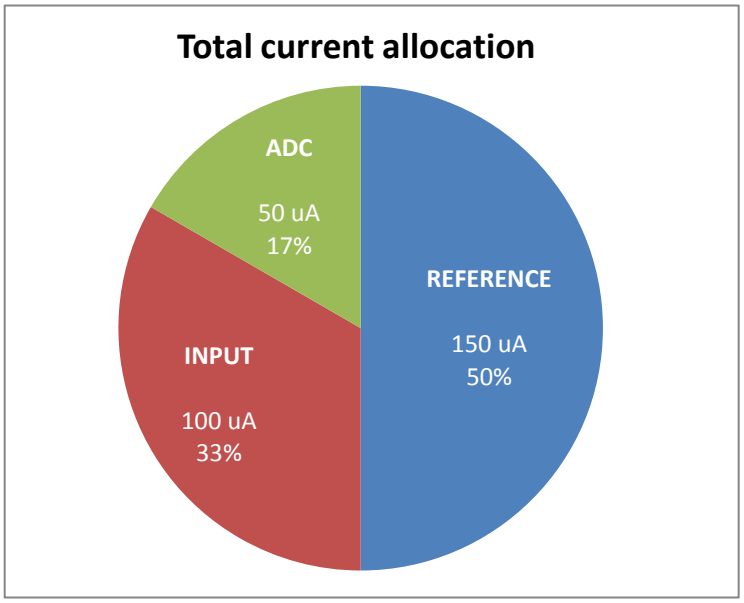


Figure 12: Total current allocation between various blocks

3.1 Reference Driver

3.1.1 Reference

The first step is to list all references that can provide 2.5 V on a 3.3 V supply and has good accuracy specification (<1 % accuracy). Out of those, references that have low quiescent current (< 150 uA) are shortlisted. Refer to Table 8 for a list of possible choices. The REF3325 selected for this design has the lowest quiescent current of 5 uA leaving 145 uA for the buffer. It has an accuracy of 0.15 % and can drive capacitive loads up to 10 uF. It is available in a small 3 pin SOT or SC70 package.

3.1.2 RC Filter

A RC filter is designed such that majority of the broadband noise from the reference is removed. The components are selected such that this noise is below a third of converter noise. The relationship below is used to estimate the cut off frequency which can then be used to estimate the value of R and C as shown in the calculations below.

$$\mathrm{REF}_{\mathrm{Broadband\_RMS\_Density}} \times \sqrt{\frac{\pi}{2} \times \left(f_{\mathrm{filter-cutoff}} - 10\ \mathrm{Hz}\right)} \leq \frac{1}{3} \times \mathrm{ADC}_{\mathrm{RMS\_Noise}} \quad (14)$$

From the datasheet, ADS8881 has 100 dB typical SNR for 5.0 V REF. One could estimate the noise of the converter to be 35.35 uV, using Equation 15.

$$\mathrm{SNR} = 20\ \mathrm{LOG}\left(\frac{\mathrm{SIGNAL_{RMS}}}{\mathrm{ADC_{RMS\_Noise}}}\right) \tag{15}$$

$$100 = 20\ \mathrm{LOG}\left(\frac{2 \times 5.0/2\sqrt{2}}{\mathrm{ADC_{RMS\_Noise}}}\right) \tag{16}$$

$$\mathrm{ADC_{RMS\_Noise}} = 35.35\ \mu\mathrm{V} \tag{17}$$

Once the noise of the converter is known, $f_{filter-cutoff}$ frequency can be derived by substituting the quiescent current of REF3325 and the ADC_{RMS_Noise} in Equation 14.

$$\frac{10\ \mu\mathrm{V}}{\sqrt{2 \times \mathrm{I_{Q\_REF}(in\ \mu A)}}} \times \sqrt{\frac{\pi}{2} \times (f_{filter-cutoff} - 10\ \mathrm{Hz})} \leq \frac{1}{3} \times \mathrm{ADC_{RMS\_Noise}} \tag{18}$$

$$\frac{10\ \mu\mathrm{V}}{\sqrt{2 \times 5\mu\mathrm{A}}} \times \sqrt{\frac{\pi}{2} \times (f_{filter-cutoff} - 10\ \mathrm{Hz})} \leq \frac{1}{3} \times 35.35\ \mu\mathrm{V} \tag{19}$$

$$f_{filter\_cutoff} \leq 18.8\ \mathrm{Hz} \tag{20}$$

To limit the noise contribution of the capacitor, its size should be greater than 0.1 uF. For board space consideration, choosing 0603 component limits the value of this capacitor to 1 uF. Thus, a 1 uF capacitor is selected. This results in a minimum resistance of 8.4 KΩ to meet the condition in Equation 20. Increasing this to 10 kΩ resistance, results in $f_{filter-cutoff}$ of 15.9 Hz thereby meeting the cut off frequency.

3.1.3 Charge bucket capacitor

Using the relationship below, for a 1 MSPS (1 us $T_{Throughput}$) converter with 200 uA I_{REF}, the minimum capacitance can be computed.

$$\frac{\mathrm{I_{REF}} \times \mathrm{T_{Throughput}}}{\mathrm{C}} \leq \frac{1}{2} \times \left[\frac{2 \times \mathrm{V_{REF}}}{2^{\mathrm{N}}}\right] \tag{21}$$

$$\frac{200\ \mu \times\ 1\mu}{\mathrm{C}} \leq \frac{1}{2} \times \left[\frac{2 \times 2.5}{2^{\mathrm{N}}}\right] \tag{22}$$

$$\mathrm{C} \geq 20.9\ \mu\mathrm{F} \tag{23}$$

A standard capacitor value of 22 uF was selected to satisfy the condition above.

3.1.4 Buffer

To reduce the number of op-amp choices for buffer, start by selecting op-amps that can operate on 3.3 V power supply. Then select those op-amps that consume less than 145 uA. As seen from Table 10, OPA333 has one of the lowest quiescent currents of 17 uA.

However, OPA333 exhibits an inductive behavior from 10 Hz to 10 KHz as can be seen by looking at the output Impedance on TINA-TI™. This along with the reactance of 22 uF acts like a resonant circuit that can make the buffer prone to oscillations. Figure 14 shows the impedance of a 22 uF capacitor plotted with the open loop output impedance of OPA333 as if a 22 uF capacitor were directly on the output of the OPA333. Around 100Hz there will be an effective L-C resonance formed by the open loop output impedance of the OPA333 and the capacitive load and make stability of this very difficult [5].

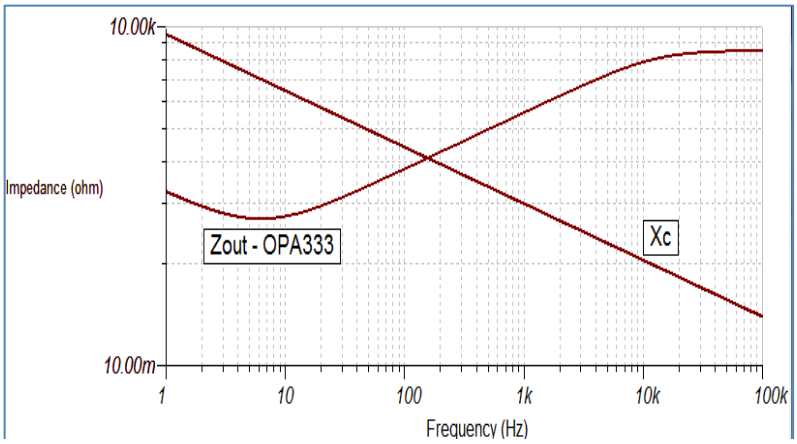


Figure 13: Crossover between the output impedance of OPA333 and 22uF capacitor

A properly selected series resistor could stabilize OPA333. The output impedance of OPA333 is too high to allow proper compensation with a reasonably valued series resistor. For example, a 1 kΩ series resistor results in a time constant of 22 ms which would far exceed the period between samples (0.1 ms at 10k SPS). This would be too long of a time for the buffer to restore the capacitor back to the reference voltage.

The next best choice is an OPA336 with 20 uA quiescent current and a unity Gain Bandwidth (GBW) of 100 KHz. With a capacitive load, the GBW drops by approximately 95% to 5 KHz. A much higher bandwidth op-amp will be needed while recharging the 22 uF capacitor.

The op-amp with the next lowest current and high enough GBW (~1MHz) in Table 10 is OPA313. This op-amp is designed to drive pure capacitive loads and is stable up to 1nF in the unity-gain configuration. A 22 uF capacitor along with output impedance of 2300 Ω degrades the phase margin quickly, causing stability issues. The equivalent series resistance (ESR) may sometimes be sufficient to alter the phase to make the amplifier stable. However, to ensure stability a small resistor in series will be introduced with the output that is comparable to ESR. The value of this resistor is designed such that we account for at least 1 time constant to be able to recharge the 22 uF capacitor to final REF value.

$$\boldsymbol{\tau \leq \frac{1}{10KSPS}} \tag{24}$$

$$\boldsymbol{(R \times 22\mu) \leq 100\ \mu s} \tag{25}$$

From the relationship above, this resistor value should be less than 4.54 Ω. A 1 Ω series resistor could be a good starting point. As a first pass check the gain plot needs to be analyzed for stability using 1 Ω and 22 uF capacitive load at the output of OPA313.

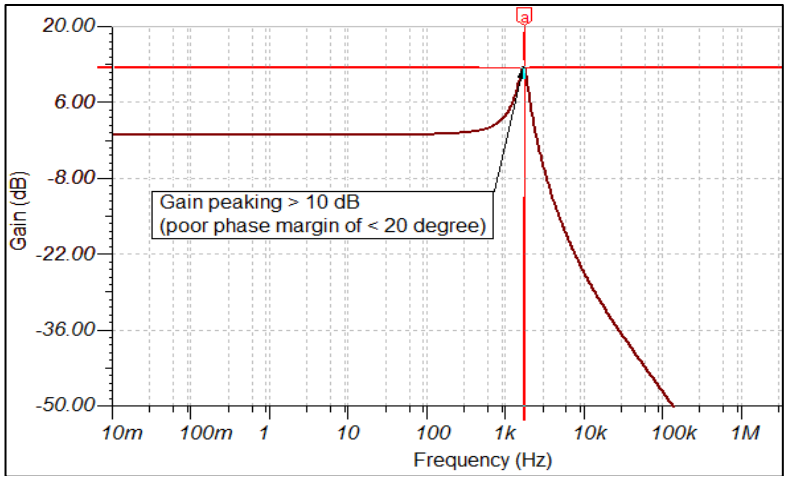
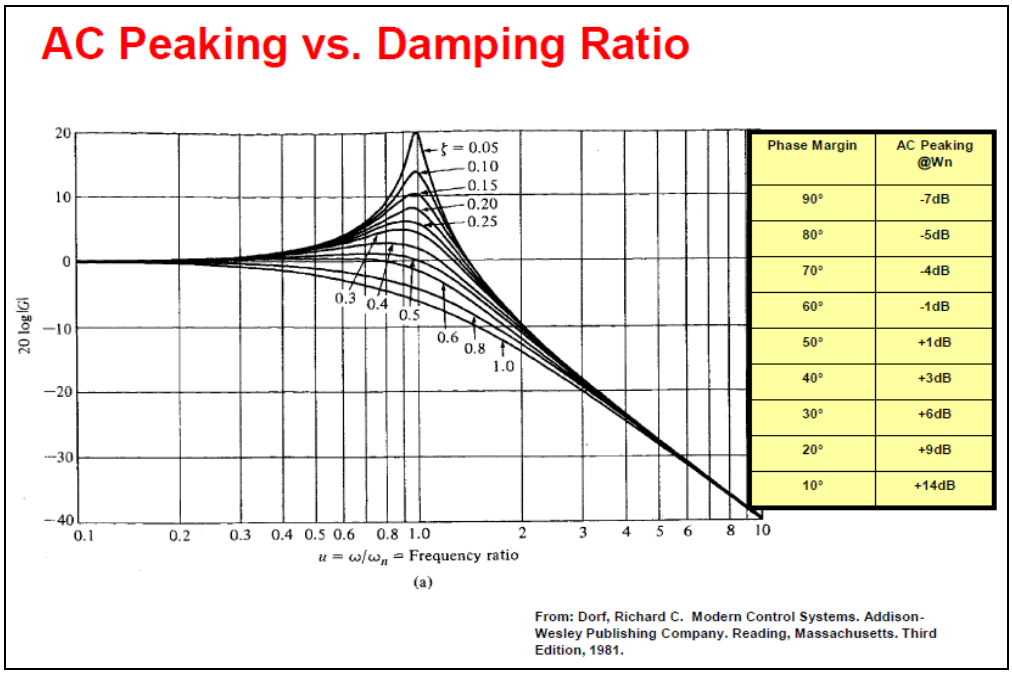


Figure 14: Gain plot – OPA313 with 1 Ohm isolation resistor

This configuration shows gain peaking of >10 dB on TINA-TI™. Similar analysis could have been performed by providing a 100 mV voltage step to the amplifier and observing the overshoot which also can be correlated back to phase margin. As seen from Figure 15, gain peaking of > 10 dB results in less than 20^{O} of phase margin. Due to device-to-device variation and parasitics, for a stable design, the phase margin of at least 40^{O} is preferred [6].



Phase Margin	AC Peaking @Wn
90°	-7dB
80°	-5dB
70°	-4dB
60°	-1dB
50°	+1dB
40°	+3dB
30°	+6dB
20°	+9dB
10°	+14dB

Figure 15: AC peaking and PM translator

This resistance is increased until the closed loop gain peaking is around 3 dB which translates to 40^{O} phase margin. This occurs at 4.5 Ω as seen in simulation in Figure 16.

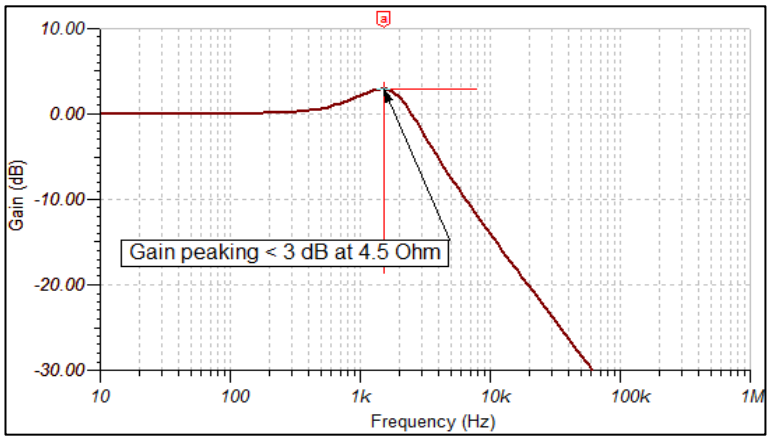


Figure 16: Gain plot – OPA313 with 4.5 Ohm isolation resistor

A standard value of 4.7 Ω is chosen for this design. The circuit then has to be verified for stability using TINA-TI™ before proceeding further. The voltage drop across the series 4.7 Ω resistor introduces an additional error on the reference voltage which can be rectified by sensing at the point where the resistor is connected to the capacitor as shown in Figure 17.

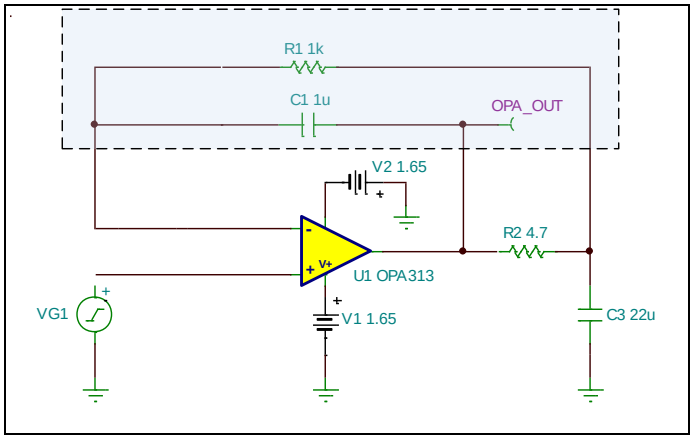


Figure 17: Dual feedback – OPA313 with 4.7 Ohm isolation resistor

A 4.7 Ω resistor in combination with the 22 uF acts as a low pass filter with a cut-off frequency of 1.5 KHz. This helps reduce the broadband noise from the op-amp. To correct for the additional drop introduced by 4.7 Ω resistor dual feedback is introduced using 1 kΩ and 1 uF resulting in a cutoff frequency that is about 10 times lower than 4.7 Ω and 22 uF. Details of this compensation technique are covered in [5, section 10].

3.2 Input Driver

3.2.1 Capacitor

The droop across the input capacitor should be limited, as it delivers charges to C_{SH}, to less than 5 % of its initial value. The maximum droop occurs when the input is close to the full scale value of V_{REF}. While designing for this capacitor, full scale input should be taken into consideration as this will be the worst case[7].

$$\Delta V_{FLT} = \frac{\Delta Q_{FLT}}{C_{FLT}} \leq 5\%\ V_{REF} \tag{26}$$

$$\frac{C_{SH} \times V_{REF}}{C_{FLT}} \leq \left[\frac{1}{20} V_{REF}\right] \tag{27}$$

$$C_{FLT} \geq 20 \times C_{SH} \tag{28}$$

From Equation 28, the input capacitor should be greater than 1.2 nF (20 x 60 pF). It is important to pick a C0G capacitor for its good voltage coefficient because a varying capacitance will affect the performance of the converter as the input voltage fed to the converter changes with capacitance. A higher value helps in band-limiting the broadband noise of the driver. A 4.7 nF is selected.

3.2.2 Op Amp (dual feedback)

As seen before, OPA2333 has one of the lowest quiescent currents (17uA/ amplifier) and can be a good choice as input buffer. Unlike reference buffer, the load capacitance of an input driver is much smaller compared to that of the reference driver (4.7 nF vs. 22 uF). The capacitive load at the output of OPA2333 has to be isolated using a resistor. Due to the high output impedance of OPA333, 1 KΩ could be a good starting value for isolation. This configuration shows gain peaking of close to 1 dB on TINA-TI™. As seen from Figure 15 before, this results greater than 40^{O} of phase margin as preferred for this design.

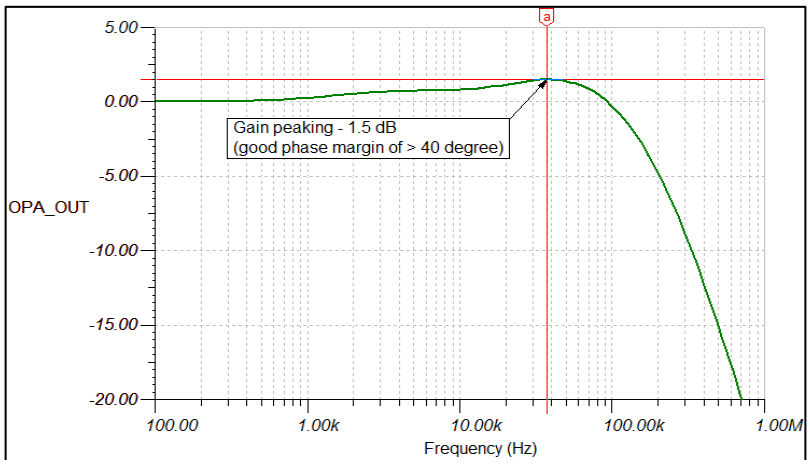


Figure 18: Gain plot - OPA333 with 1 kOhm isolation resistor

As a result, a gain error is introduced by 1 KΩ series isolation resistor along with an input Impedance 200 Ω of R_{SW} of the converter. This can be corrected with dual feedback using a 10 KΩ for feedback. A 10 nF capacitor is used to close the loop for high frequency AC for quicker feedback as shown in Figure 19. The cutoff frequency should be 1 decade away from 1 KΩ and 9.4 nF [5, section 10].

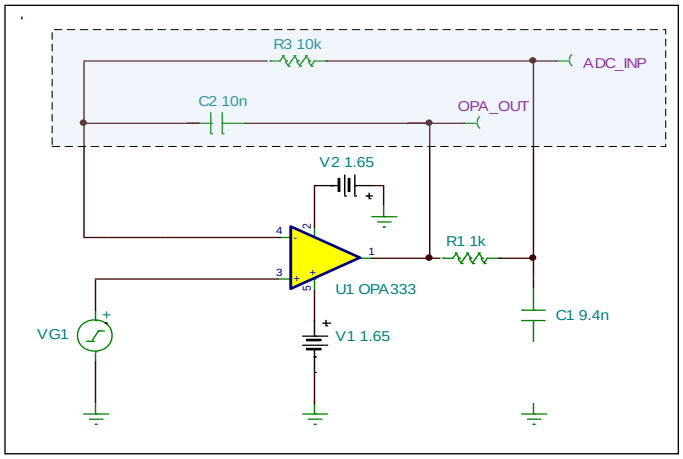


Figure 19: Dual feedback introduced to correct for gain error

4 Simulation

Figure 20 depicts the complete TINA-TI™ schematic for this design. Due to the complexity, the design was simulated on a block-by-block basis.

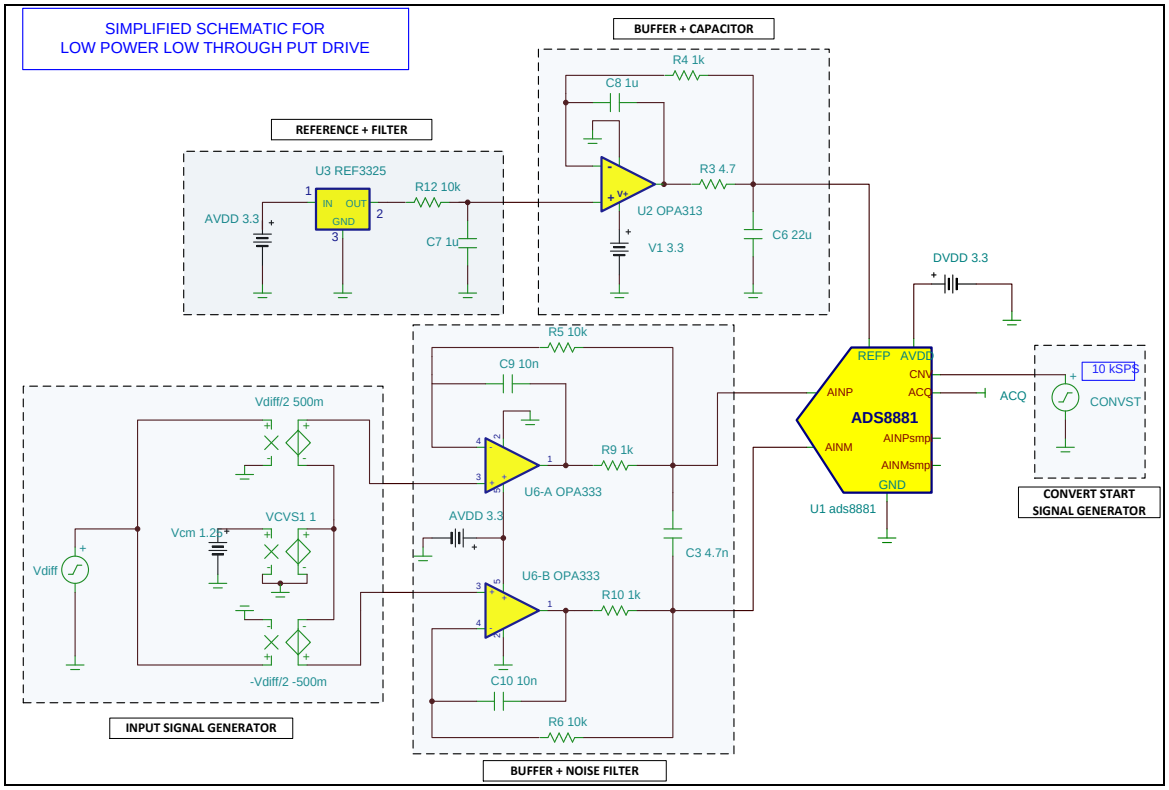


Figure 20: TINA-TI Schematic for Reference Drive and Input Drive

4.1 Reference drive

The performance of the reference drive is checked in two stages. Stability of the buffer that is driving the 22 uF capacitor should be verified as shown in Figure 21. Once that is confirmed, the change in voltage across the capacitor should monitored to be with in an LSB (1/2 LSB for this design) during conversion.

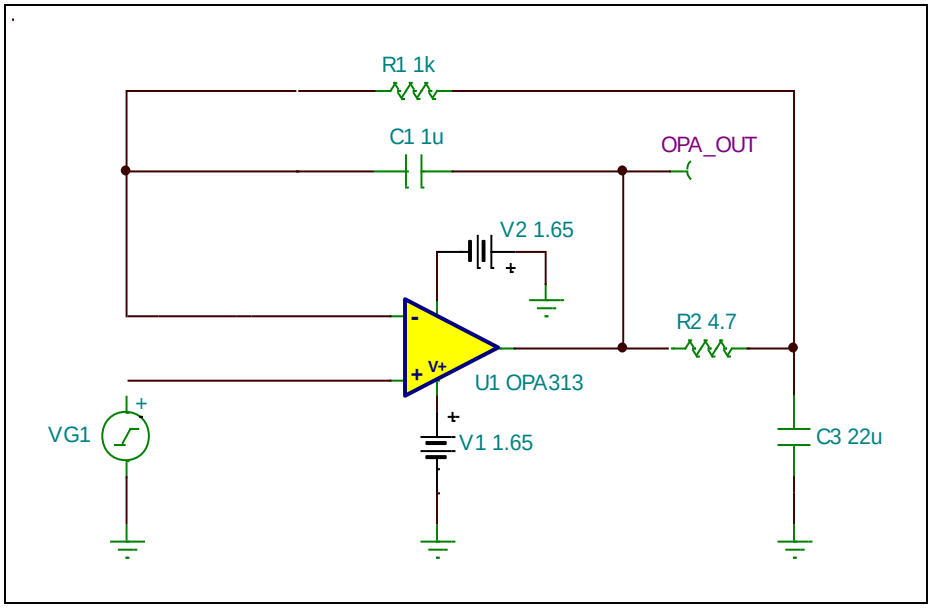


Figure 20: Reference buffer circuit for stability check

A quick check for the reference buffer with the dual feedback configuration is run in order to verify the phase margin. As seen from Figure 22, the peaking with dual feedback is around 3 dB providing close to 40^{O} phase margin.

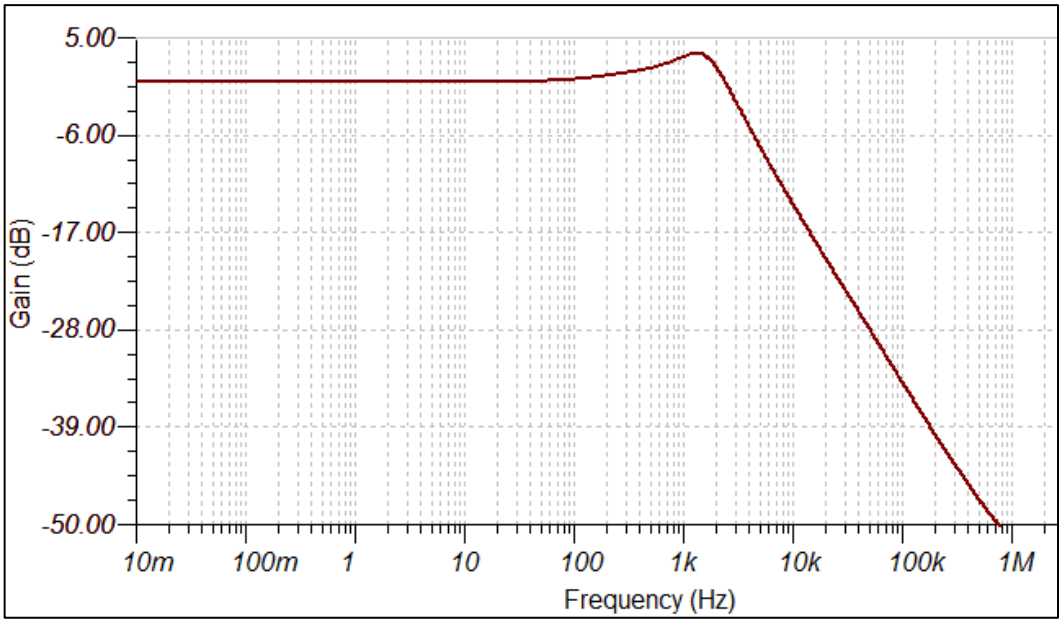


Figure 21: Reference buffer stability check gain plot

To verify the voltage drop across the reference capacitor, the input of the converter is connected to the common mode voltage of $V_{REF}/2$. A convert start signal is applied and the voltage at the reference input pin of the converter is monitored.

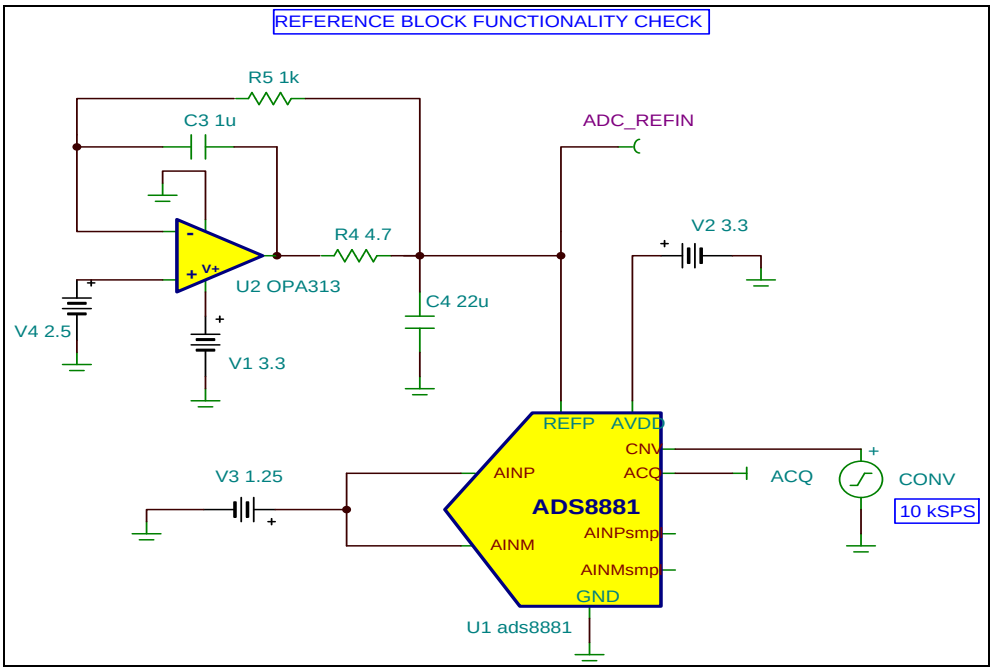


Figure 23: Simplified schematic to check working of reference capacitor

As seen from simulation, the maximum drop across the 22 uF capacitor, as it delivers charges to the reference pin during conversion time, is around 14.1 uV. The capacitor value that was chosen was based on a limit of 9.5 uV (1/2 LSB) of change. A 14.1 uV drop indicates that the model consumes close to 310 uA of I_{REF}. This change in voltage is acceptable as it is still under an LSB (19 uV) of change.

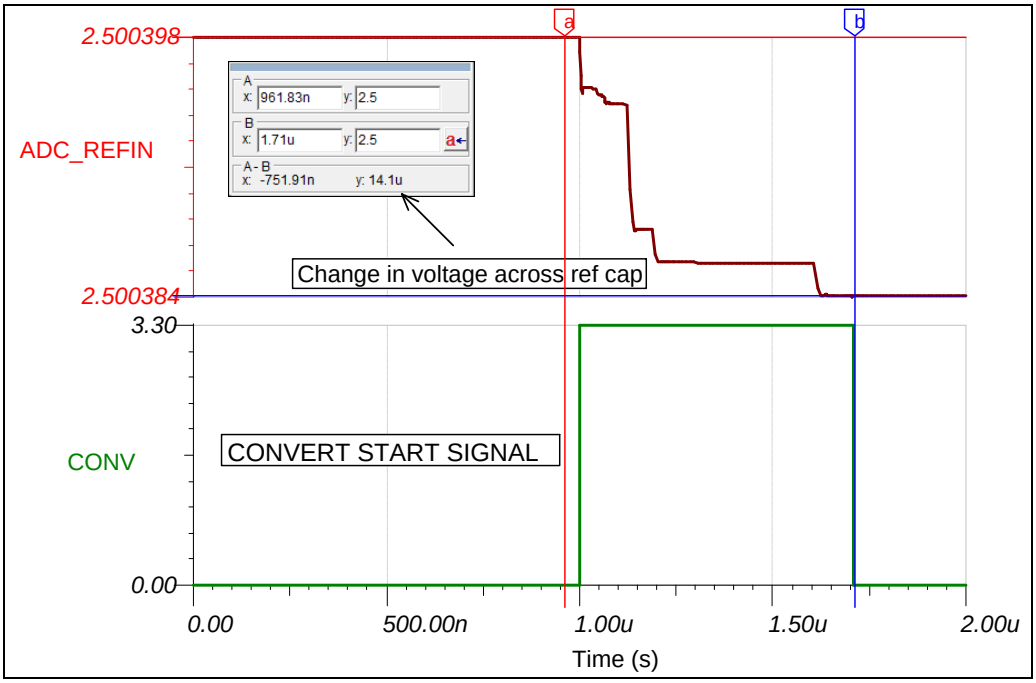


Figure 24: Voltage change across reference capacitor during conversion time

4.2 Input drive

The performance of the input drive is also checked in two stages. The stability of the buffer that is driving the input capacitor is verified first. Voltage across this capacitor has to be verified next such that it settles to within ½ LSB from one conversion to the next.

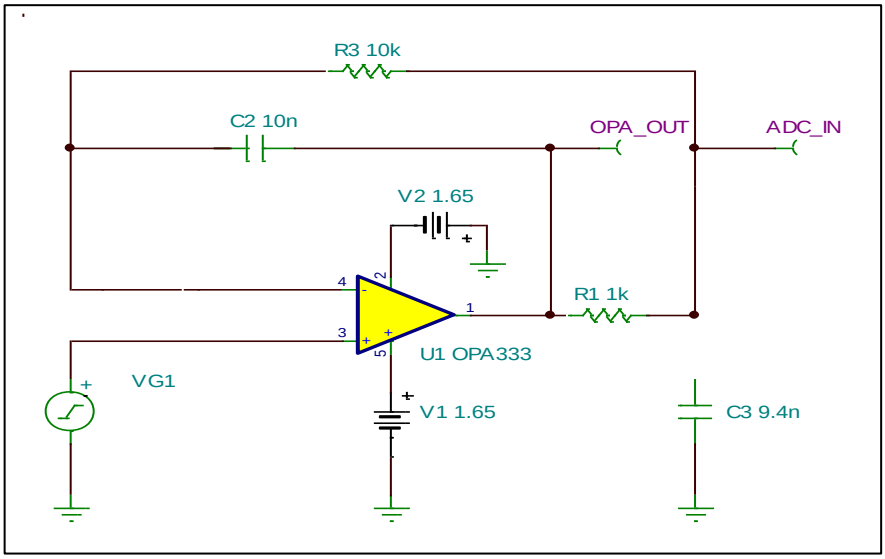


Figure 25: Input buffer circuit for stability check

As before, a quick check for the input buffer with the dual feedback configuration is run in order to verify the phase margin. As seen from Figure 26, the peaking with dual feedback is around 3 dB providing close to 40^{O} phase margin.

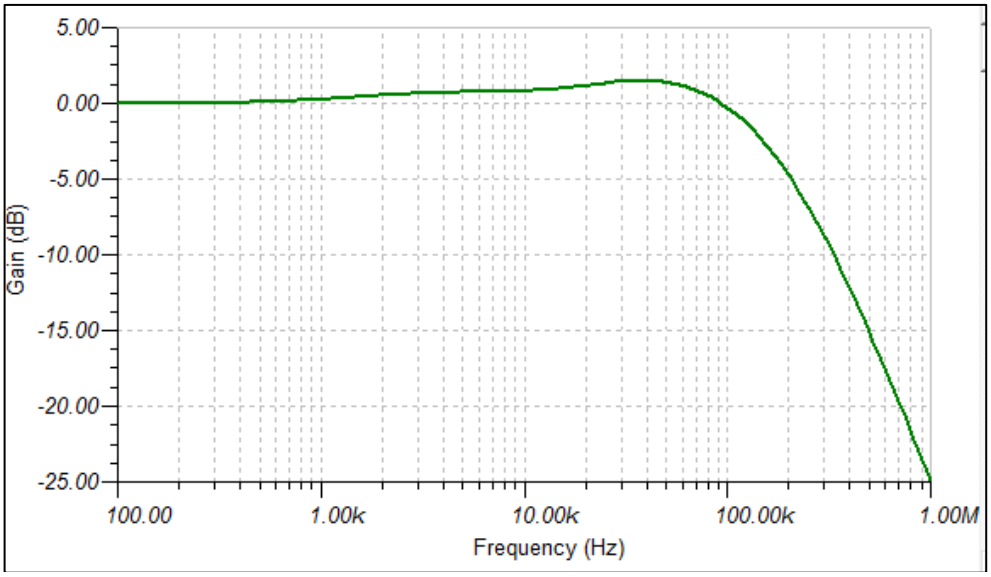


Figure 26: Input buffer stability check gain plot

To verify the working of the input stage, OPA333 along with the noise reduction filter is connected to the input. A convert start signal is applied and the voltage difference between the output of the op-amp and the sample hold capacitor is monitored to see if they are tracking as shown in Figure 27.

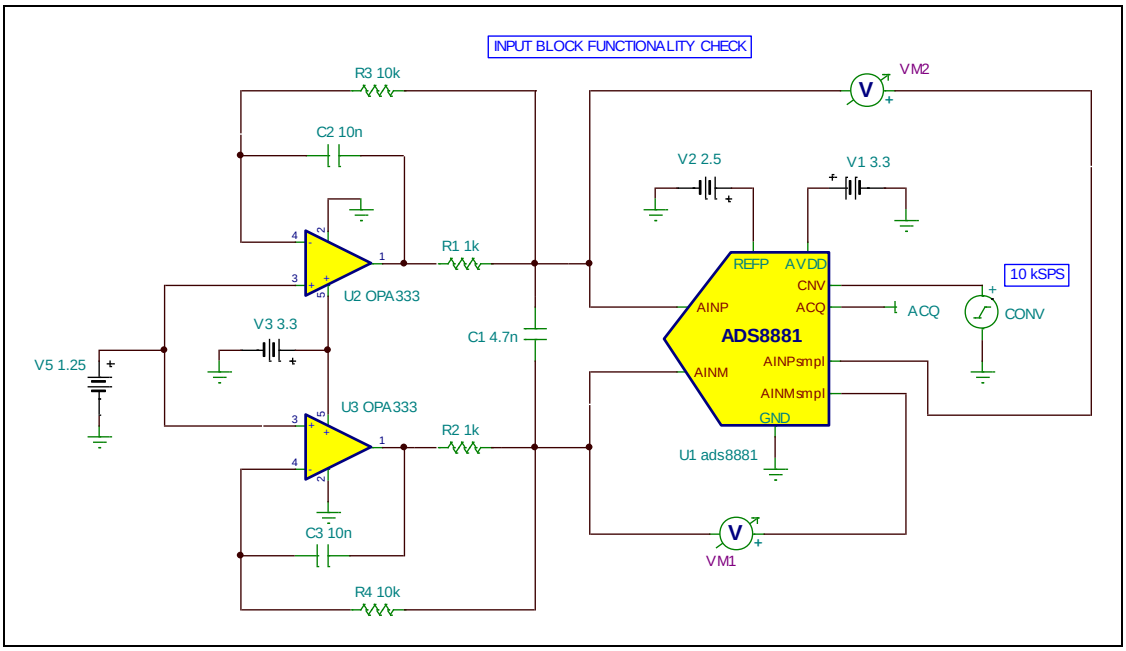


Figure 27: Simplified schematic to check working of input drive

When the convert start signal goes high, the sample-hold switch is disconnected from the input. As the convert start signal goes low, the sample-hold switch is closed. As soon as this load is connected, the output of the op-amp gets disturbed as the op-amp tries to regulate its load and bring it back to the input voltage. The op-amp then corrects its output during the settling time. We want the op-amp regulating its output and thus the voltage at sample-hold capacitor to be within ½ LSB before the next conversion. As seen in Figure 28, settling to ½ LSB of 10 uV occurs within 4.34us much before the next convert start signal.

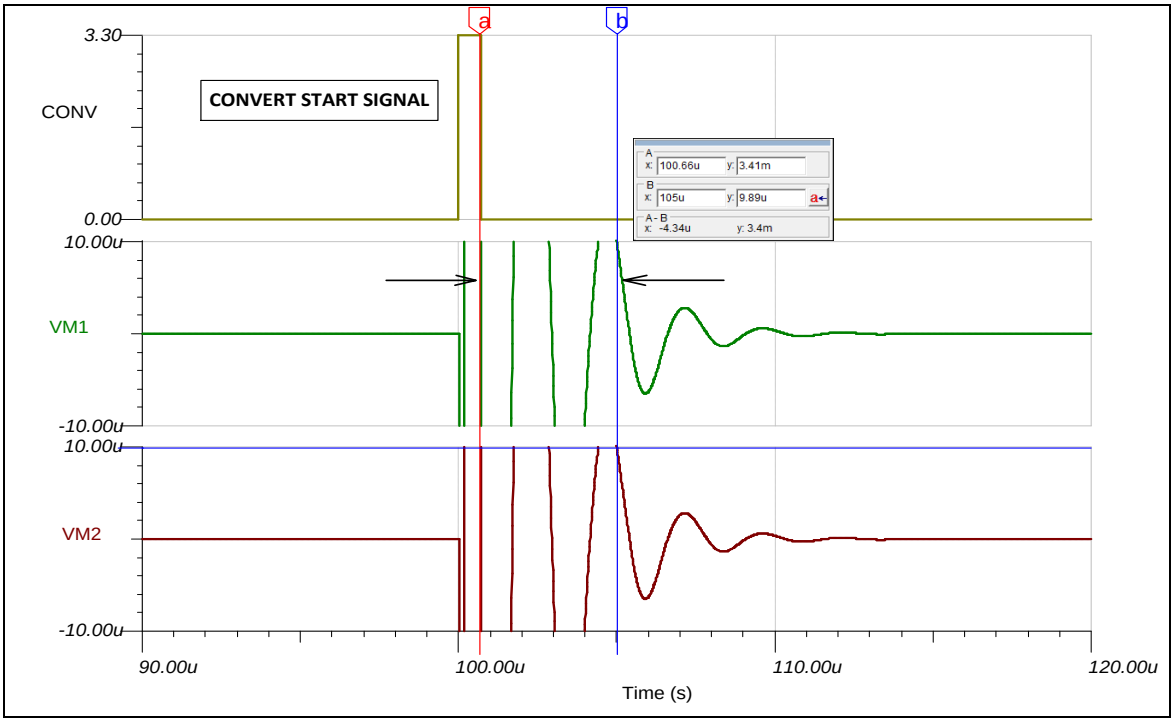


Figure 28 : Op-amp regulating load when sample hold circuit is connected

5 PCB Design

The PCB schematic and bill of materials can be found in the Appendix.

5.1 PCB Layout

The top side view of the board along with the placement of the components can be seen in Figure 29.

Analog signals run on to the left side of the board and the digital signals are placed to the right as much as possible. This reduces any cross-talk between the two. A single ground plane is underneath the entire board.

The components for the reference drive are placed as close as possible to pin1 of the converter on the top left side of the board. In doing so, we are reducing the trace length and hence minimizing the noise picked up by the traces. Also by using wider traces for the reference path, we reduce the trace resistance and thereby any unintentional drop in reference voltage when driving the reference pin.

More than one via to ground is provided to the reference capacitor (C6 – 22 uF) in order to reduce the stray inductance.

Similarly the input drive components are placed close to pin3 and pin4 of the converter on the left side of the board. The connection to the analog supply and the components going to pin 2 (C13 – 1 uF, C16 – 1 nF, R22 – 10 ohm) are placed at the bottom of the converter in order to make room for the input drive components. The traces that run the differential signal are laid out symmetrically from the signal source to the input pin3 and pin 4 of the converter. This helps maintain the same error on each input which then gets nullified out at the input of the converter.

The input noise reduction capacitor (C3 – 4.7 nF) should be of C0G type. This is to reduce the change in capacitance with input voltage which in turns improves the THD performance.

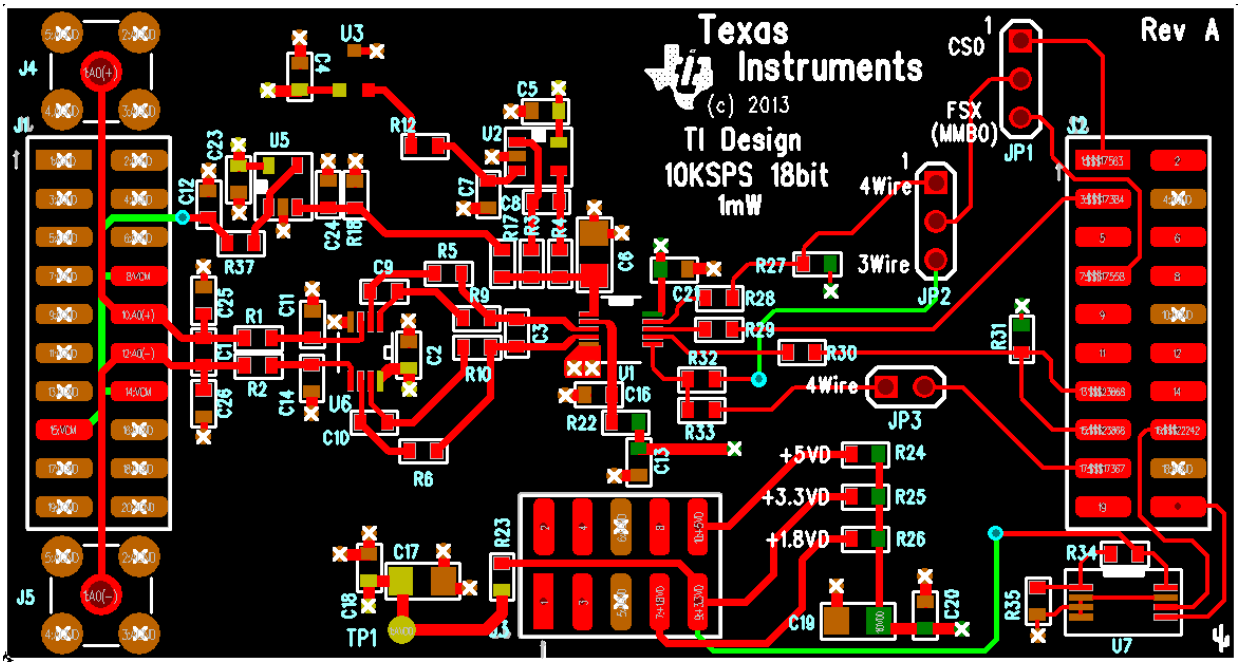


Figure 29: Layout for the EVM

6 Verification & Measured Performance

Having designed all the components and verifying the stability through simulation, it's important to see if the components chosen meet the overall system requirements for noise and power.

6.1 System noise estimation

6.1.1 Reference driver noise

The total noise estimated for the reference driver section includes both noise introduced by reference as well as by the op-amp. This is around 15 uV as shown in Table 2. This will be the square root of sum of squares of all the noise in the path.

Table 2: Overall noise of the reference driver

Noise Source	Magnitude	Comment
Reference Noise		
- REF3325 (Flicker Noise)	10.60	70 uVp-p/6.6. This is dominant up to 10Hz.
- REF3325 + Filter (Broadband Noise)	9.64	3.16 uV/ $\sqrt{Hz}$ density. This gets band limited by filter.
Buffer Noise		
- OPA313 (Flicker Noise)	0.90	6 uVp-p/6.6. This is dominant up to 10Hz.
- OPA313 + Filter (Broadband Noise)	1.22	25 nV/ $\sqrt{Hz}$ density. This gets band limited by filter.
Total Reference Noise	**14.41 uV**	

Noise simulation for the reference block on TINA-TI™ shows around 23.7uV. This includes both flicker and broadband Noise. As seen from the noise plot below, the reference noise has been cut down from 200 uV at the output of the reference to 23 uV at the reference input pin of the converter.

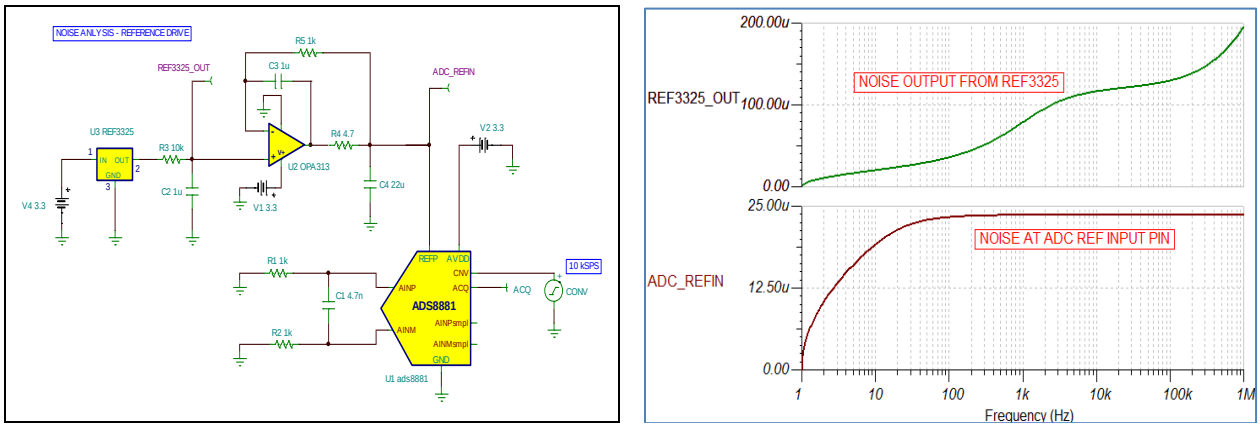


Figure 30: Noise analysis for reference drive

6.1.2 *Input driver noise:*

The overall noise seen at each input is much smaller at around 9uV. The broadband noise of 8.9 uV at each input is comparable to that of reference because of much higher cutoff frequency filter at the input. The combined noise for both inputs is the root of sum of squares of noise at each input which is estimated to be around 12.7 uV.

Table 3: Overall noise of the input driver

Noise Source	Magnitude	Comment
Positive Input Noise		
- OPA2333 (Flicker Noise)	0.16	70uVp-p/6.6. This is dominant up to 10Hz.
- OPA2333 + Filter (Broadband Noise)	8.97	55nV / $\sqrt{Hz}$ density. This gets band limited by filter.
Negative Input Noise		
- OPA2333 (Flicker Noise)	0.16	6uVp-p/6.6. This is dominant up to 10Hz.
- OPA2333 + Filter (Broadband Noise)	8.97	55nV/ $\sqrt{Hz}$ density. This gets band limited by filter.
Total Input Noise	**12.69 uV**	

Noise simulation for the input block on TINA-TI™ shows around 8.3 uV at each input. This includes both flicker and broadband noise of OPA333. The combined noise as seen by the ADC will be root of sum of squares of noise at each input which in this case will be around 11.75 uV. The 7.5% reduction seen in simulation is because the noise density used by the OPA333 model is around 47 nV/ $\sqrt{Hz}$ whereas the calculation uses 55 nV/ $\sqrt{Hz}$.

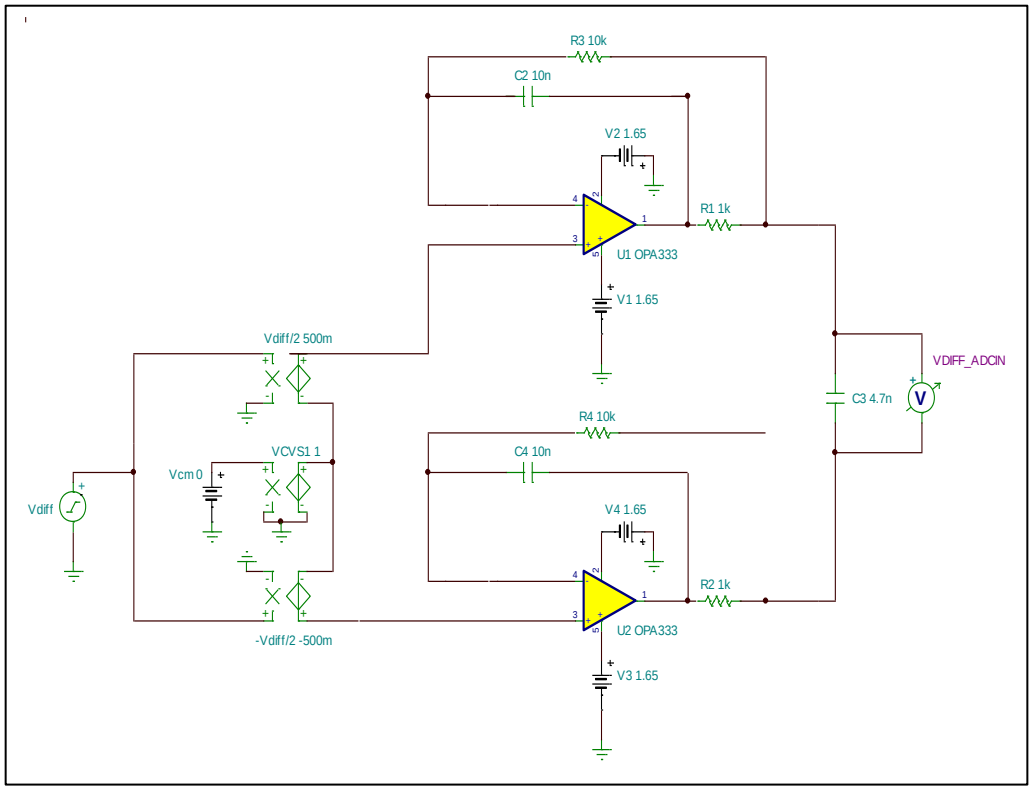


Figure 31: Noise analysis circuit for input drive

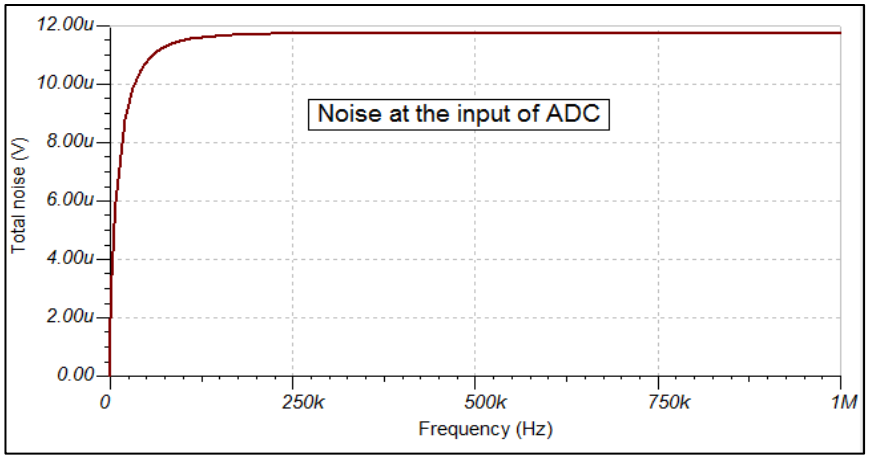


Figure 32: Noise at the input of ADC

The total noise estimated for the system will be square root of sum of square of noise at the positive input, negative input and ADC.

Table 4: System noise estimation

ADC_{RMS_Noise}	Positive input noise	Negative input noise	System noise
35.35 uV_{RMS}	8.97 uV_{RMS}	8.97 uV_{RMS}	37.56 uV_{RMS}

6.2 System Power Estimation

The total power for the reference driver, input driver and the data converter can be estimated based on the components that are selected and from the product datasheet. As seen from Table 5 below, the total power consumption is estimated to be within 0.5 mW.

Table 5: Power estimation for the entire system

Block	Current (uA)	Power (uW)	Comment
Reference			
- REF3325	5	16.5	5 uA x 3.3 V
- OPA313	50	165	50 uA x 3.3 V
Input			
- OPA2333	50	165	50 uA x 3.3 V
Converter			
- ADS8881		55	Specified on the datasheet at 10 kSPS
Total Power	**401.5 uW**		

6.3 Bench verification

6.3.1 DC/ AC performance

To check for the overall performance the noise, linearity, SNR and THD of the system has to be verified. DC noise is measured by setting up mid-scale input and checking for the rms noise.

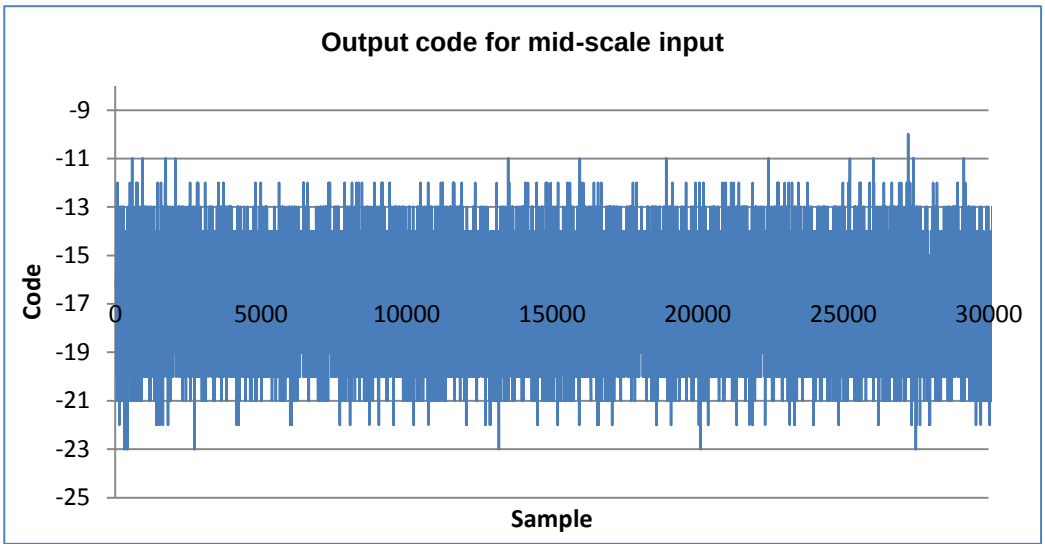


Figure 33 : Output code for mid-scale input

The histogram for the output above is shown in Figure 35. A slight negative shift is seen in the output code due to the offset of the part. The rms noise for the histogram is 1.64 LSB which for a 2.5V reference is around 31.28 uV. This corresponds to a noise free resolution of 14.19 bit.

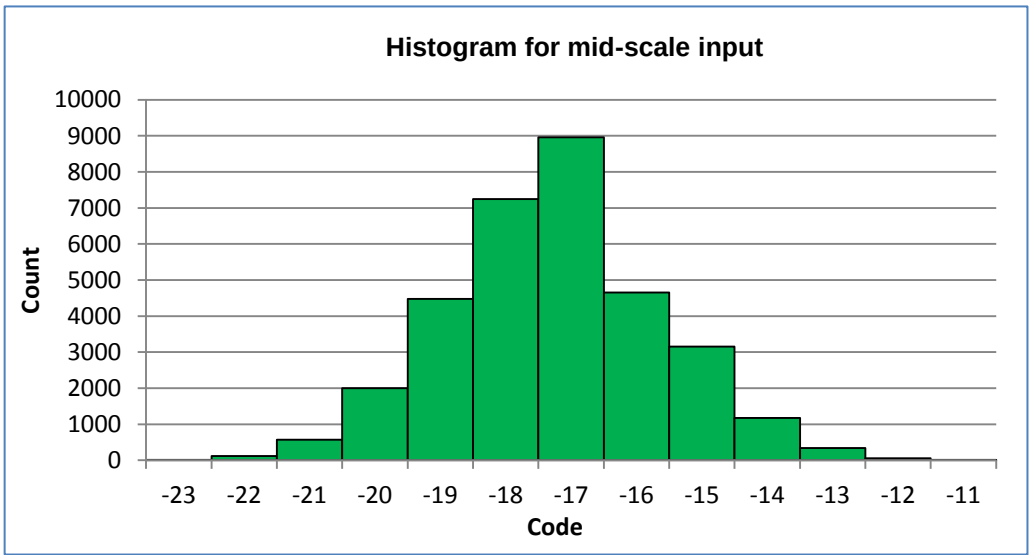


Figure 34: Histogram

Table 6: Noise performance

Maximum Code	Minimum Code	Noise Code (peak to peak)	Noise (uV_{RMS})	Noise free Bits
-10	-23	14	31.28	14.19

A 25 point linearity check shows minimum and maximum error of -2.45 LSB and 0.78 LSB meeting the performance goal.

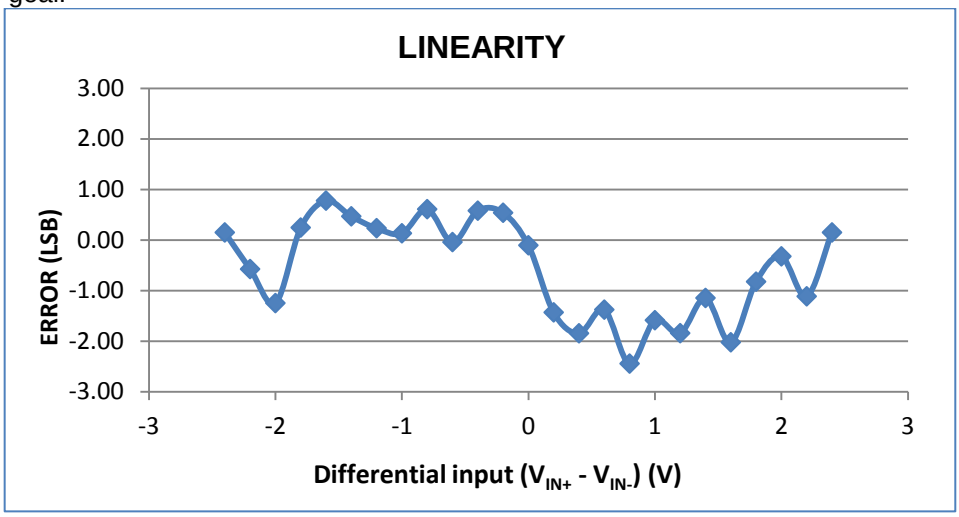


Figure 35: 25 point linearity check

The next check is to verify the SNR and THD of this design. A SNR of 100 dB at 5.0 V reference is equivalent to 93.9 dB at 2.5 V reference. This is measured to be close to 92.1 dB indicating good performance.

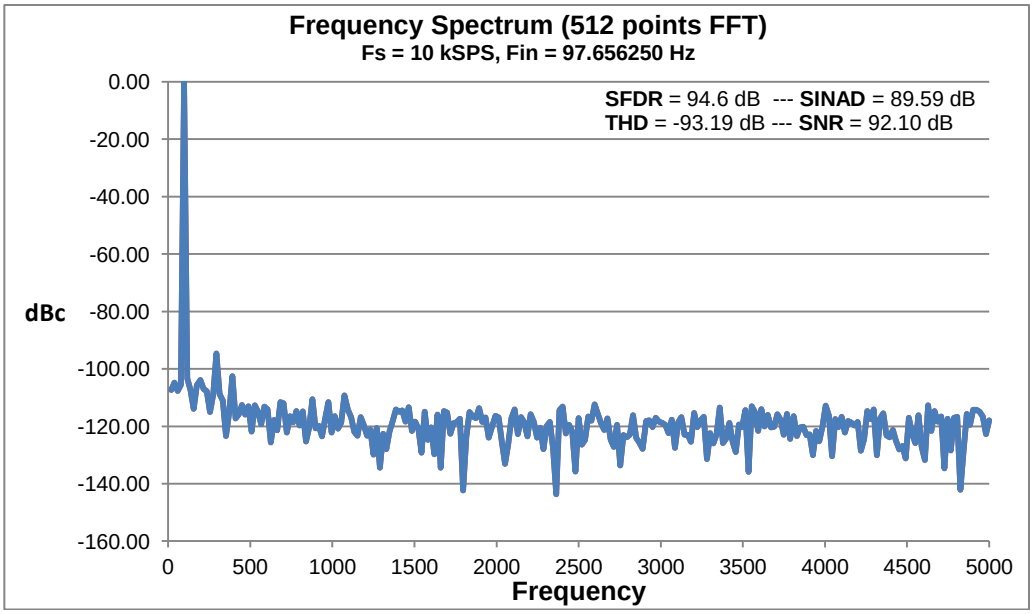


Figure 36 : AC performance

6.3.2 Power consumption

The design goal was to pick components for less than 1 mW of total power consumption. Verification on bench show a power consumption of 0.23 mW during the idle state when there is no active conversion ongoing. This is same as the standby mode.

During an active conversion, a total current of 170 uA is measured resulting in power consumption of 0.56 mW which is much below our goal of 1 mW. Initial estimate of 0.4 mW was based on the static power consumption in each device. The additional 0.16 mW of power on bench is due to dynamic power consumption in various blocks during conversion.

Table 7: Power consumption

Mode	Current (uA)	Voltage (V)	Power (mW)
Idle or Standby mode	70	3.3	0.23
Active mode	170	3.3	0.56

7 Modifications

In this design, in order to reduce power consumption, REF3325 was chosen as it consumes only 5uA. In doing so, the overall noise of the system has increased. One could cut down the noise by selecting a reference that consumes higher power. The pros and cons will become apparent if the noise and power of a replacement reference is analyzed from Table 8.

Table 8: 2.5V references with low current

Device	Current (uA)	Flicker Noise (uVp-p)	Broadband Noise/ (10 Hz – 10 k Hz) (uV_{RMS})	Accuracy (%)	Drift (ppm/^{O}C)	I_{OUT} (mA)
REF3325	5	70	NA	0.15	30	+/-5
REF3025	50	28	80	0.20	50	25
REF3125	100	33	48	0.20	20	+/-10
REF3225	100	33	48	0.20	4	+/-10
REF5025	1000	7.5	NA	0.05	3	+/-10

As an example, REF3025 is compared against REF3325 to observe the improvement in noise performance. This improvement in noise is at the expense of more power. For comparing the two choices, the same filter as per the design is chosen (10 KΩ, 1 uF RC filter, f_{cutoff} = 15.92 Hz) following the reference.

Table 9: Comparison for noise and power between REF3325 and REF3025

Device	Current (uA)	Flicker Noise (uVp-p)	Broadband Noise/ (10 Hz – 10 k Hz) (uV_{RMS})	Flicker Noise (uVp-p/ 6.6) (uV_{RMS})	Broadband Noise/ (15.92 Hz Filter) (uV_{RMS})	Noise (uV_{RMS})	Power (uW)
REF3325	5	70	NA	**10.6**	**9.64**	**14.33**	**16.5**
REF3025	50	28	80	**4.24**	**1.94**	**4.66**	**165**
Change						**9.66**	**148.5**

A reduction of 9.66 uV (14.33 uV – 4.66 uV) is seen in reference noise going from REF3325 to REF3025. This reduction in noise is significant as it translates to greater than 25% improvement over the ADC_{RMS_Noise} (9.66 uV/ 35.35 uV).

The additional power that is needed is 148.5 uW (45 uA x 3.3 V). This increases the overall power consumption by 37% from 401.5 uW to 550 uW. A shown above, depending on the system requirement noise vs. power tradeoff can be achieved as needed.

Similar comparison can be made between other references in Table 8.

While selecting the buffer for the input drive op-amp with lowest quiescent current is picked. Other combinations from Table 10 can be used for improved settling response for some of the higher throughput applications. Improvement in the input noise will be seen as op-amp with lower broadband noise are picked from bottom of Table 10.

Table 10: Op-amp with less than 150uA of current

Device	I_Q (uA)	GBW (k Hz)	Broadband Noise ($nV_{RMS}/\sqrt{Hz}$)	Slew Rate (V/ us)	I_B (pA)
OPA333	17	350	55	0.16	+/-200
OPA336	20	100	40	0.03	+/-10
OPA313	50	1000	25	0.50	+/-10
OPA378	120	900	20	0.40	+/-550
OPA314	150	3000	14	1.50	+/-10

8 Acknowledgements & References

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2. *Trump. Bruce, (2012, May 23), Why Op Amps oscillate – an intuitive look at two frequent causes, Available: http://e2e.ti.com/blogs_/b/thesignal/archive/2012/05/23/why-op-amps-oscillate-an-intuitive-look-at-two-frequent-causes.aspx*
3. *Trump. Bruce, (2012, May 30), Taming the Oscillating Op Amp, Available: http://e2e.ti.com/blogs_/b/thesignal/archive/2012/05/30/taming-the-oscillating-op-amp.aspx*
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5. *Green, Tim, Operational Amplifier Stability Parts 1-11, November 2008, Available: http://www.en-genius.net/site/zones/acquisitionZONE/technical_notes/acqt_050712*
6. *Wells. Collin (2012, February 2), Internal presentation – Operational Amplifier Stability*
7. *Green. Tim (2008, February), Internal presentation – Selecting the right amplifier for a precision CDAC SAR A/D*
8. *Thanks to Hann. Matthew, Lis. Marek, M. Bryan, Semig. Peter for their help with this project.*

Appendix A.

A.1 Electrical Schematic

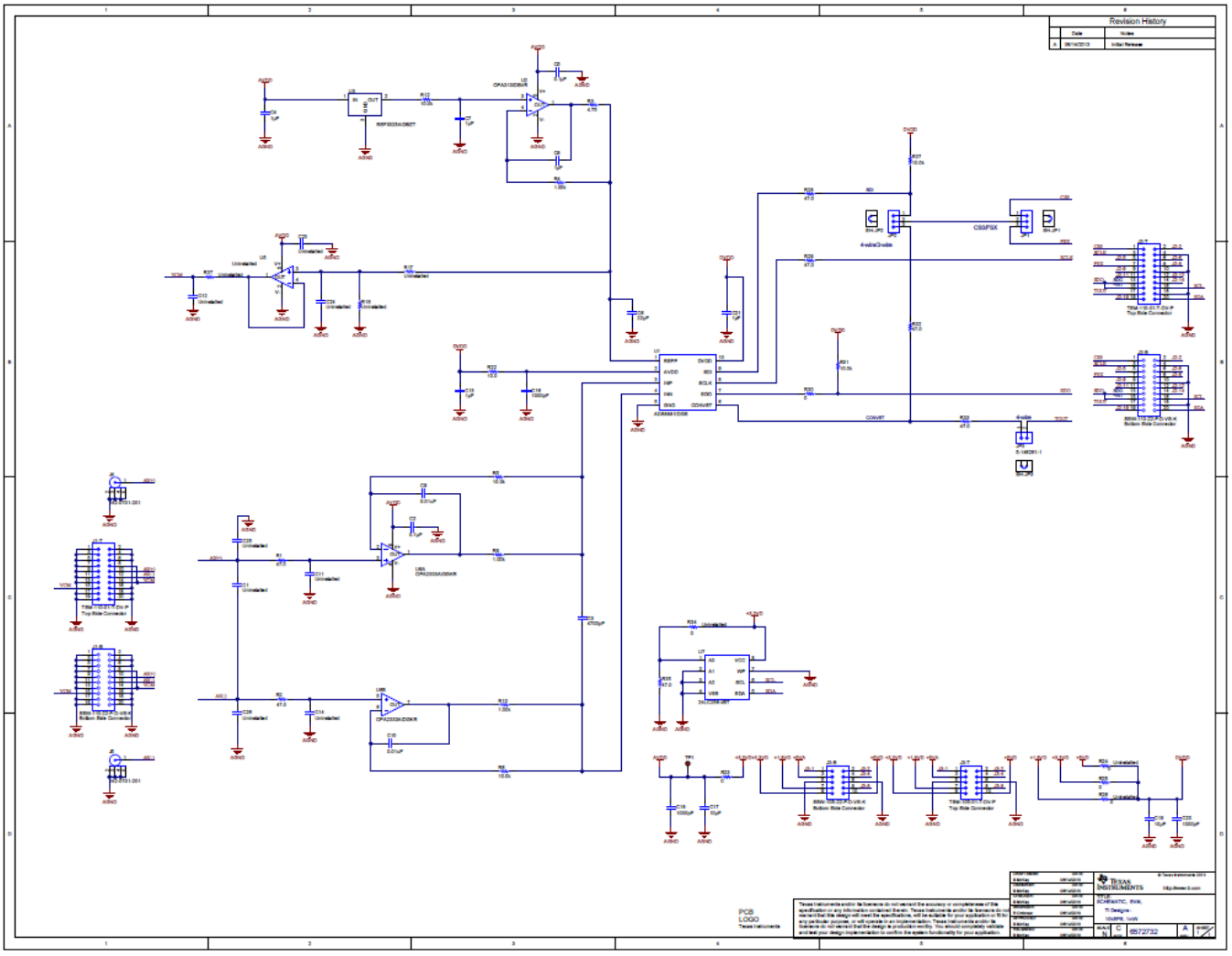

Figure A-1: Electrical Schematic

A.2 Bill of Materials

ITEM	QTY	MFG	MFG PART#	REF DES	DESCRIPTION	VALUE or FUNCTION
1	2	Emerson Network Power	142-0701-201	J4, J5	Connector, TH, SMA	
2	1	Samtec, Inc.	SSW-105-22-F-D-VS-K	J3-B	Connector, Header, 10-Pos (10x2), Receptacle, 100x100-mil Pitch	
3	2	Samtec, Inc.	TSM-110-01-T-DV-P	J1-T, J2-T	Header, 100mil, 10x2, SMD	
4	2	Samtec, Inc.	SSW-110-22-F-D-VS-K	J1-B, J2-B	Connector, Receptacle, 100mil, 10x2, Gold plated, SMD	
5	1	Samtec, Inc.	TSM-105-01-T-DV-P	J3-T	Header, 100mil, 5x2, SMD	
6	2	MuRata	GRM31CR71C106KAC7L	C17, C19	CAP, CERM, 10uF, 16V, +/-10%, X7R, 1206	10uF
7	2	Sullins Connector Solutions	PBC03SAAN	JP1, JP2	Header, TH, 100mil, 1x3, Gold plated, 230 mil above insulator	
8	3	Kemet	C0603C102J5GAC	C16, C18, C20	CAP, CERM, 1000pF, 50V, +/-5%, C0G/NP0, 0603	1000pF
9	1	Keystone	5000	TP1	Test Point, Miniature, Red, TH	
10	2	TDK	C1608C0G1H103J080AA	C9, C10	CAP, 10000pF, 0603, 5%, 50V, C0G	10,000pF
11	5	MuRata	GRM188R71A105KA61D	C4, C7, C8, C13, C21	CAP, CERM, 1uF, 10V, +/-10%, X7R, 0603	1uF
12	1	TDK	C1608C0G1E472J	C3	CAP, CERM, 4700pF, 25V, +/-5%, C0G/NP0, 0603	4700pF
13	3	3M	969102-0000-DA	SH-JP1, SH-JP2, SH-JP3	Shunt, 100mil, Gold plated, Black	
14	1	Vishay-Dale	CRCW060310R0FKEA	R22	RES, 10.0 ohm, 1%, 0.1W, 0603	10.0 ohm
15	1	Vishay-Dale	CRCW06034R75FKEA	R3	RES, 4.75 ohm, 1%, 0.1W, 0603	4.75 ohm
16	3	Vishay-Dale	CRCW06031K00FKEA	R4, R9, R10	RES, 1.00k ohm, 1%, 0.1W, 0603	1.0k ohm
17	5	Vishay-Dale	CRCW060310K0FKEA	R5, R6, R12, R27, R31	RES, 10.0k ohm, 1%, 0.1W, 0603	10.0k ohm
18	2	AVX	06033C104KAT2A	C2, C5	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0603	0.1uF
19	3	Panasonic	ERJ-3GEY0R00V	R23, R25, R30	RES, 0 ohm, 5%, 0.1W, 0603	0 ohm
20	7	Yageo America	RC0603FR-0747RL	R1, R2, R28, R29, R32, R33, R35	RES, 47.0 ohm, 1%, 0.1W, 0603	47.0 ohm
21	1	Microchip	24LC256-I/ST	U7		
22	1	Texas Instruments	ADS8881IDGS	U1	ADC 1MSPS 18bit Fully-Diff MSOP-10	ADS8881
23	1	MuRata	GRM31CR61C226KE15L	C6	CAP, CERM, 22uF, 16V, +/-10%, X5R, 1206	22uF
24	1	TE Connectivity	5-146261-1	JP3	Header, 100mil, 2x1, Gold plated, TH	
25	1	Texas Instruments	OPA2333AIDGKR	U6	OpAmp, 1.8V, Low Power, Low Drift	OPA2333
26	1	Texas Instruments	OPA313IDBVR	U2	OpAmp, Low Power, Low Noise, RRIO, 1MHz, 1.8V	OPA313
27	1	Texas Instruments	REF3325AIDBZT	U3	Ref, Voltage, 2.5V, 3.9uA, SC70-3	REF3325
28	15		N/A	C1, C11, C12, C14, C23, C24, C25, C26, R17, R18, R24, R26, R34, R37, U5	Uninstalled	

SPECIAL NOTES AND INSTRUCTIONS

END OF BOM

Figure A-2: Bill of Materials

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