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TI Precision Designs: Verified Design
High-Side Voltage-to-Current (V-I) Converter

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Circuit Description

This high-side voltage-to-current (V-I) converter delivers a well-regulated current to a ground-referenced load. The design utilizes a two-stage approach to allow the high-side current source to accept a ground-referenced input. The first stage uses an op amp and n-channel MOSFET to translate the ground-referenced input to a supply-referenced signal. The supply-referenced signal drives the second stage op amp that controls the gate of a p-channel MOSFET to regulate the load current.

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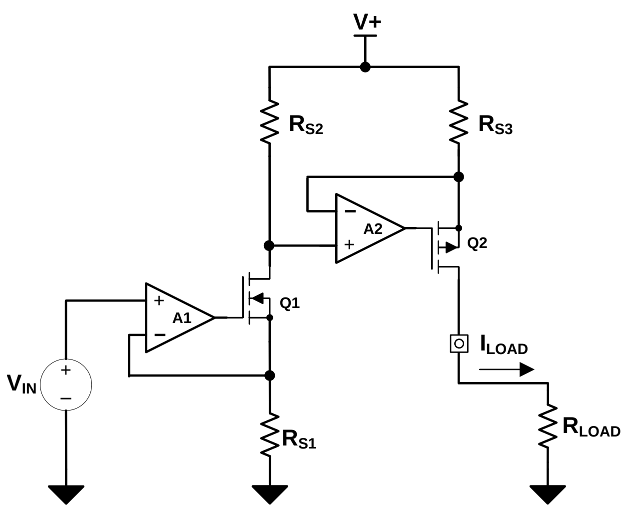

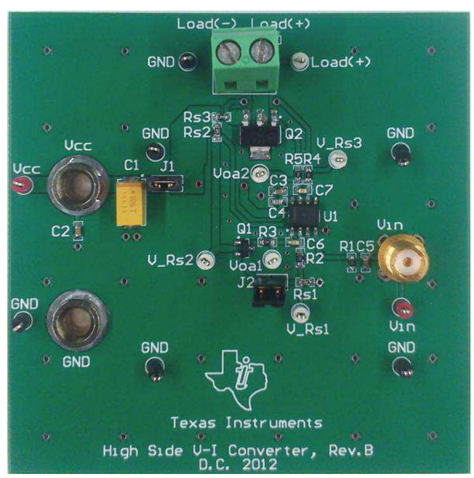

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1 Design Summary

The design requirements are as follows:

- Supply Voltage: 5 V dc
- Input: 0 V - 2 V dc
- Output: 0 mA - 100 mA dc

The design goals and performance are summarized in Table 1. Figure 1 depicts the measured transfer function of the design where Channel 1 is V_{IN} and Channel 2 is I_{OUT}.

Table 1. Comparison of Design Goal, Simulation, and Measured Performance

	Goal	Simulated	Measured
Offset (%FSR)	0.025	0.0000013	0.0001
Gain Error (%FSR)	0.1	0.102	0.0165
Efficiency (%)	98.5	98.974	98.96
Load Compliance (V)	4.5	4.5	4.508

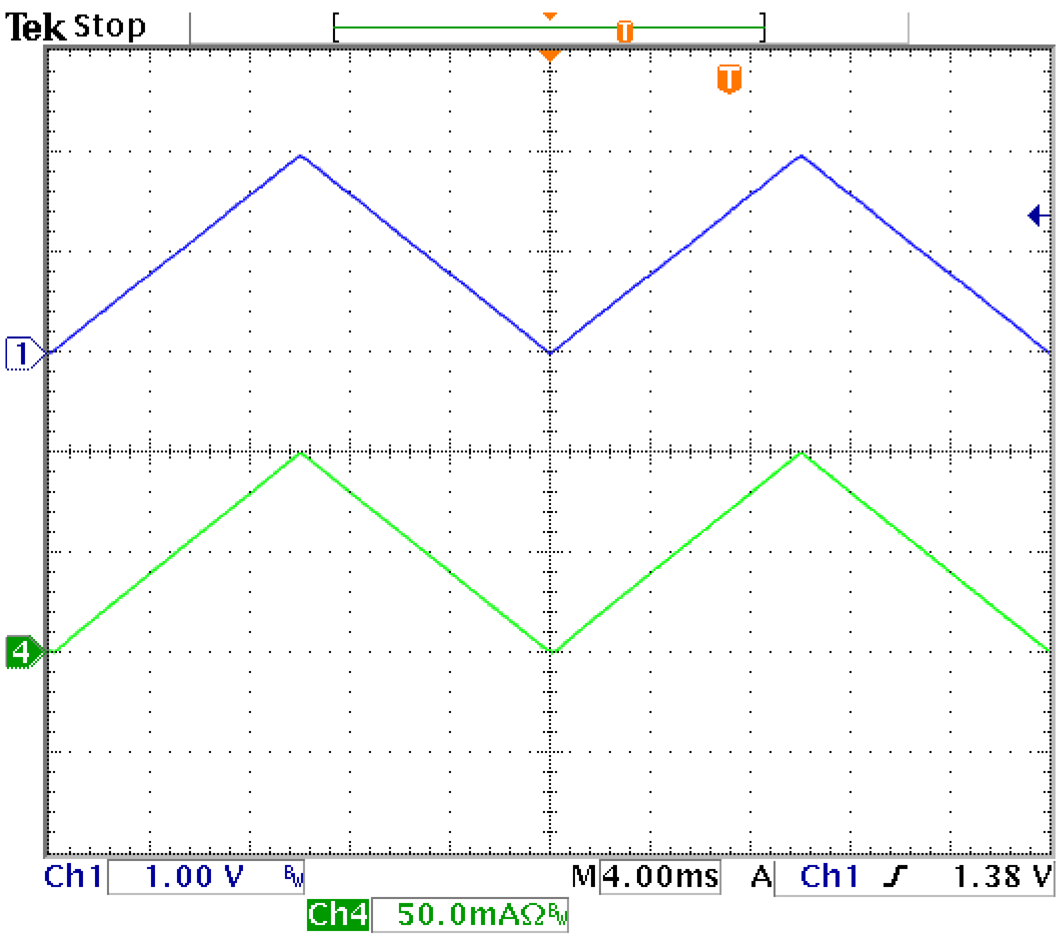

Figure 1. Measured Transfer Function of Design

2 Theory of Operation

A more complete schematic for this design is shown in Figure 2. The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, and the three current sensing resistors, R_{S1}, R_{S2}, and R_{S3}. The relationship between V_{IN} and R_{S1} will determine the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3}.

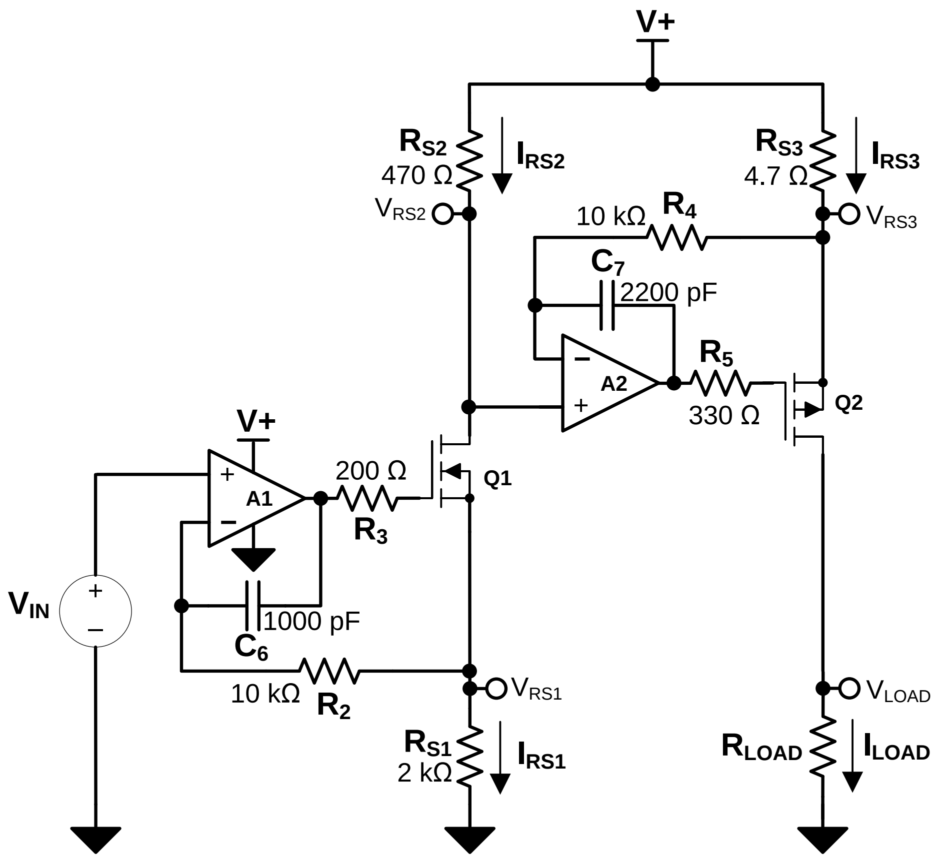

Figure 2. Complete Circuit Schematic

The transfer function of this design is defined in Equation 1:

$$I_{LOAD} = \frac{V_{IN} \times R_{S2}}{R_{S1} \times R_{S3}} \quad (1)$$

2.1 First Stage: Current Sink Design

The first stage of the circuit creates a current sink that produces a voltage drop across a high-side sense resistor, R_{S2}. This voltage drop is used to drive the second stage of the design.

The current sink is accomplished by placing a resistor, R_{S1}, in series with the n-channel MOSFET to sense the current through the first stage. The voltage drop across the R_{S1} resistor, V_{RS1}, is applied to the inverting input of the first op amp. Through negative feedback, the op amp will control the current through R_{S1} so that V_{RS1} will be set to the same voltage as V_{IN}, which is applied to the non-inverting input.

$$V_{RS1} = V_{IN} \quad (2)$$

Therefore at max current,

$$V_{RS1} = V_{IN} = 2\ V \quad (3)$$

The first stage of the circuit does not deliver power to the load, therefore all current used in the first stage directly reduces the efficiency of the circuit. To meet the efficiency goal of 98.5% while leaving headroom for the op amp quiescent current, the power dissipation in the first stage will be limited to 1% of the output current at full-scale. Therefore, the design should set the current in the first stage, I_{RS1}, to 1 mA when the output is at the full-scale value of 100 mA.

To select the value of R_{S1},

$$R_{S1} = \frac{V_{IN}}{I_{RS1}} = \frac{2\,V}{1mA} = 2\,k\Omega \tag{4}$$

The current flowing through the R_{S2} resistor, I_{RS2}, is ideally the same as the current flowing through I_{RS1}. There is a small error current present between the drain and the source of the n-channel MOSFET, but is insignificant under most circumstances.

$$I_{RS2} \cong I_{RS1} = 1mA \tag{5}$$

2.2 Second Stage: Current Source Design

The second stage of the circuit creates the output current source that will drive the load. The second amplifier that drives this stage is controlled by the voltage drop across the R_{S2} resistor, V_{RS2}, which is applied to the non-inverting input. A final sense resistor, R_{S3}, is placed in series with the output p-channel MOSFET to produce a voltage drop, V_{RS3}, proportional to the load current that flows through it. The V_{RS3} voltage is applied to the inverting input and through negative feedback, the amplifier will set V_{RS2} and V_{RS3} to be equal.

$$V_{RS3} \cong V_{RS2} \tag{6}$$

V_{RS3} subtracts from the output compliance voltage and should therefore be kept small to maximize the output voltage that can be delivered to the load. Select the value of R_{S2} to minimize V_{RS3} at full-scale to a value less than 500mV, allowing the compliance voltage goal of 4.5V to be accomplished.

$$R_{S2} = \frac{V_{RS3}}{I_{RS2}} = \frac{470\,mV}{1mA} = 470\,\Omega \tag{7}$$

Similar to the first stage, a very small error current is present between the current flowing through the R_{S3} resistor, I_{RS3}, and the current that flows through the load, I_{LOAD}, but is insignificant under most circumstances as well.

$$I_{LOAD} \cong I_{RS3} \tag{8}$$

To achieve the design goal of a 100 mA output at full-scale, select R_{S3}.

$$R_{S3} = \frac{V_{RS3}}{I_{LOAD}} = \frac{470\,mV}{100\,mA} = 4.70\,\Omega \tag{9}$$

2.3 Compensation Components

The first and second stages both require compensation components to ensure proper design stability. A thorough stability analysis is outside of the scope of this document and can be reviewed using the first reference in Section 9. The compensation components in the first stage are R2, R3, and C6, and the second stage uses R4, R5, and C7. The compensation scheme helps improve the circuit in two ways. First, the resistor placed between the output of the op amp and the MOSFET, R_{ISO}, helps isolate the amplifier from the capacitive load of the MOSFET gate. Second, the gain of the MOSFET is removed from the feedback loop at high frequencies by providing feedback directly from the op amp output to the inverting input through the feedback capacitor, C_F. This direct feedback loop replaces the dc feedback from the MOSFET drain through the feedback resistor, R_F. The frequency this transition occurs at is roughly based on the RC time constant formed from the values C_F and R_F. In general, the compensation components for this circuit are not set by fixed equations, but rather by choosing values and then manipulating them while observing the output response.

To experimentally determine values, the first step is to choose modest component values for the three components. Begin with 10 Ω for R_{ISO}, 10 kΩ for R_F, and 100 pF for C_F. Without using all three components, the circuit will not be stable and the next steps will not work. Apply a small-signal step response to the input of the circuit and observe the output of the op amp and the load current. Begin increasing the value of the series resistance between the op amp output and the MOSFET gate until a response with little ringing and overshoot has been achieved. Then begin increasing the value of the feedback capacitor until the final desired response is achieved. If the response becomes over-damped before overshoot, ringing, or oscillations are resolved, increase the series resistance further and begin the capacitor sizing process over. Analysis in this circuit is possible in simulation due to the availability of the SPICE models for the op amps and MOSFETs in this design.

3 Component Selection

3.1 Amplifier Selection

For a successful design, one must pay close attention to the dc characteristics of the op amp chosen for the application. To meet the performance goals, this application will benefit from an op amp with **low offset voltage**, **low temperature drift**, and **rail-to-rail output**.

The OPA2333 CMOS operational amplifier is a high-precision 5 uV offset, 0.05 µV/C drift amplifier optimized for low-voltage, single supply operation with an output swing to within 50 mV of the positive rail. The OPA2333 family uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift will reduce the offset error in the system, making these devices appropriate for precise dc control. The rail-to-rail output stage of the OPA2333 will ensure the output swing of the op amp is able to fully control the gate of the MOSFET devices within the supply rails.

3.2 MOSFET Selection

When selecting the n and p-channel MOSFETs for this design, it is important to ensure that the absolute maximum ratings are not exceeded. The primary specifications to design around will be the maximum gate-to-source voltage (V_{GS}), drain-to-source voltage (V_{DS}), and drain current (I_D). To ensure that the op amp used in the design can properly control the gate, a low threshold voltage ($V_{GS(TH)}$) is also desired. The SI2304DS n-channel MOSFET and NTF2955 p-channel MOSFET were chosen in this design to exceed these key specifications and avoid issues.

3.3 Passive Component Selection

The critical passive components for this design are the three resistors that are part of the transfer function, R_{S1}, R_{S2}, and R_{S3}. To meet the gain error design goal of 0.1% FSR, the tolerance of these resistors was chosen to be 0.1%.

The current in the first stage is multiplied in the second stage by the ratio of R_{S2} to R_{S3}. Therefore, accuracy in the first stage is very critical because errors will be multiplied and carried forward to the output by the second stage. Higher precision designs may therefore require lower tolerances for the R_{S1} resistor.

Other passive components in this design may be selected for 1% or greater as they will not directly affect the transfer function of this design.

4 Simulation

The TINA-TI™ schematic shown in Figure 3 includes the circuit values obtained in the design process.

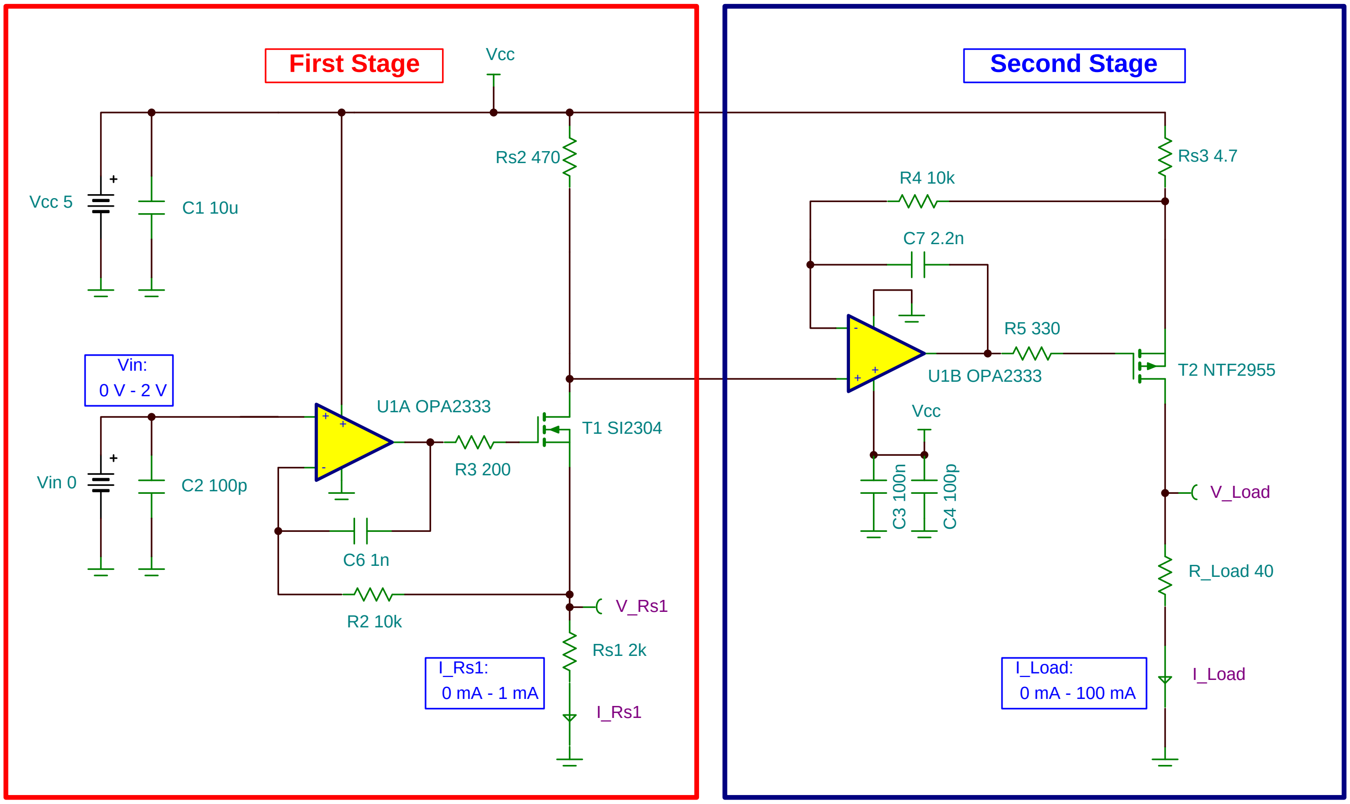

Figure 3. TINA-TI™ - Schematic

4.1 DC Transfer Function

The dc transfer function simulation results of the circuit in Figure 3 are shown in Table 2 and Figure 4. The results can be used to reference the voltage or current at a given node as a function of the input voltage.

Table 2. Simulated DC Transfer Function Results

Offset (nA)	1.267
Full-Scale I_{LOAD} (mA)	99.999
|Error| (mA)	0.001

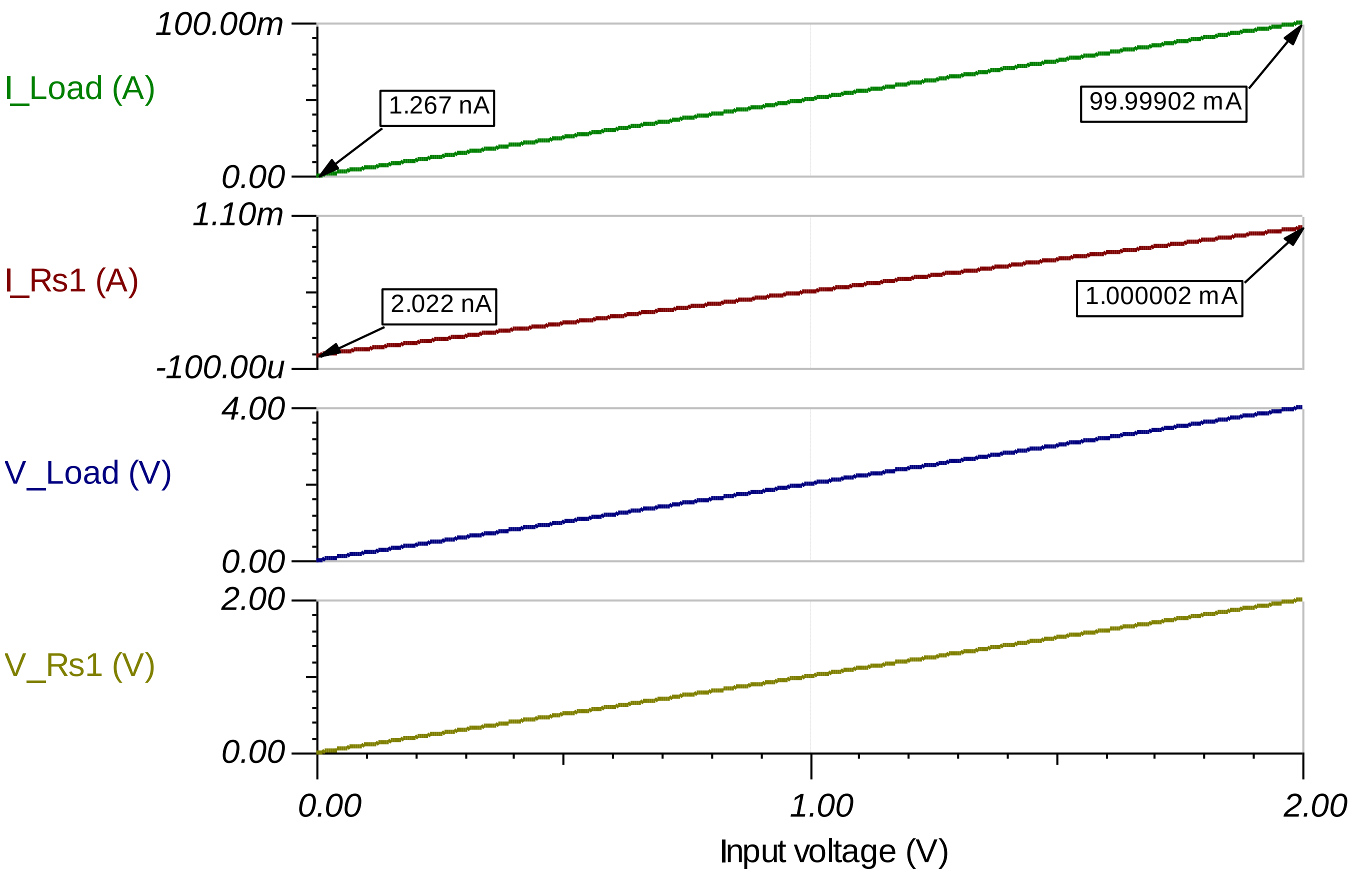

Figure 4. TINA-TI™ - DC Transfer Function

The system gain error from this simulation was determined using Equation 11:

$$\text{Gain Error (\%FSR)} = \frac{\left|\left(I_{LOAD\_IDEAL}(max) - I_{LOAD\_IDEAL}(min)\right) - \left(I_{LOAD}(max) - I_{LOAD}(min)\right)\right|}{\left(I_{LOAD\_IDEAL}(max) - I_{LOAD\_IDEAL}(min)\right)} \times 100 \tag{10}$$

$$\text{Gain Error (\%FSR)} = \frac{|100\text{ mA} - 99.99902\text{ mA}|}{100\text{ mA}} \times 100 = 0.001\,\% \tag{11}$$

The simulation results in Figure 4 were obtained using ideal passive components which reduces errors in the circuit to only the performance of the op amps and other active circuits in the design. More realistic simulation results can be obtained by running a Monte-Carlo simulation which will take into account the tolerance of the passive components.

Figure 5 displays the I_{LOAD} results of a twenty iteration Monte-Carlo dc sweep performed after entering the actual passive component tolerances. The statistical results of the Monte-Carlo simulation are summarized in Table 3.

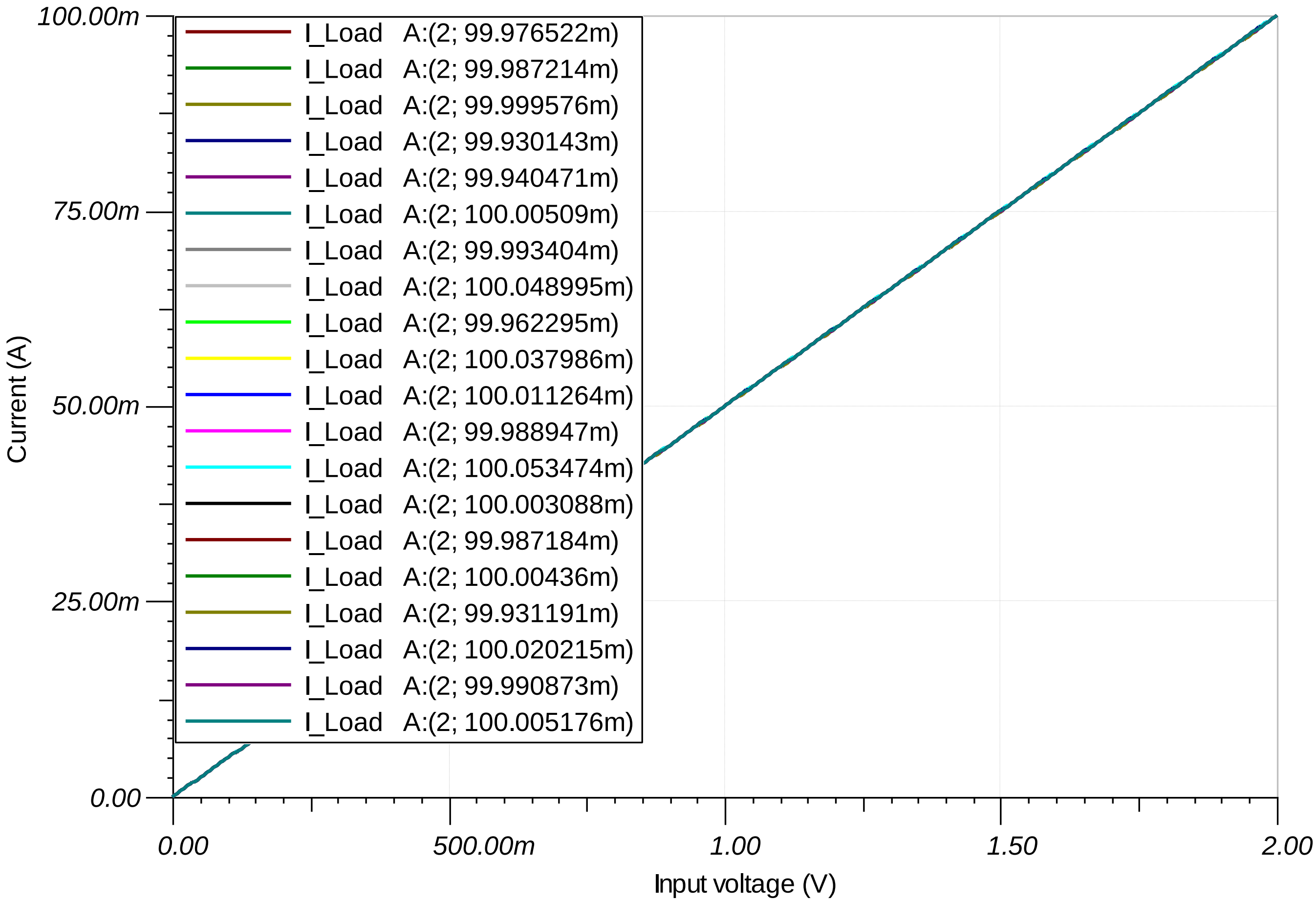

Figure 5. TINA-TI™ - I_{LOAD} Monte-Carlo DC Transfer Function

Table 3. Monte-Carlo DC Transfer Results

	Min	**Max**	**Average**	**Std. Dev (σ)**
Offset (nA)	1.267	1.267	1.267	0.0
Full-Scale (mA)	99.9301	100.0535	99.9939	0.0342
Full-Scale |Error| (mA)	0.0004	0.0699	0.0251	n/a

A more realistic range for the system gain error can be calculated by multiplying the standard deviation (σ) of the Monte-Carlo results by 3 which should cover 99.7% of the units, a 3-σ system. Therefore, a more realistic gain error range for the system is around 0.102% as shown in Equation 12.

$$\text{Gain Error (\%FSR)} = \left(\frac{3 \times \sigma}{\left(I_{LOAD}(\max) - I_{LOAD}(\min)\right)}\right) \times 100 = 0.102\ \% \tag{12}$$

4.2 Step Response

The step response of the design can be seen in Figure 6. The results show that the output of both stages settle to the proper values with little overshoot and ringing indicating a stable design.

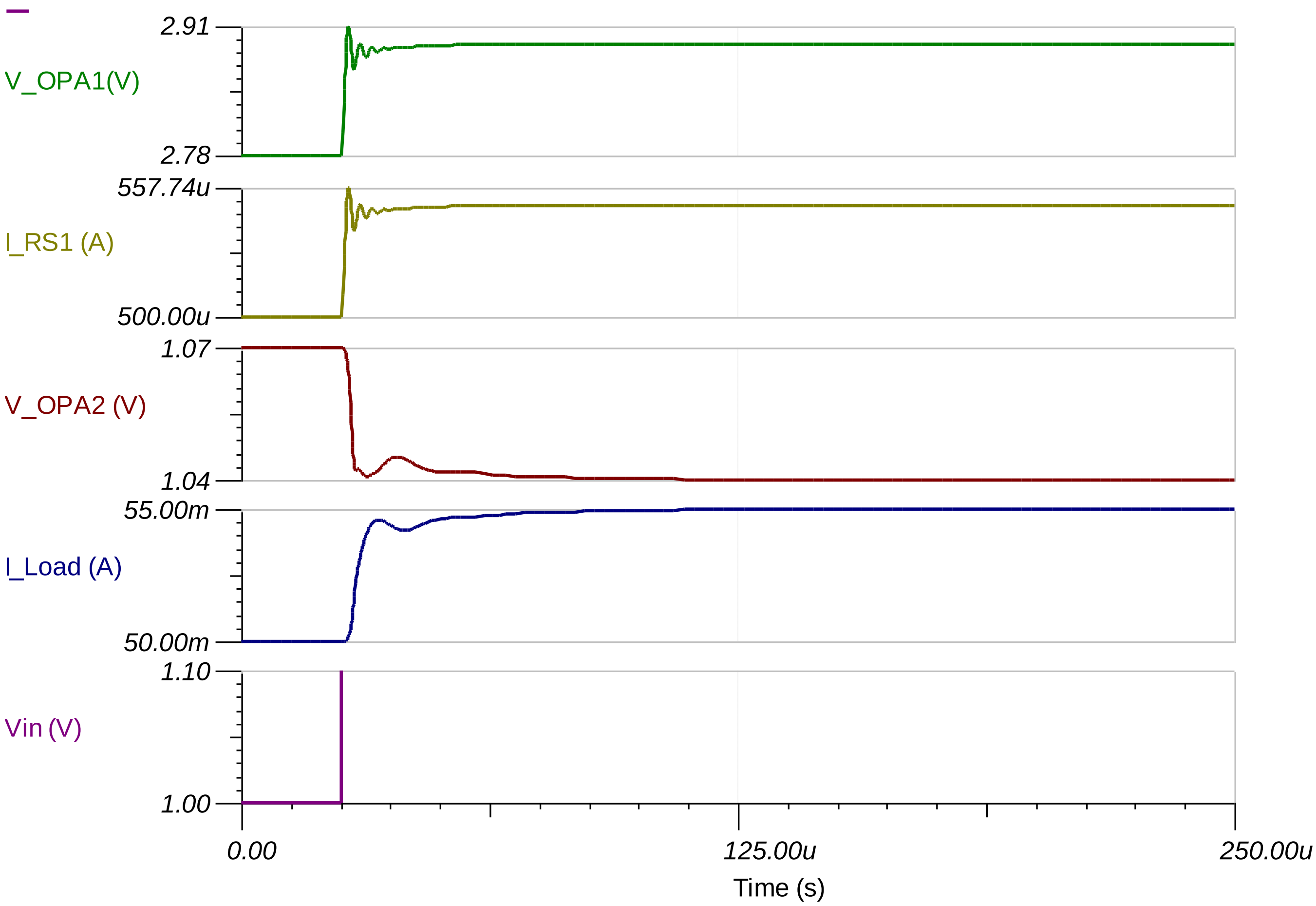

Figure 6. TINA-TI™ - Step Response

4.3 Compliance Voltage

To test the maximum compliance voltage and load resistance, the output was set to full-scale (100 mA) and the load resistor, R_{LOAD}, was swept from 0 Ω - 60 Ω. It was found that the output compliance voltage was 4.5 V and the maximum output resistance was 45 Ω as shown in Figure 7 below.

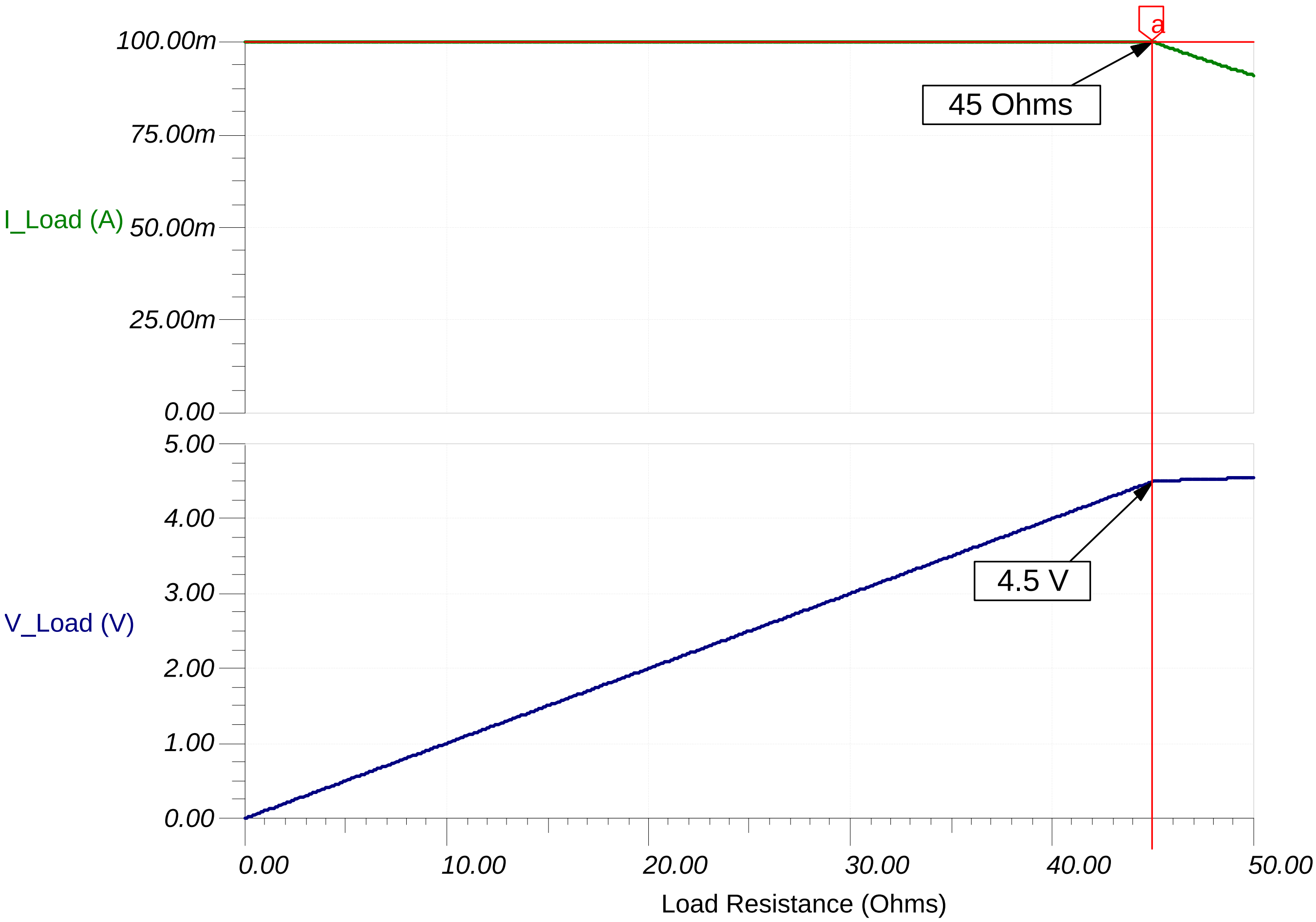

Figure 7. TINA-TI™ - Compliance Voltage and Maximum Load Resistance

4.4 Simulated Results Summary

Table 4. Comparison of Design Goal and Simulated Performance

	Goal	Simulated (Ideal Components)	Simulated (Monte-Carlo Components)
Offset (%FSR)	0.025	0.0000013	0.0000013
Gain Error (%FSR)	0.1	0.001	0.102
Efficiency (%)	98.5	98.974	98.974
Load Compliance (V)	4.5	4.5	4.5

5 PCB Design

The PCB schematic and bill of materials can be found in Section 10.1.

5.1 PCB Layout

PCB trace resistance is a primary concern in this design. When a PCB trace is in series with any of the current sensing resistors in this circuit, the parasitic PCB trace resistance will cause gain errors in the design. If this design is modified for higher current outputs or if the current sense resistor values are decreased, these parasitic resistances will cause larger errors in the circuit.

The PCB layout for this design, shown in Figure 8, features a Kelvin connection back to the op amp inputs for all three sense resistors. The Kelvin connection, also known as four-terminal sensing, separates sensing signals from power signals which eliminate voltage drops that are a result of PCB trace impedances. For proper operation of the second stage, the high side connections of R_{S2} and R_{S3} must be at the same voltage potential. To ensure this occurs, R_{S2} and R_{S3} were placed as physically close as possible to each other.

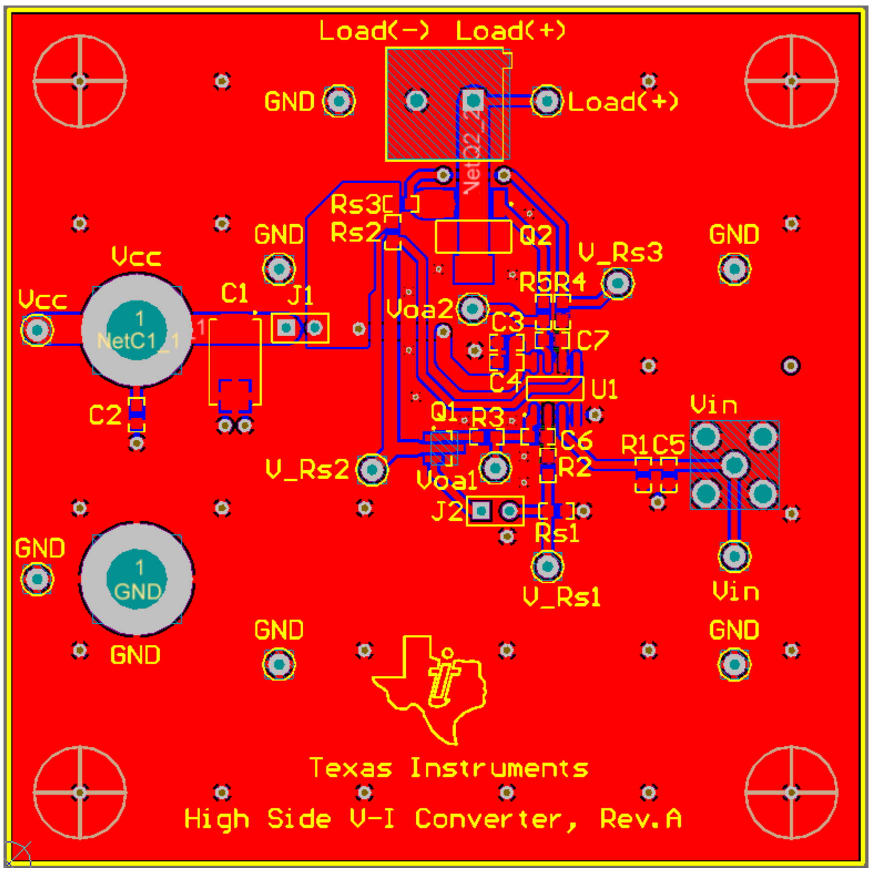

Figure 8. PCB Layout

6 Verification and Measured Performance

6.1 Transfer Function

Data was collected by sweeping V_{IN} from 0 V – 2 V dc while measuring the load current, I_{LOAD}. Figure 9 displays a plot of I_{LOAD} versus V_{IN}.

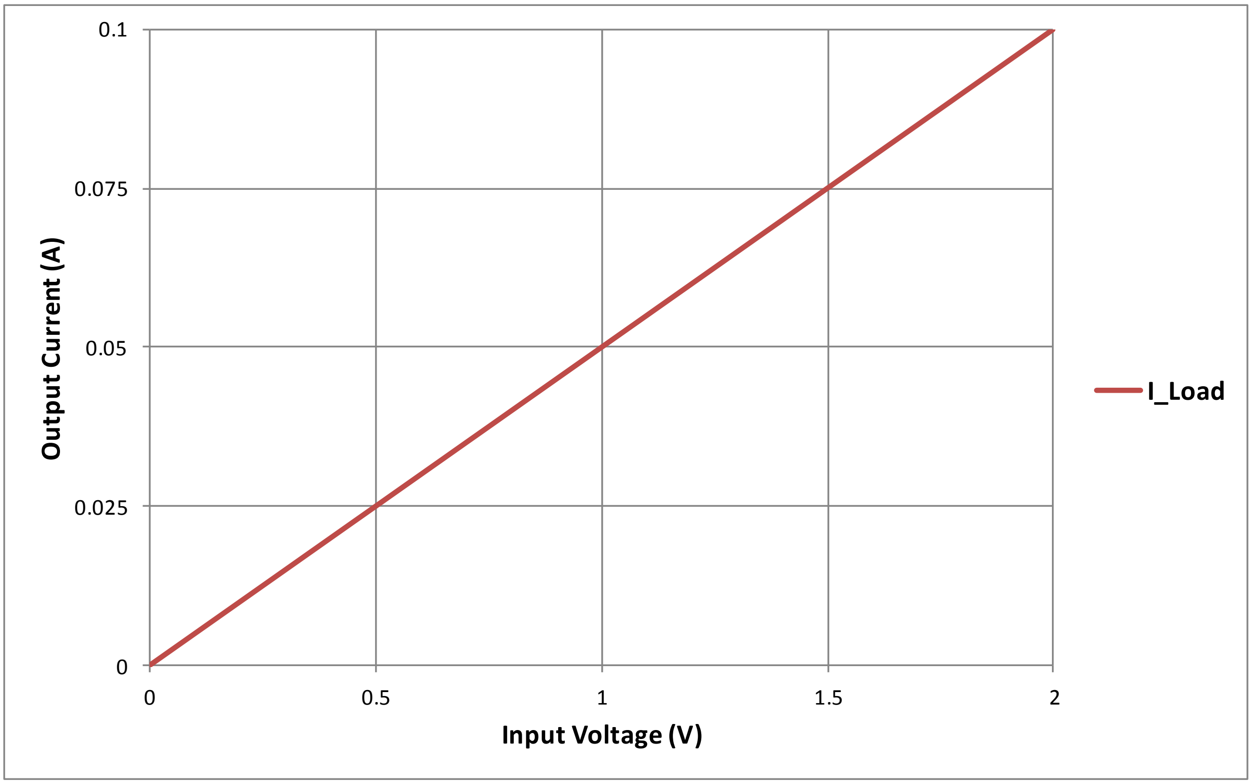

Figure 9.

To view the circuit errors more effectively over the span of measurement, the error current, I_{LOAD_ERROR}, was calculated by taking the difference between the calculated ideal current, I_{LOAD_IDEAL}, and I_{LOAD}. Also, the error current of the first stage, I_{RS1_ERROR}, was calculated by taking the difference between the calculated ideal current of the first stage, I_{RS1_IDEAL}, and I_{RS1}. The gain errors of both stages were calculated using similar equations to the one shown in Equation 11. The results are shown in Table 5 and Figure 10 and Figure 11.

Table 5. Measured DC Transfer Function Results

	First Stage	Second Stage
Offset (nA)	24	112
Full-Scale Current (mA)	0.9998	100.0165
|Error| (uA)	0.2	16.5
Gain Error (%)	0.02	0.0165

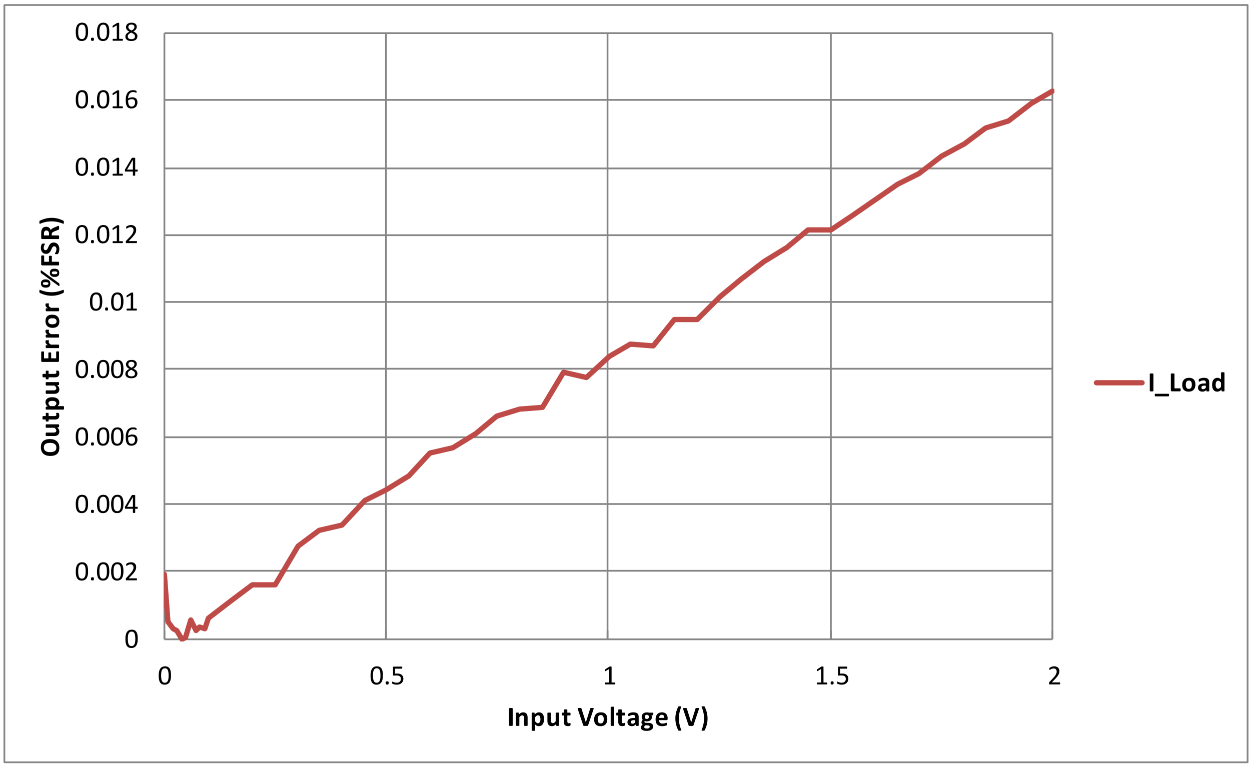

Figure 10. I_{LOAD_ERROR} versus V_{IN}

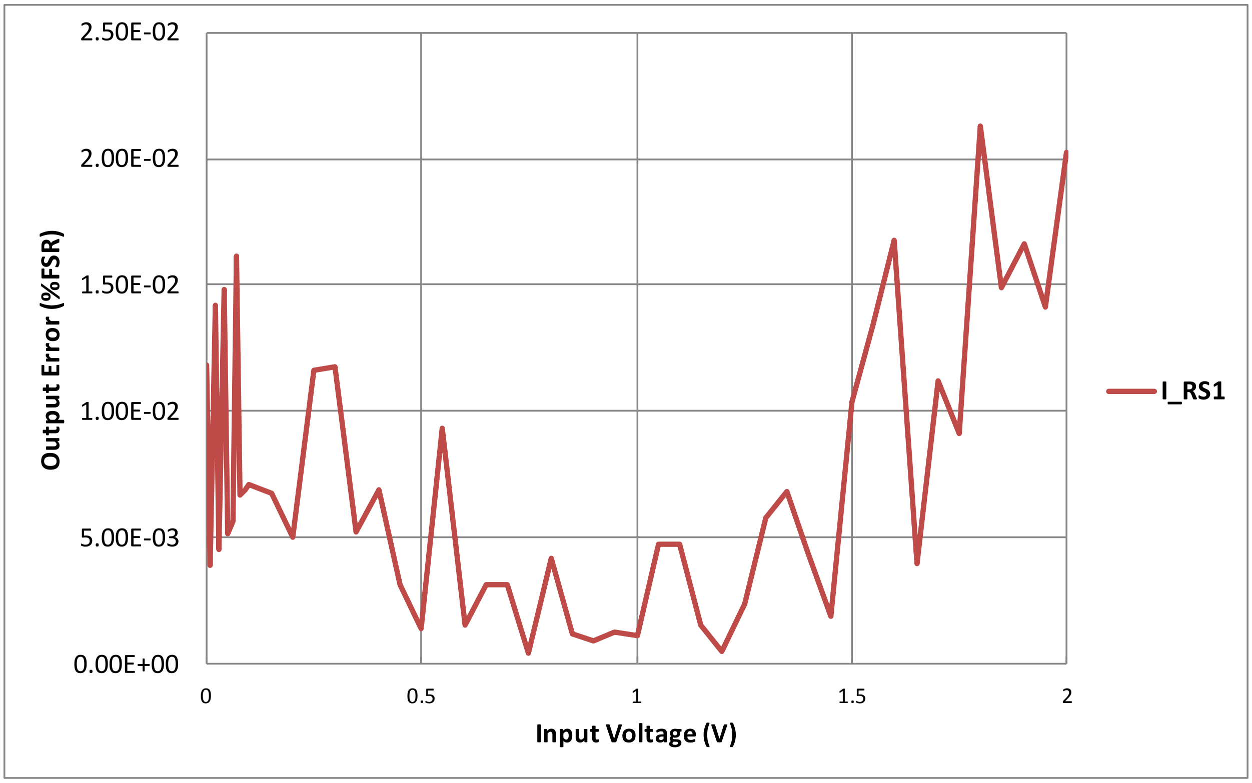

Figure 11. I_{RS1_ERROR} (%FSR) versus V_{IN}

6.2 Transient Response

To observe how the design reacts when a full-scale ramp is applied to the input, a full-scale 2 Vpp, 50 Hz triangle wave centered at 1 V dc was applied to V_{IN}. Figure 12 shows an oscilloscope screen capture of the input voltage and the output current through the load resistor, Channel 1 and Channel 4 respectively.

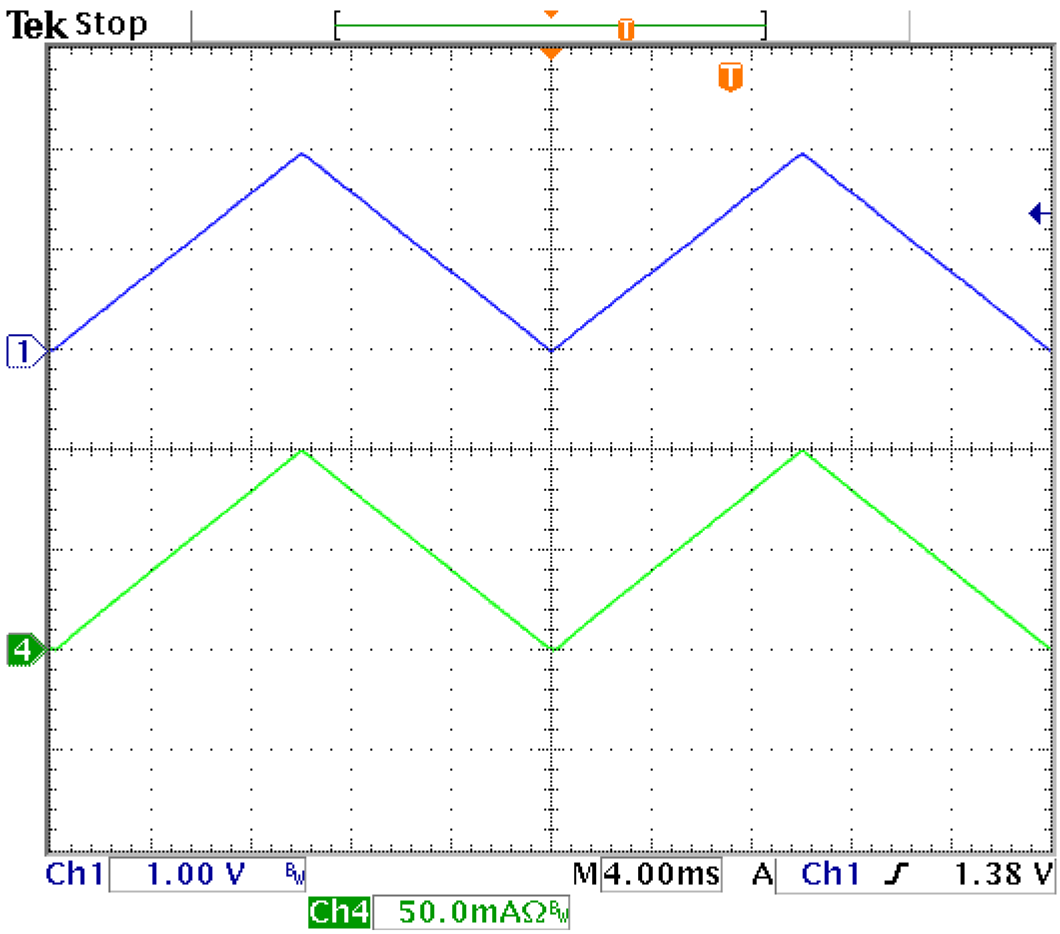

Figure 12. Full-Scale Triangle Wave Input

To observe the full-scale response and settling time of the design, a full-scale 2 Vpp, 1 kHz full-scale square wave centered at 1 V dc is applied to V_{IN}. Figure 13 shows an oscilloscope screen capture of the input voltage, Channel 1, and the output current through the load resistor, Channel 2.

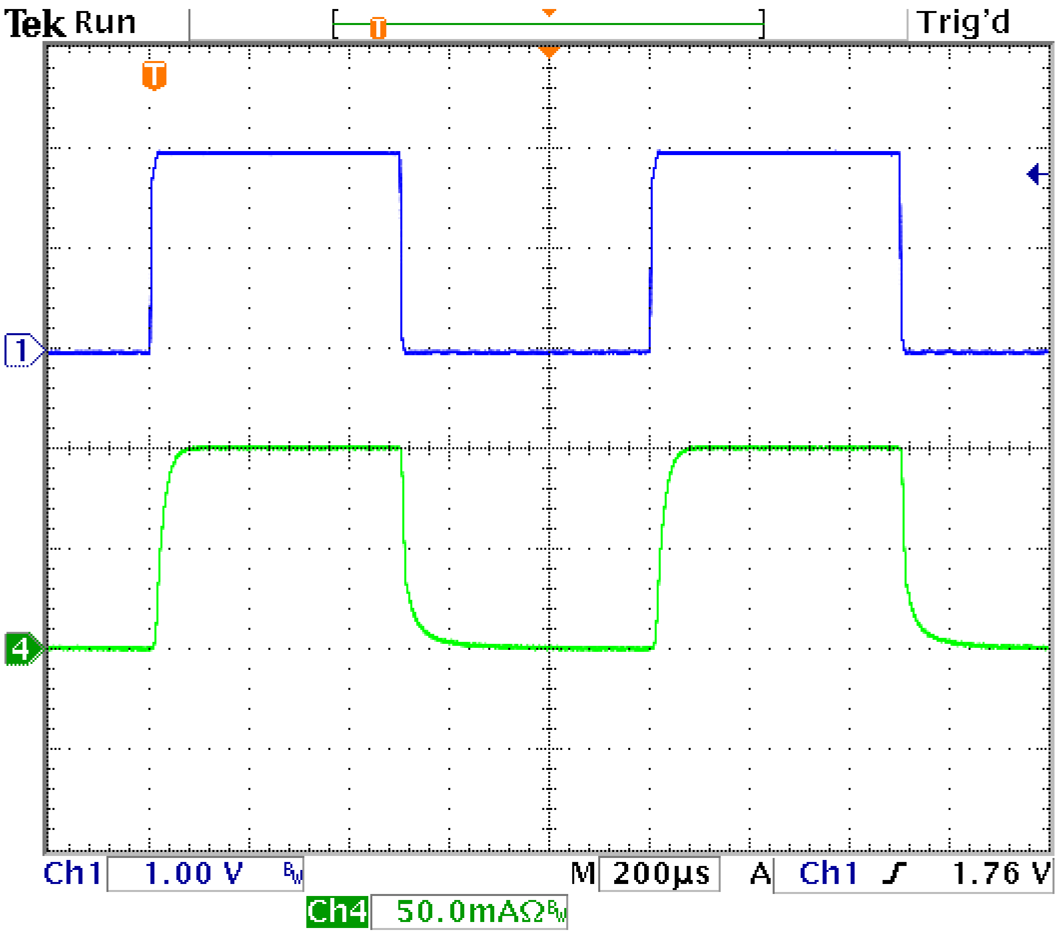

Figure 13. Full-Scale Settling Response

To test the small-signal stability of the design, a 500 mVpp, 1 kHz small-signal input step centered at 1 V dc was applied to V_{IN}. Figure 14 shows the resulting oscilloscope screen capture of the input voltage, Channel 1, the output voltage of the second op amp, V_{OA2}, Channel 2, the output of the first op amp, Channel 3, and the output current through the resistive load, Channel 4. The design quickly settles to the final value with a properly damped response without overshoot or ringing.

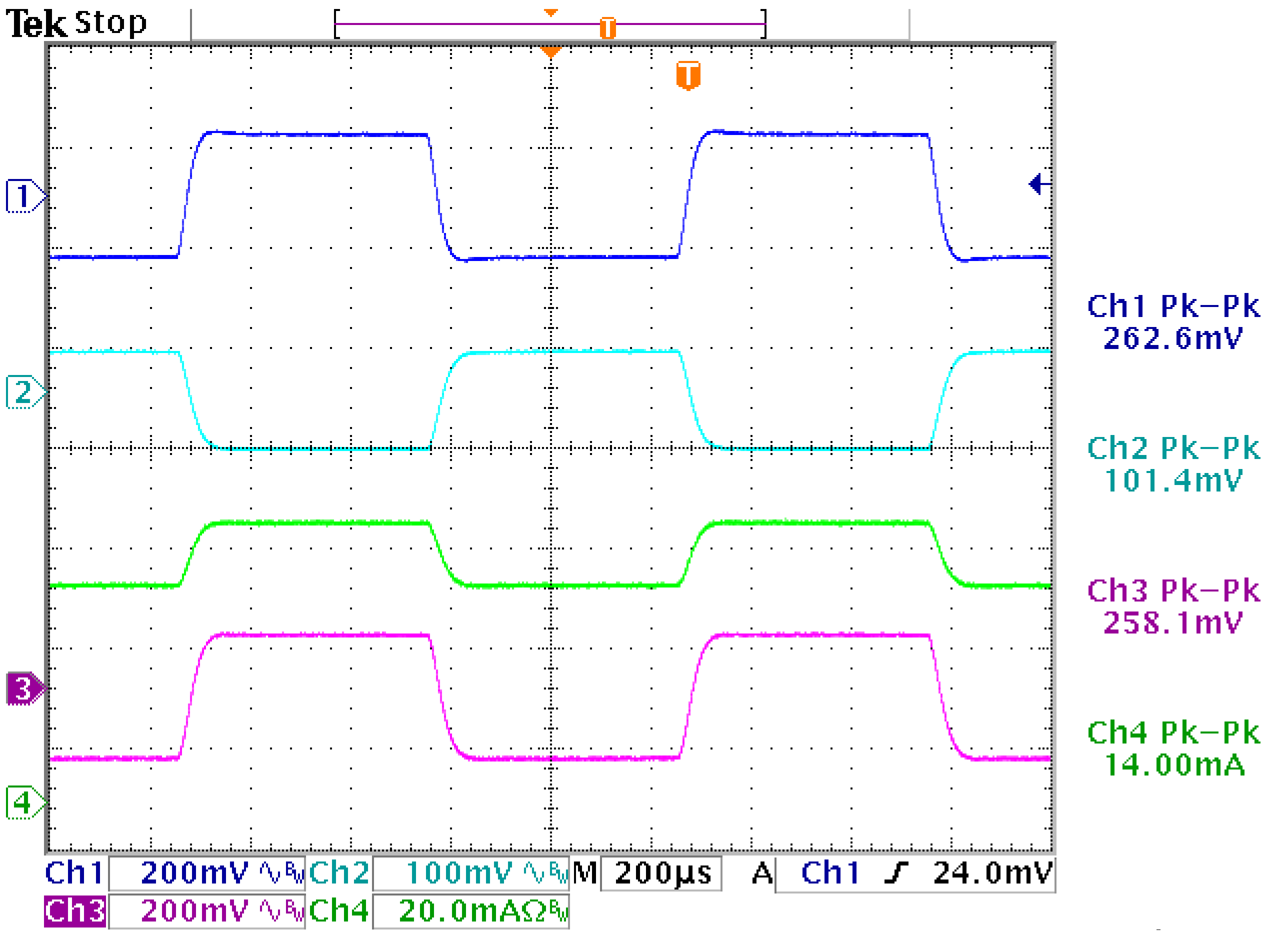

Figure 14. Small-Signal Stability

6.3 Output Compliance Voltage

The compliance voltage of the circuit is primarily based on the supply voltage, V_{CC}, the V_{RS3} voltage drop, and the saturation voltage of the p-channel MOSFET. To test the maximum compliance voltage, the output was first set precisely to 100 mA by adjusting the input voltage to overcome the errors of the circuit. Then a precision resistor box was used to sweep the R_{LOAD} value until the output current began to decrease. In this circuit, the maximum R_{LOAD} resistance was found to be 45.08 Ω before the output current began to decrease from 100 mA.

Based on measured maximum load resistance, the output voltage compliance, V_{COMP}, can be calculated based on Ohm's Law.

$$V_{COMP} = \frac{I_{LOAD}}{R_{LOAD}} \quad (13)$$

$$V_{COMP} = 4.508\ V \quad (14)$$

6.4 Measured Result Summary

A summary of the goals and measured results can be seen in Table 6

Table 6. Comparison of Design Goal and Measured Performance

	Goal	Measured
Offset (%FSR)	0.025	0.001
Gain Error (%FSR)	0.1	0.0165
Efficiency (%)	98.5	98.96
Load Compliance (V)	4.5	4.508

7 Modifications

The components selected for this design were based on the design goals outlined in Section 1. Selecting a chopper-stabilized amplifier such as the OPA2333 removes most of the dc errors normally attributed to the amplifier in this design. However, higher accuracy designs may be accomplished by reducing the resistor tolerance of the key components, R_{S1}, R_{S2}, and R_{S3}.

Although the zero-drift features of the OPA2333 will allow for little change in op amp performance over temperature, the other resistors in the design may drift substantially over the full range of -40 C – 125 C. Therefore, if the design is meant to operate over a wide temperature range, it is recommended to choose low temperature coefficient resistors in addition to low tolerances for the three sense resistors as well.

Modifying the design to allow for higher compliance voltages, and therefore larger resistive loads, requires a larger supply voltage. Since the maximum supply voltage of the OPA2333 is +5.5 V, higher voltages rule out the OPA2333 as a suitable candidate, and thus an amplifier with a higher maximum supply voltage will be required. Similarly, there are amplifier options that feature higher bandwidths or lower quiescent currents at the expense of other specifications. Table 7 summarizes some of the other potential amplifiers for this design as compared to the OPA2333.

Table 7. Brief Comparison of Alternate Amplifiers

Amplifier	Max Supply Voltage (V)	Max Offset Voltage (uV)	Max Offset Voltage Drift (uV/°C)	Bandwidth (MHz)	Quiescent Current (uA)
OPA2333	5.5	10	0.05	0.35	34
OPA2335	5.5	5	0.05	2	700
OPA2320	5.5	150	5	20	1600
OPA2735	12	5	0.05	1.5	1500
OPA2188	36	25	0.085	1	950

Care should be taken to ensure that the MOSFET and other components in the design are not overstressed when modifying the design for higher voltages or larger output currents.

Devices such as the XTR110 and XTR111 integrate the circuit shown in this design to create common industrial current loop outputs such as 4 – 20 mA and other similar ranges. These devices also feature voltage regulators, error flags, and other features that help create robust current loop output modules.

8 About the Authors

David F. Chan graduated from the Rochester Institute of Technology, where he earned a Bachelor of Science in Electrical Engineering Technology and a minor in both Management and Psychology. He joined Texas Instruments through the Applications Rotation Program, where he worked with the Precision Analog - Linear and the Analog Centralized Applications teams.

Collin Wells is an applications engineer in the Precision Linear group at Texas Instruments where he supports industrial products and applications. Collin received his BSEE from the University of Texas, Dallas.

9 References and Acknowledgements

1. Green, Tim, *Operational Amplifier Stability, Parts 1-11*, November 2008, http://www.en-genius.net/site/zones/acquisitionZONE/technical_notes/acqt_050712
2. R. Mark Stitt, "*Implementation and Applications of Current Sources and Current Receivers*" SBOA046, March 1990.

10 Appendix

10.1 Electrical Schematic and Bill of Materials

The electrical schematic and Bill of Materials for this design are respectively shown in Figure 15 and Figure 16.

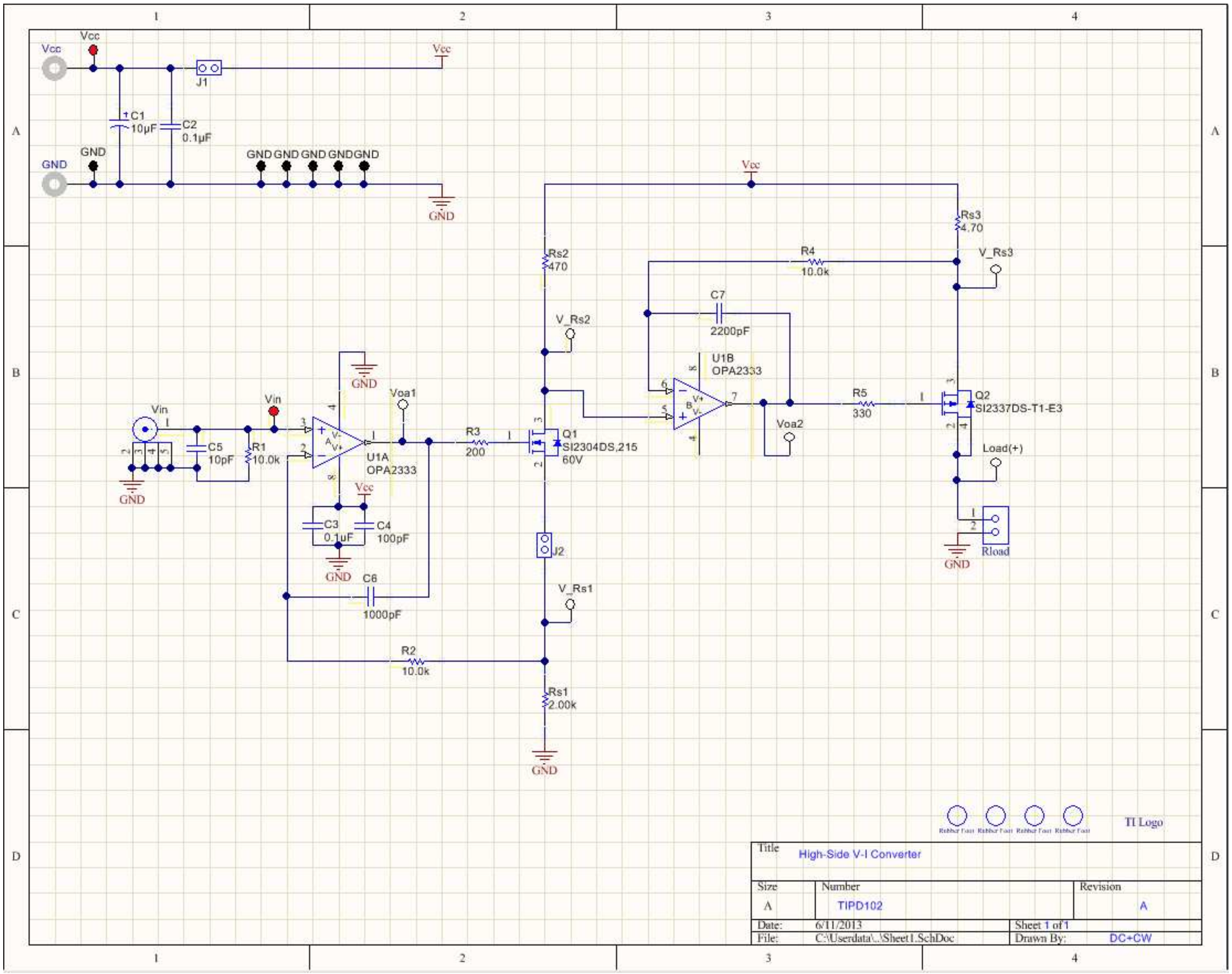

Figure 15. Electrical Schematic

Item #	Quantity	Value	Designator	Description	Manufacturer	Part Number	Supplier Part Number 1
1	1	10uF	C1	CAP, TANT, 10uF, 50V, +/-10%, 0.4 ohm, 7343-43 SMD	AVX	TPSE106K050R0400	478-3361-1-ND
2	2	0.1uF	C2, C3	CAP, CERM, 0.1uF, 100V, +/-10%, X7R, 0603	MuRata	GRM188R72A104KA35D	490-3285-1-ND
3	1	100pF	C4	CAP, CERM, 100pF, 100V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G2A101J	445-2306-1-ND
4	1	10pF	C5	CAP, CERM, 10pF, 50V, +/-5%, C0G/NP0, 0603	AVX	06035A100JAT2A	478-1163-1-ND
5	1	1000pF	C6	CAP, CERM, 1000pF, 100V, +/-5%, X7R, 0603	AVX	06031C102JAT2A	478-3698-1-ND
6	1	2200pF	C7	CAP, CERM, 2200pF, 50V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1H222J	445-1297-1-ND
7	4		F1, F2, F3, F4	BUMPON CYLINDRICAL .312X.200 BLK	3M	SJ61A1	SJ5746-0-ND
8	2		GND, Vcc	Standard Banana Jack, Uninsulated, 5.5mm	Keystone	575-4	575-4K-ND
9	2		J1, J2	CONN HEADER 2POS .100" SNGL SMD	Samtec	TSM-102-01-T-SV	TSM-102-01-T-SV-ND
10	1		Q1	MOSFET, N-CH, 30V, 4.5A, SOT-23	NXP Semiconductors	SI2304DS,215	568-5957-1-ND
11	1		Q2	MOSFET P-CH 60V 1.7A SOT-223	ON Semi	NTF2955T1G	NTF2955T1GOSCT-ND
12	1	10.0k	R1	RES, 10.0k ohm, 0.1%, 0.1W, 0603	Susumu Co Ltd	RG1608P-103-B-T5	RG16P10.0KBCT-ND
13	2	10.0k	R2, R4	RES, 10.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K0FKEA	541-10.0KHCT-ND
14	1	200	R3	RES, 200 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603200RFKEA	541-200HCT-ND
15	1	330	R5	RES, 330 ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-07330RL	311-330HRCT-ND
16	1	2.00k	Rc	RES, 2.00k ohm, 0.1%, 0.1W, 0603	Susumu Co Ltd	RG1608P-202-B-T5	RG16P2.0KBCT-ND
17	1		Rload	Conn Term Block, 2POS, 5.08mm PCB	Phoenix Contact	1715721	277-1263-ND
18	1	470	Rs1+	RES 470 OHM 1/6W 0.1% 0603 SMD	Susumu	RGH1608-2C-P-471-B	RGH16P470CT-ND
19	1	4.7	Rs2+	RES 4.70 OHM 1/16W 0.1% 0603	TE Connectivity	8-1614882-3	A103106CT-ND
20	2	Red	TP1, TP8	Test Point, TH, Miniature, Red	Keystone	5000	5000K-ND
21	6	Black	TP2, TP3, TP4, TP5, TP6, TP7	Test Point, TH, Miniature, Black	Keystone	5001	5001K-ND
22	6	White	TP9, TP10, TP11, TP12, TP13, TP14	Test Point, TH, Miniature, White	Keystone	5002	5002K-ND
23	1	OPA2333	U1	IC OPAMP CHOP R-R 350KHZ 8MSOP	Texas Instruments	OPA2333AIDGKR	296-22883-2-ND
24	1		Vin	Connector, TH, SMA	Emerson Network Power	142-0701-201	J500-ND

Figure 16. Bill of Materials

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