

ADS4449 EVM User Guide

This document serves as a user's guide for the ADS4449 Evaluation Module (EVM). The EVM provides a platform for evaluating the ADS4449, a quad-channel, 14-bit telecommunications analog-to-digital converter (ADC) operating at sampling rates of up to 250 MSPS. Designed for low-power consumption and high spurious free dynamic range (SFDR), the ADC has low-noise performance and outstanding SFDR over a large input-frequency range. The four ADC channels are separated into two blocks with two ADCs each.

This EVM is ideally suited for mating with the TSW1400 Capture Card for performing a data capture into a capture buffer, uploading the sample data to a PC, performing an FFT, and reporting on SNR, SFDR, and other performance metrics.

For more information regarding the ADS4449 and the related evaluation tools, please refer to the following:

- ADS4449 – Quad 14-bit 250-MSPS ADC ([SBAS603](#))
- TSW1400 – High-Speed Data Capture and Pattern Generation Platform ([SLWU079](#))
- ADS4449 EVM Configuration Software ([SLAC566](#)).

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1 Introduction

1.1 EVM Block Diagram

Figure 1 shows a simplified block diagram of the default configuration of the EVM. The four analog inputs are supplied to the EVM through a single-ended SMA connection, then transformer coupled, turning the single-ended signal into a balanced differential signal, and then input to the ADS4449. A dual transformer input circuit provides better phase and amplitude balance of the input signal when compared to the performance delivered by a single transformer input circuit.

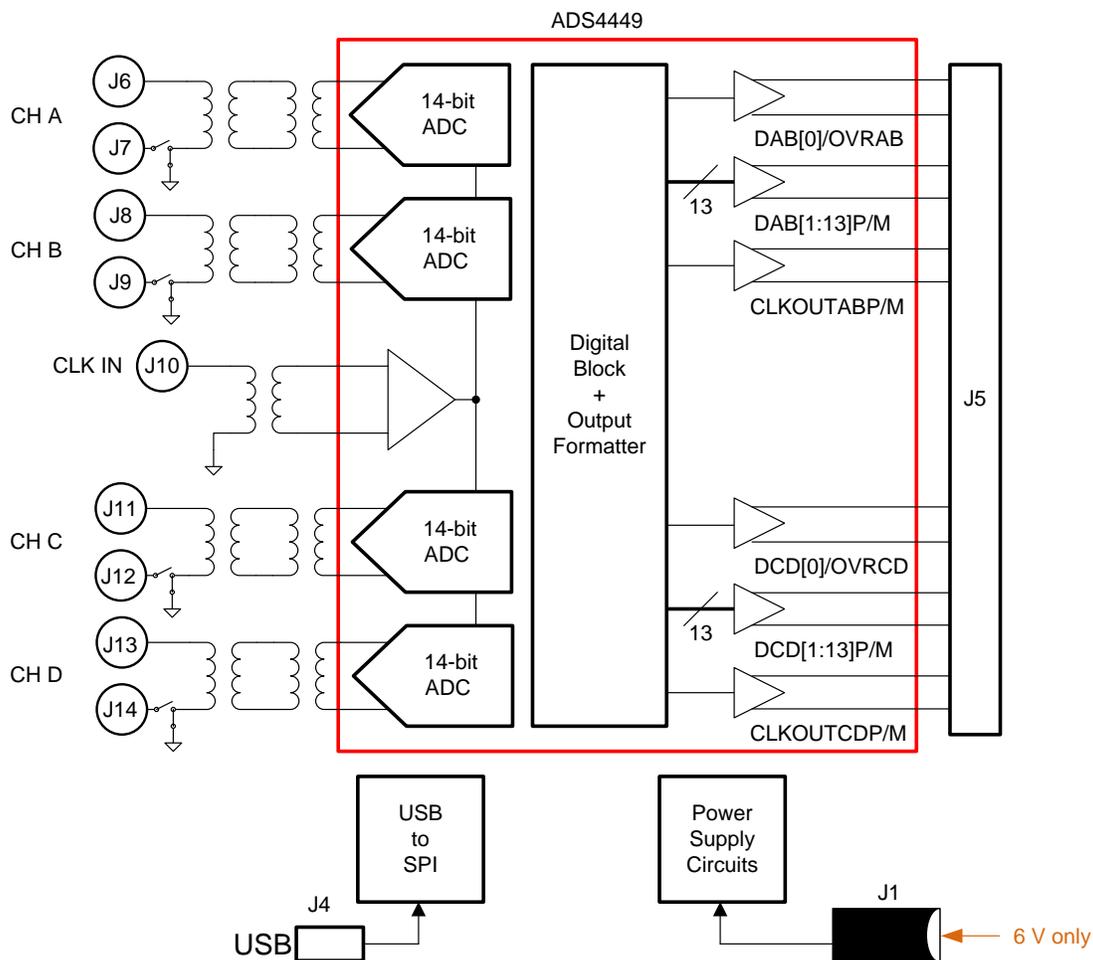


Figure 1. Simplified ADS4449 EVM Block Diagram

The clock input is supplied by way of a single-ended signal to an SMA connector and transformer coupled producing a differential clock signal for the ADS4449.

Power to the EVM is supplied by connecting the provide power cable between J1 of the EVM and a 6-VDC power supply capable of providing 3 amps. Banana jacks may also be used to supply power to the EVM. All necessary voltages for the ADS4449 are derived from the 6-V input connection.

1.2 EVM Power Supply

Figure 2 illustrates the power supply options available on the EVM. Jumpers are used to choose the power supply options, with the default jumper positions indicated by the darker portion of the jumper that represents the presence of the jumper. For jumper and feedback resistor configuration, see Table 1.

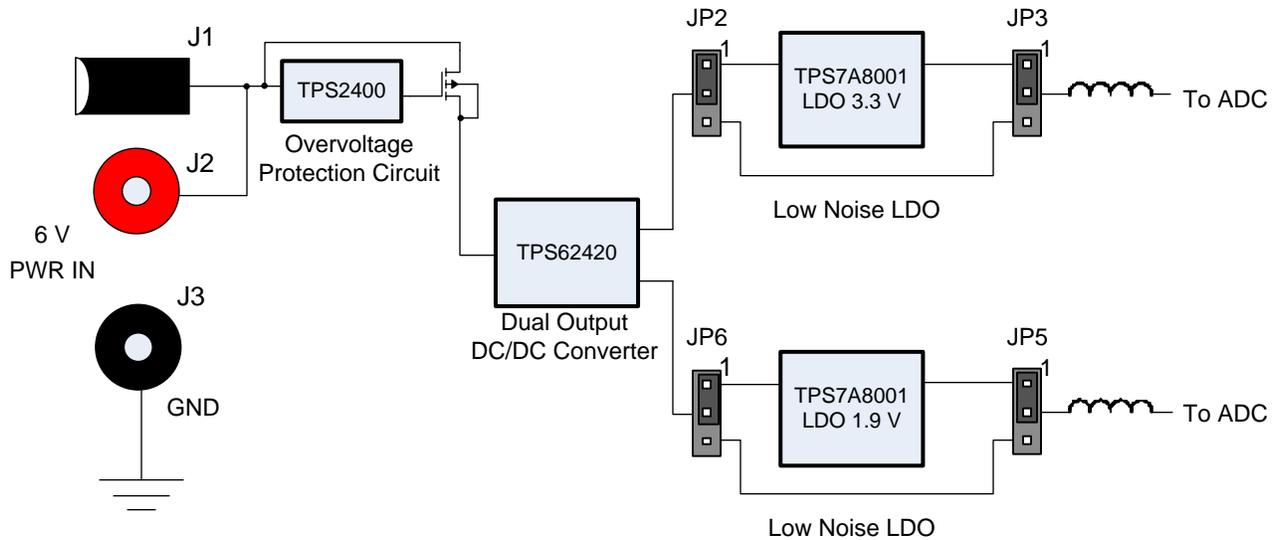


Figure 2. Simplified ADS4449 EVM Power Supply

Table 1. Power Supply Options

Power Supply Options	JP2	JP3	JP4	JP5	R3	R7	Comment
Option #1 (Default)	1-2	1-2	1-2	1-2	649 kΩ	536 kΩ	Dual outputs DC/DC converter supplies 3.85 V and 2.4 V to two low-noise LDOs. The low-noise LDOs output 3.3 V and 1.9 V, respectively.
Option #2	2-3	2-3	2-3	2-3	536 kΩ	390 kΩ	Low-noise LDOs are bypassed. DC/DC converter powers the ADC directly.

The default power path has an efficient dual output DC-DC switching power supply to first step down the input supplies for the low-noise LDOs. The low-noise LDOs generate the 3.3 V and 1.9 V for the ADC power.

The low-noise LDOs can be bypassed, allowing the DC/DC power supply to directly power the ADC. In this implementation, adjust the feedback resistors of the DC/DC converter accordingly.

1.3 EVM Connectors and Jumpers

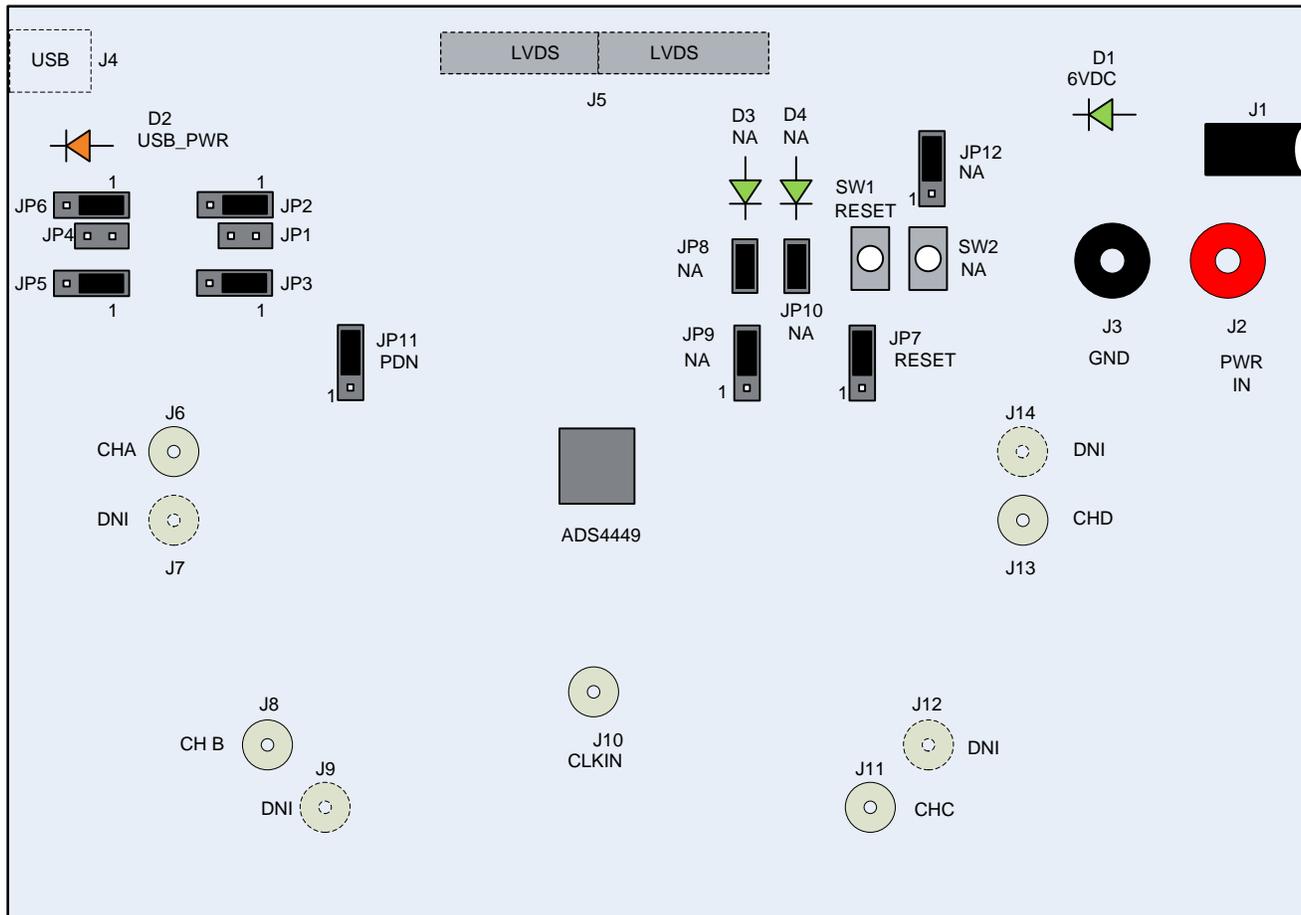


Figure 3. ADS4449 EVM Connector and Jumper Locations

The locations of the connectors, jumpers, pushbutton switches, and LEDs are shown in [Figure 3](#). The EVM has power connectors or banana jacks connecting the main power for power distribution. The SMA connectors connect the ADC input and ADC clock input to the ADC. Typically, the ADC inputs are transformer coupled, accepting single-ended connections. The input circuit can be configured to connect to two SMA connectors for differential signaling. [Table 2](#) lists the connector information for the EVM.

Table 2. ADS4449 EVM Connectors

Reference Designator	Description
J1	6 V (main) power input
J2	6 V (optional) power input
J3	Ground return
J4	USB Mini-B connector
J5	SAMTEC high-speed LVDS connector
J6	CH A input (positive)
J7	CH A input (negative) DNI
J8	CH B input (positive)
J9	CH B input (negative) DNI
J10	ADC clock input
J11	CH C input (positive)
J12	CH C input (negative) DNI

Table 2. ADS4449 EVM Connectors (continued)

Reference Designator	Description
J13	CH D input (positive)
J14	CH D input (negative) DNI

The on-board jumper options allow configuration of on-board power supplies and ADC options. Many of the jumper selections that involve DC inputs or static control signals are by way of push-on square post jumpers. The jumper options are listed in [Table 3](#). The table indicates the default settings of the jumpers as the EVM is normally shipped. Some of the jumpers are open circuit by default.

Table 3. ADS4449 EVM Jumper Options

Reference Designator	Default Setting	Function	Optional Setting	Function
JP1	DNI	Connects low-noise LDO (U2) input to main power input	N/A	
JP2	1-2	Connects DC/DC converter (U3) output to low-noise LDO (U2) input	2-3	Connects DC/DC converter (U3) output directly to the ADC
JP3	1-2	Connects low-noise LDO (U2) output to ADC	2-3	Connects DC/DC converter (U3) output directly to the ADC
JP4	DNI	Connects low-noise LDO (U4) input to main power input	N/A	
JP5	1-2	Connects DC/DC converter (U3) output to low-noise LDO (U4) input	2-3	Connects DC/DC converter (U3) output directly to the ADC
JP6	1-2	Connects low-noise LDO (U4) output to ADC	2-3	Connects DC/DC converter (U3) output directly to the ADC
JP7	2-3	Connects ADC RESET pin G6 to SW1 RESET switch	1-2	Connects ADC RESET pin G6 to DRVDD
JP8	1-2	N/A	Open	N/A
JP9	2-3	N/A	1-2	N/A
JP10	1-2	N/A	Open	N/A
JP11	2-3	Enables ADC	1-2	Power down the ADC or allows the ADC to standby (configured by CONFIG 0x45, bit D0)
JP12	2-3	N/A	1-2	N/A

There are two pushbuttons on the EVM. While JP7 is set in the 2-3 position, the pushbutton switch, SW1, provides a hardware reset to the ADS4449. Upon powering up, the ADC can either accept a hardware reset by pressing SW1 or by toggling the software reset switch on the EVM GUI. Pushbutton SW2 is not used. [Table 4](#) lists the descriptions of each pushbutton switch.

Table 4. ADS4449 EVM Pushbutton Switches

Reference Designator	Purpose
SW1	While JP7 is set in the 2-3 position, pressing SW1 resets the ADC. The ADC can be reset either by pressing SW1 or with a software reset in the GUI.
SW2	N/A

LED D1 is lit indicating the presence of the 6-V supply voltage to the EVM, while LED D2 is lit indicating the presence of the USB to serial converter power. LEDs D3 and D4 are not used. [Table 5](#) lists the description of each LED indicator.

Table 5. ADS4449 EVM LED Indicators

Reference Designator	Description
D1	When lit, D1 shows the presence of the 6-V (main) power supply

Table 5. ADS4449 EVM LED Indicators (continued)

Reference Designator	Description
D2	When lit, D2 shows the presence of the USB to serial converter power
D3	N/A
D4	N/A

1.4 EVM ADC Input Circuit Configurations

Figure 4 shows the ADS4449 ADC input circuit. The default setup has a dual 1:1 impedance ratio transformer input circuit, which achieves better phase and amplitude balance of the input signal than is typically produced by a single transformer input circuit. Third-order bandpass filter component pads are available for installing bandpass filter components. The default components for the bandpass filter are either zero Ω or open circuit.

The default input termination is 50 Ω , which is formed by two 25- Ω resistors connected to the ADC VCM node. If the user chooses to use 100- Ω termination with the 1:2 impedance transformer, the optional RLR differential arm can be used to tune the in-band flatness.

The ADC analog input consists of a switched-capacitor-based, differential sample-and-hold (S/H) architecture. Due to the opening and closing of the sampling glitches, the kick-back noise from the S/H circuit may affect the ADC performance. Besides the on-chip R-C filter of the ADC input, the external RLCR circuit provides additional filtering of the glitches. The default RLCR components have been optimized for input bandwidth centered at 185 MHz.

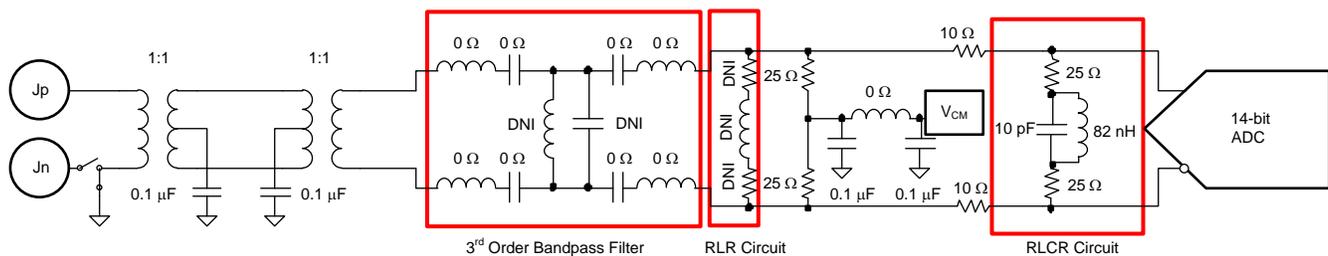


Figure 4. ADS4449 ADC Input Circuit

Figure 5 shows the ADS4449 clock input circuit. The clock signal goes through the 1:4 impedance ratio transformer increasing the clock amplitude by two (1:4 impedance ratio equals to 1:2 voltage ratio). The two 121- Ω resistors will impedance transform back to the primary side as 50- Ω load impedance for the signal source generator. For ADC evaluation, set the signal generator output to 10 dBm.

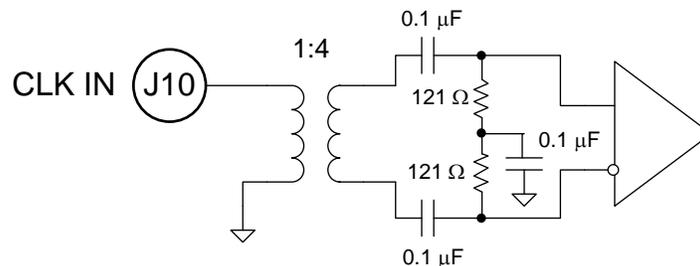


Figure 5. ADS4449 Clock Input Circuit

2 Software Control

2.1 Installation Instructions

- Open the ADS4449_Installer_vxpx folder (xpx represents the latest version, which is 2.0 at the time of

this writing)

- Run Setup.exe
- Follow the on-screen instructions
- Once installed, launch by clicking on the ADS4449_GUI_vxpx program in Start → All Programs → Texas Instruments ADCs
- When plugging in the USB cable for the first time, the Found-New-Hardware-Wizard prompts to install the USB drivers
 - When a pop-up screen opens, select *Continue Downloading*
 - Follow the on-screen instructions to install the USB drivers
 - If needed, access the drivers directly in the install directory

2.2 Software Operation

The ADS4449 EVM GUI software allows programming control of the ADS4449 device. The front panel provides a tab for common control of the ADS4449. The GUI tabs provide a convenient and simplified interface to the most-used registers of each device.

2.2.1 Control Options

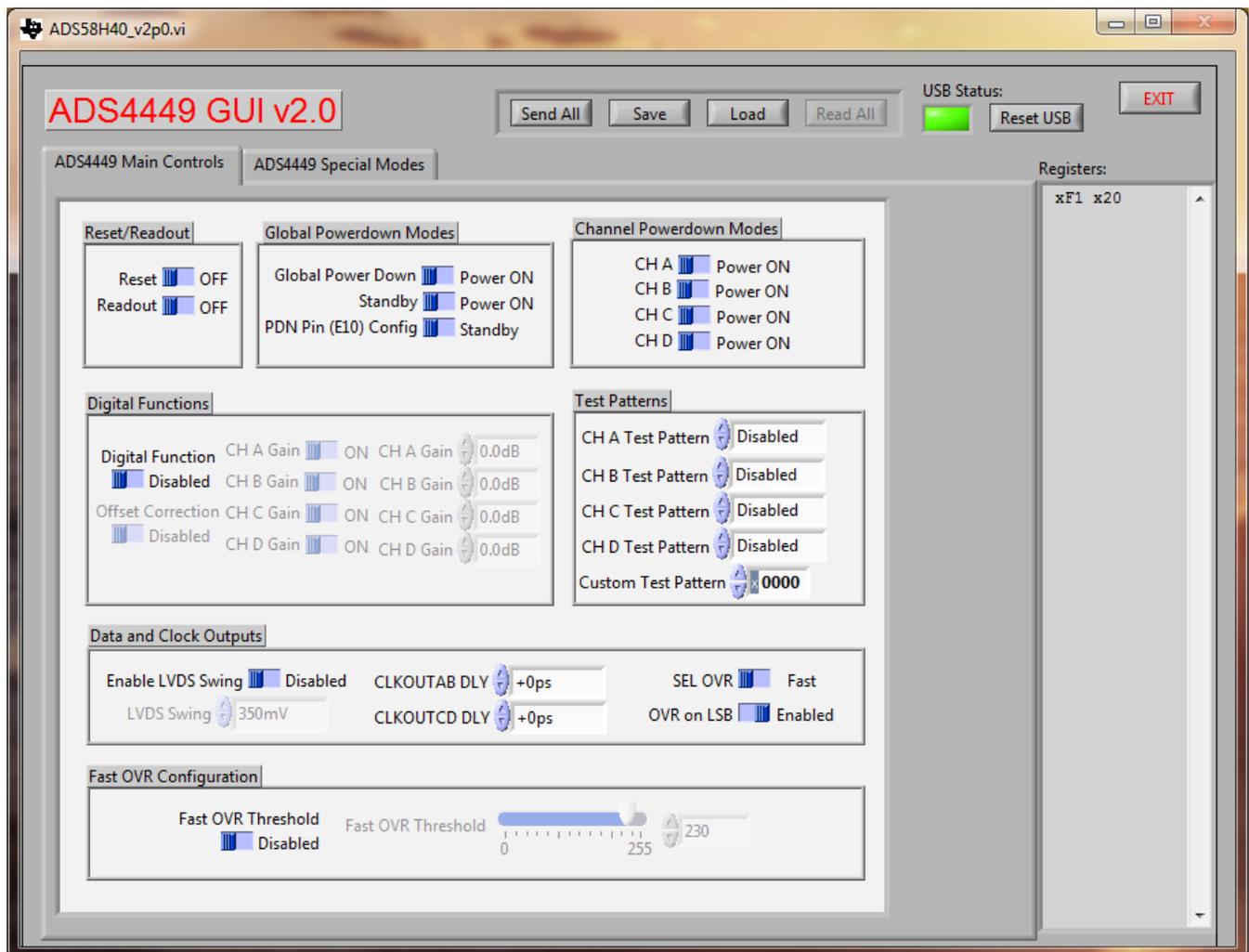


Figure 6. ADS4449 Main Control Panel

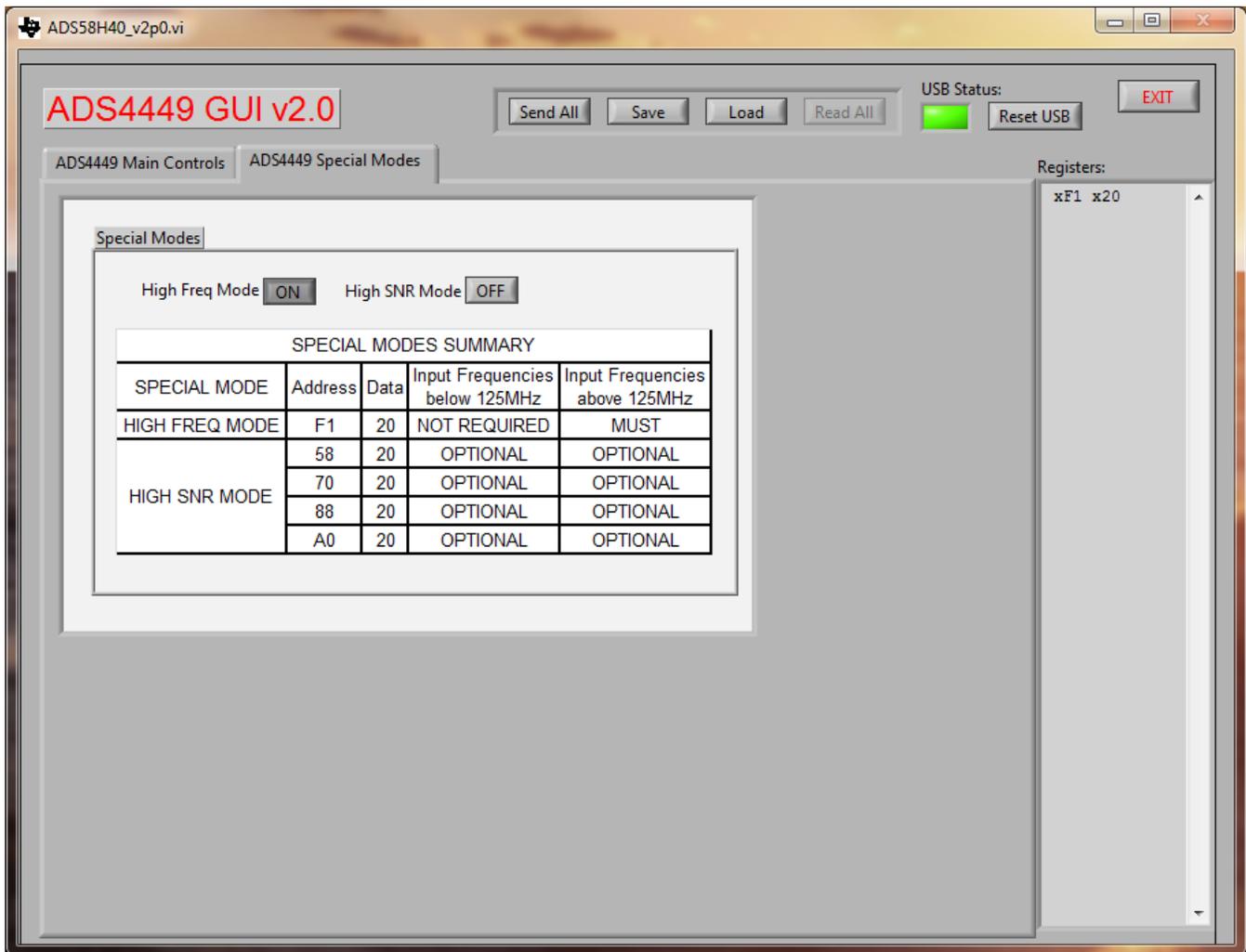


Figure 7. ADS4449 Special Modes Panel

2.2.2 Register Control

- **Send All:** Sends the register configuration to all devices
- **Save Regs:** Saves the register configuration for all devices
- **Load Regs:** Load a register file for all devices.
 - Select *Load Regs* button
 - Double click on the *data* folder
 - Double click on the desired register file
 - Click *Send All*, ensuring all of the values are loaded properly

2.2.3 Miscellaneous Settings

- **Reset USB:** Toggle this button if the USB port is not responding. This generates a new USB handle address
 - Note:** Reset the board after every power cycle and click the **Reset USB** button on the GUI
- **Exit:** Stops the program

3 Basic Test Procedure

This section outlines the basic test procedure for testing the EVM.

3.1 Test Block Diagram

The test set-up for evaluation of the EVM with the TSW1400 Capture Card is shown in Figure 8. As seen in this figure, the evaluation setup involves a clock from a high-quality signal generator and a sine wave for the analog input from a high-quality signal generator. High-order, narrow-bandpass filters are usually required on clock and input frequency to remove phase noise and harmonic content from the input sine waves. If the two signal generators are not synchronized by an external reference signal to make the clock and input frequency coherent, then the resulting FFT first needs a windowing function, such as Hanning or Blackman-Harris, applied to the data.

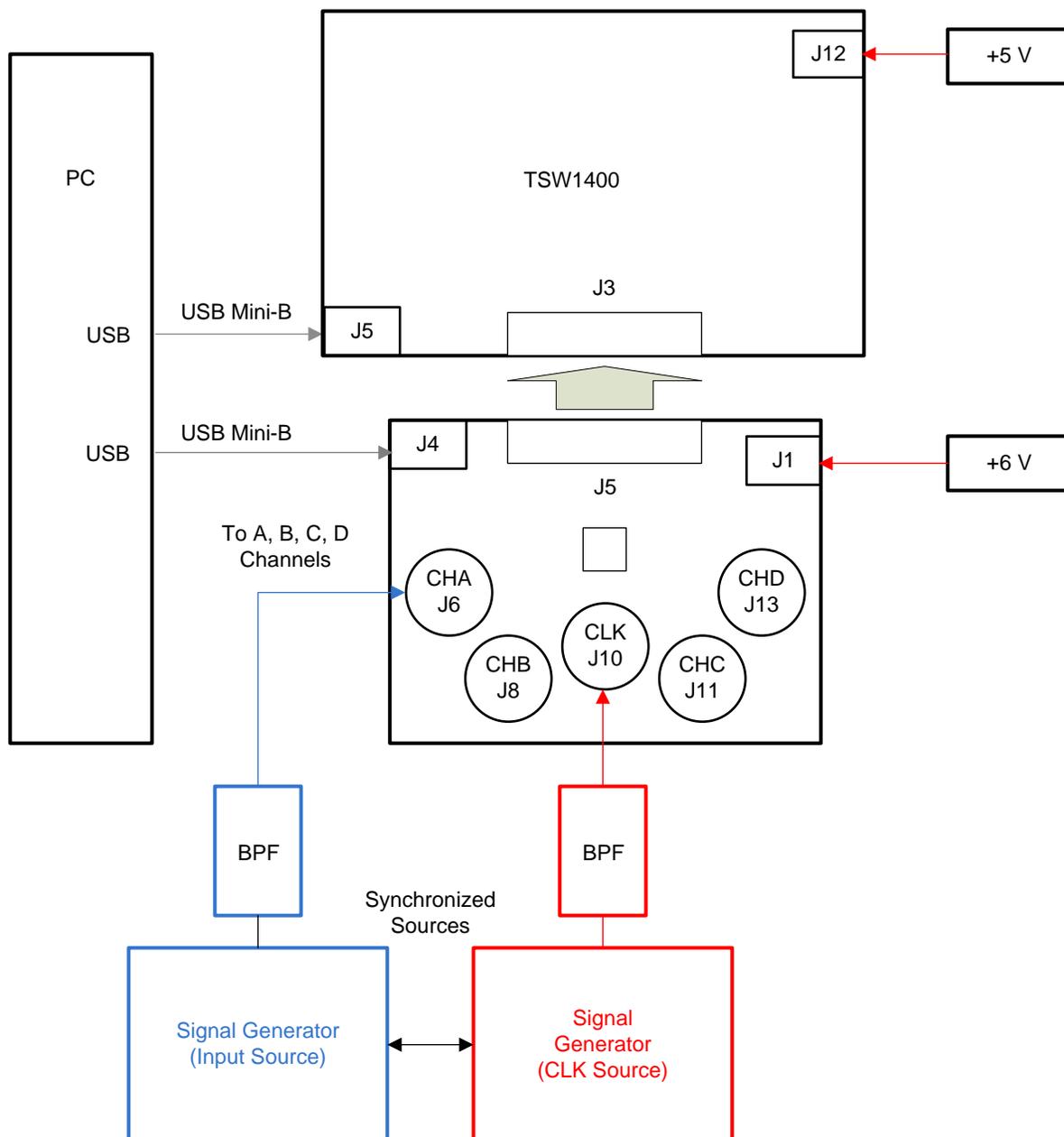


Figure 8. ADS4449 and TSW1400 Test Setup Block Diagram

3.2 Test Set-up Connection

1. Connect the J5 connector of the EVM to the J3 connector of TSW1400 EVM
2. Connect 5 V to the J12 supply input connector of the TSW1400 and 6 V to the J1 supply input connector of the EVM
3. Provide a sample clock at J10 SMA connector of the EVM
4. Provide a sine wave for the analog input at J6, J8, J11, or J13 SMA connectors of the EVM
5. Connect a USB cable from the TSW1400 to the programming computer
6. Connect a USB cable from the EVM to the computer
7. Ensure the initial jumper settings of ADS4449, as per [Table 3](#) (if default usage of the ADS4449 is desired)

3.3 ADS4449 Software Quick Start Guide

[Figure 6](#) introduced the front panel of the ADS4449 SPI GUI. This section covers the initial use of the SPI GUI necessary for most evaluations of the ADS4449.

1. Press the **Reset USB Port** button if the USB connection has been disrupted since last use, or if an error message pops up warning that the USB connection is not valid.
2. Use the mouse to select the *reset* position of the reset switch. This switch is self-clearing.
3. Press **Send All** to send all the register settings.
4. From this point, select digital functions as desired such as High Frequency Mode, High SNR Mode, or set test pattern modes if desired. All register bits listed in the register map of the ADS4449 data sheet have a *switch* on the front panel of the SPI GUI for easy configuration of the ADS4449.

Note that any greyed-out front panel switches are unavailable for use because they have a dependency upon other switch settings, as indicated in the ADS4449 datasheet. For example, the Channel A Gain selection is unavailable because the default state of the Channel A Gain Enable switch is off. Select the Channel A Gain Enable switch, toggling the switch to the enabled state, and then the Channel A Gain selection becomes available for use.

3.4 ADS4449 and TSW1400 Setup Guide

Reference the TSW1400 User's Guide ([SLWU079A](#)) for more detailed explanations of the TSW1400 set-up and operation. This document assumes the High Speed Data Converter Pro software and the TSW1400 hardware are installed and functioning properly. This EVM requires High Speed Data Converter Pro software version 2.09 with TSW1400 hardware of Rev D (or higher).

Single-tone FFT test (ADS4449 11-bit Operating Mode)

1. Start the High Speed Converter Pro GUI program. When the program starts, select the ADC tab and then select the ADS4449 device in the Select ADC menu.

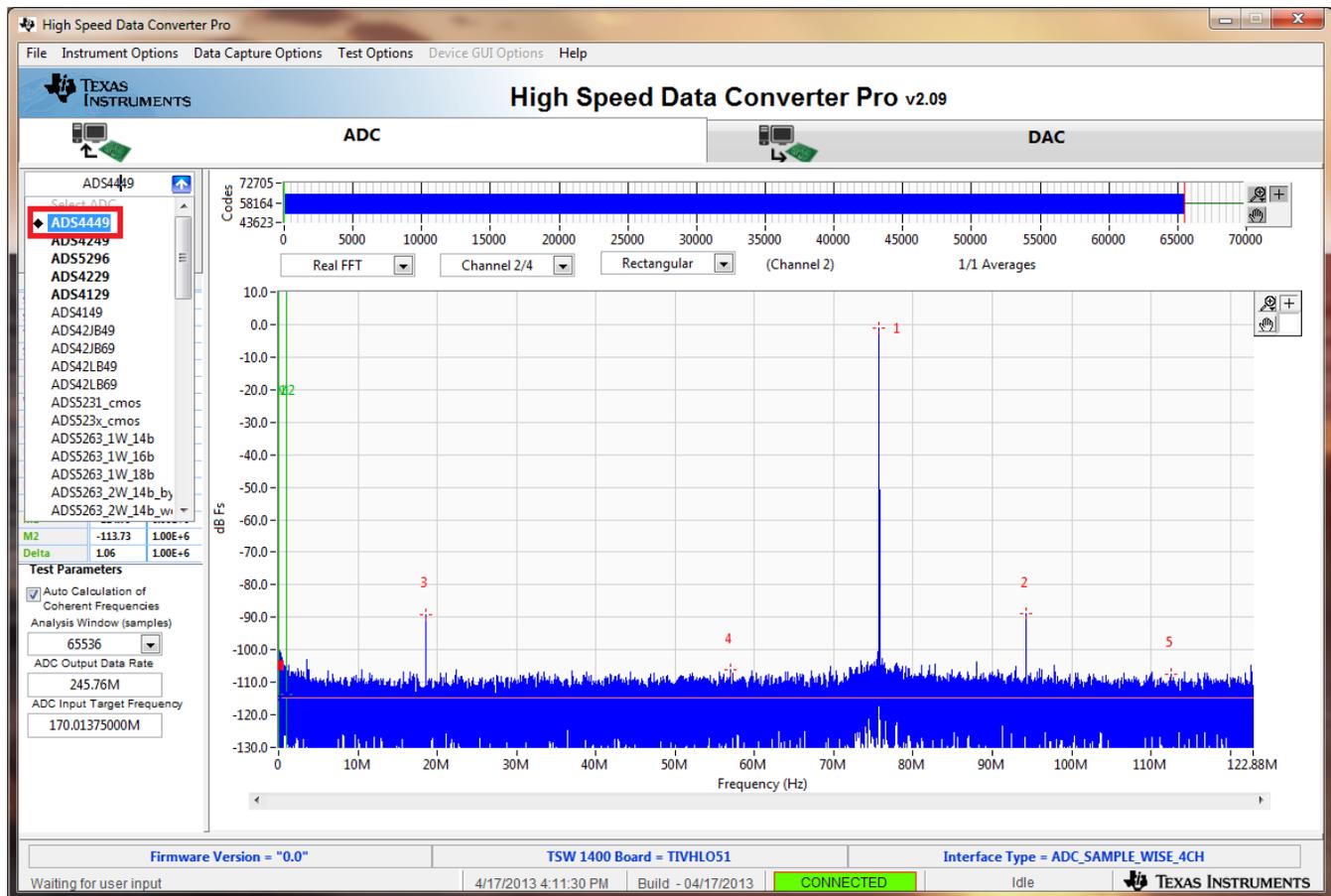


Figure 9. Select ADS4449 in the High Speed Converter Pro GUI Program

2. When prompted *Do you want to update the Firmware for ADC?*, select **Yes**

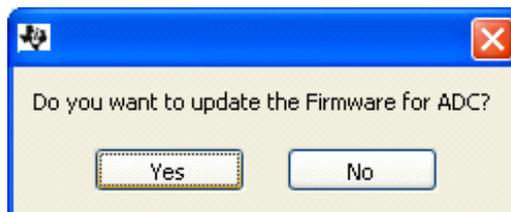


Figure 10. Load ADC Firmware Prompt

3. Select *Single Tone* FFT Test under *Test Selection*
4. Select the number of sample points (and resulting number of FFT bins). The example shown in [Figure 11](#) has 65536 samples.
5. Enter the ADS4449 sampling rate. The example shown in [Figure 11](#) has the sample rate set at 245.76 MSPS.
6. Enter the input frequency desired. If the clock and input frequency signal generators are synchronized, then make sure the checkbox for coherent frequency is checked and set the input frequency signal generator to the input frequency displayed. The example shown in [Figure 11](#) has the input frequency set at 170 MHz.
7. For this example, High Frequency Mode is selected under the ADS4449 GUI special mode tab.
8. Select channel A, B, C, or D depending on which channel is connected to the signal generator.
9. Press the **Capture** button on the High Speed Data Converter Pro GUI.
Observe an FFT result similar to that of [Figure 11](#).

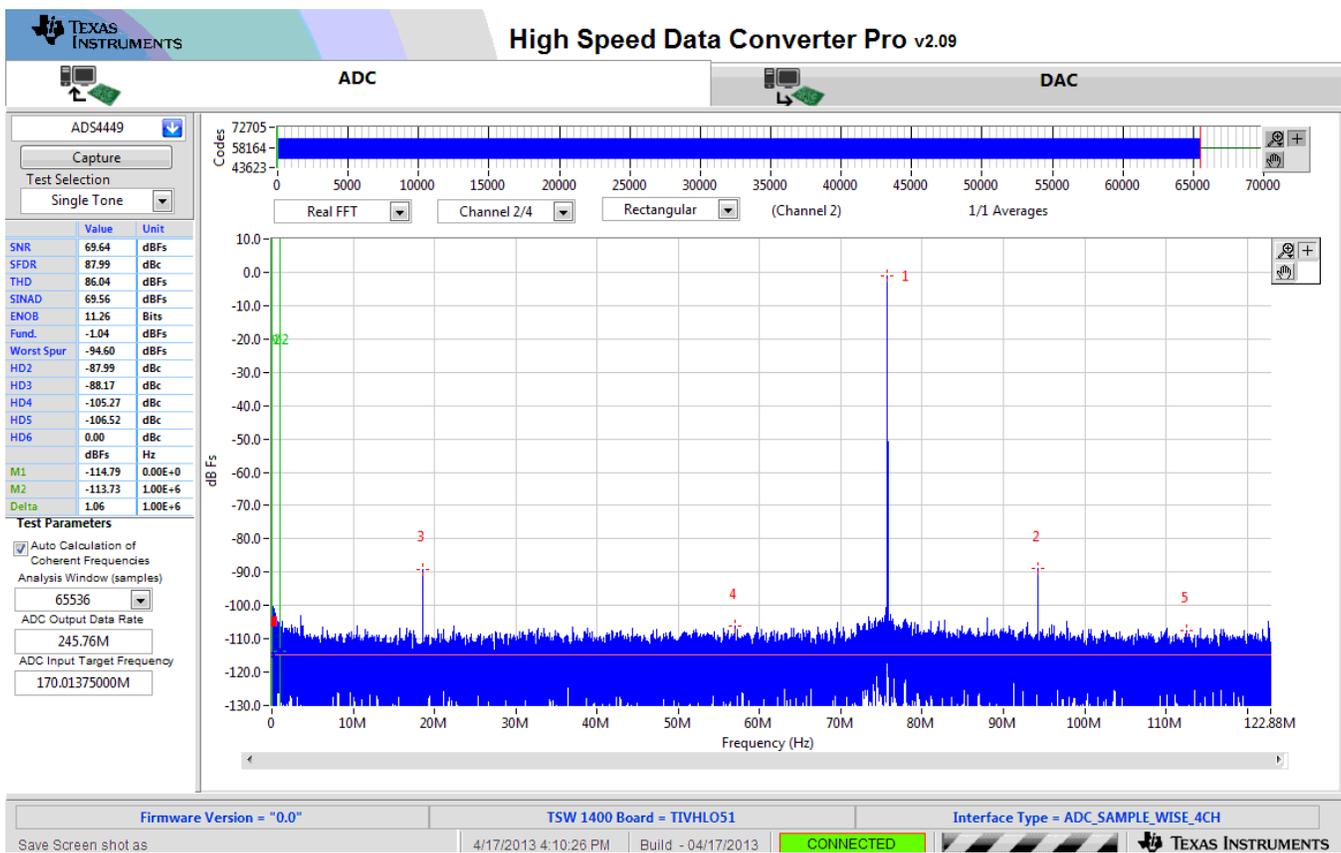


Figure 11. ADS4449 14-bit Operating Mode, Single Tone Test Result: $F_s = 245.76$ MSPS, $F_{in} = 170$ MHz

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2013) to A Revision

Page

- Changed wording regarding power supply following the *Simplified ADS4449 EVM Block Diagram* image. 2
- Changed description on the J2 row of the *ADS4449 EVM Connectors* table. 4

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3. *Regulatory Notices:*
 - 3.1 *United States*
 - 3.1.1 *Notice applicable to EVMs not FCC-Approved:*

This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.
 - 3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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4.3 *Safety-Related Warnings and Restrictions:*

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