SN65HVS880

This design guide helps system designers of digital input modules to design with the SN65HVS880 in the shortest time possible. The document suggests how to design the input stage, select the debounce times, decouple the voltage regulator, control the internal serializer, and accomplish a robust circuit board design withstanding industrial levels of surge, burst, and ESD test voltages.

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1 Introduction

This design guide helps system designers of digital input modules to design with the SN65HVS880 in the shortest time possible. The document suggests how to design the input stage, select the debounce times, decouple the voltage regulator, control the internal serializer, and accomplish a robust circuit board design withstanding industrial levels of surge, burst, and ESD test voltages.

Further information is available in the SN65HVS880 data sheet (SLAS592), the SN65HVS880 EVM manual (SLAU245), and the application report *Special Features of the SN65HVS88x Family of Digital Input Serializers* (SLAA401).

2 Designing the Input Stage

The most common procedure when designing the input stage of a digital input module is:

1. To determine the switching characteristics of the desired sensor switch
2. To identify the input current limit during the switch On-condition
3. To define the input threshold voltage at which an On-condition is indicated

2.1 Setting the Input-Current Limit

Each field input represents a current sink whose current limit is determined by a reference current, I_{REF}. The reference current is created by a voltage reference driving current through a precision resistor, R_{LIM}.

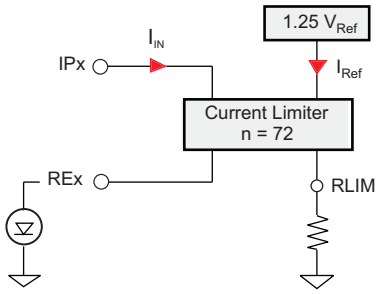

Figure 1. Field Input Stage

Figure 1 shows that the current limiter limits the input current, I_{IN}, at a maximum of:

$$I_{IN} = n \times I_{REF} \quad (1)$$

Because the reference current is determined via:

$$I_{REF} = \frac{V_{REF}}{R_{LIM}} \quad (2)$$

inserting Equation 2 into Equation 1 provides the input current as a function of R_{LIM}:

$$I_{IN} = \frac{n \times V_{REF}}{R_{LIM}} \quad (3)$$

Inserting the actual values for n and V_{REF} simplifies Equation 3 to:

$$I_{IN}\ [mA] = \frac{90\ V}{R_{LIM}\ [k\Omega]} \quad (4)$$

Then, solving for R_{LIM} provides the resistor value for a desired input current limit:

$$R_{LIM}\ [k\Omega] = \frac{90\ V}{I_{IN}\ [mA]} \quad (5)$$

For example, for a desired current limit of 2.5 mA, the value for R_{LIM} becomes 90 V/2.5 mA = 36 kΩ.

2.2 Setting the On/Off Thresholds of the Field Input Voltage

The On-threshold voltage at the device inputs is fixed. The SN65HVS880 data sheet specifies this voltage with $V_{TH(IP+)}$ = 5.2 V typical. The On-threshold voltage of the field inputs, however, depends on the value of the input resistor, R_{IN}. Following the current and voltage conventions in Figure 2, the equation for the field input voltage is:

$$V_{IN} = I_{IN} \times R_{IN} + V_{IP} \quad (6)$$

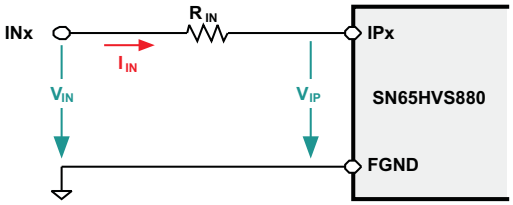

Figure 2. Voltage and Current Conventions

For the specific case of an On-condition, however, the threshold voltages, $V_{TH(IN+)}$ and $V_{TH(IP+)}$ must be inserted into Equation 6:

$$V_{TH(IN+)} = I_{IN} \times R_{IN} + V_{TH(IP+)} \quad (7)$$

Then, solving for R_{IN} provides the resistor value necessary to accomplish the desired On-threshold voltage:

$$R_{IN} = \frac{\left(V_{TH(IN+)} - V_{TH(IP+)}\right)}{I_{IN}} \quad (8)$$

Substituting I_{IN} with Equation 3 gives:

$$R_{IN} = \frac{\left(V_{TH(IN-)} - V_{TH(IP+)}\right) + R_{LIM}}{n \times V_{REF}} \quad (9)$$

And inserting the numerical values for n, V_{REF}, and $V_{TH(IP+)}$ simplifies Equation 9 to:

$$R_{IN} = \frac{\left(V_{TH(IN+)} - 5.2V\right) \times R_{LIM}}{90V} \quad (10)$$

For example, for a desired On-threshold voltage of $V_{TH(IN+)}$ = 8.2V, and a current limiting resistor of R_{LIM} = 36 kΩ, the input resistor value calculates to:

$$R_{IN} = \frac{\left(8.2V - 5.2V\right) \times 36\,k\Omega}{90V} = 1.2\,k\Omega \quad (11)$$

Based on the values of R_{LIM}, R_{IN}, and the specified device Off-threshold voltage of $V_{TH(IP-)}$ = 4.3 V, the Off-threshold at the field input can be easily calculated via:

$$V_{TH(IN-)} = \frac{90V \times R_{IN}}{R_{LIM}} + V_{TH(IP-)} \quad (11)$$

Using the values from the previous example yields an Off-threshold voltage of:

$$V_{TH(IN-)} = \frac{90\ V \times 1.2\ k\Omega}{36\ k\Omega} + 4.3\ V = 7.3\ V \quad (11)$$

The resulting input characteristic is shown in Figure 3.

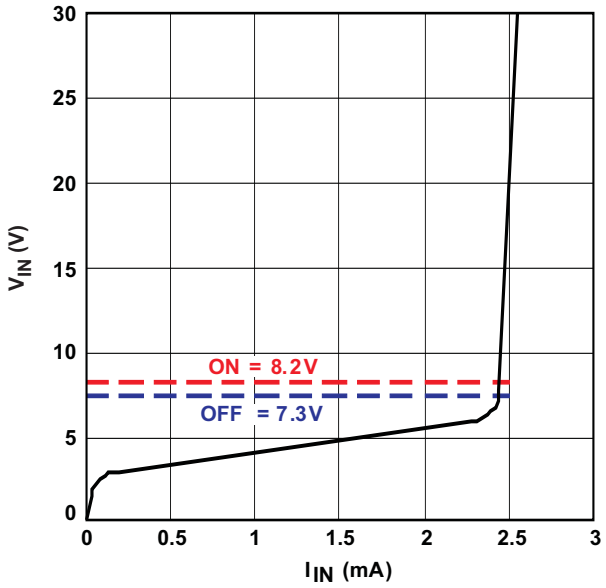

Figure 3. Input Characteristic for R_{LIM} = 36 kΩ and R_{IN} = 1.2 kΩ

3 Achieving Current Limits Beyond 5 mA

The SN65HVS880 can sink input currents of up to 5 mA per channel. For sensor switches requiring higher input currents, it is necessary to connect two inputs in parallel. In this case, both inputs have the same current limit, so that the total current limit is twice that of a single channel. The connection between the two channels can be carried out on the circuit board, or at the terminal block.

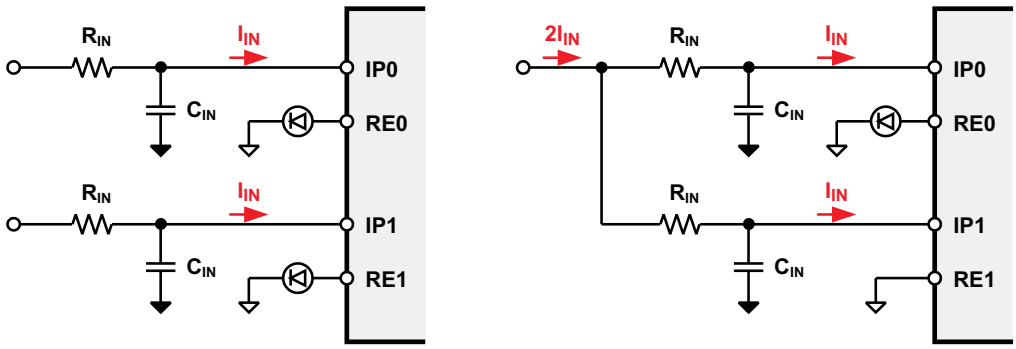

Figure 4. Paralleling Inputs for Higher Currents

While in single-channel operation, each return-pin (REx) requires its own LED; in parallel operation, only one LED needs to be connected to a return pin (REx). The other RE-pin can be directly connected to ground.

Be aware that each combined input now consumes two bits of the serializer. Thus, reading the serializer produces four double-bits rather than eight single bits during single-channel operation.

4 Setting the Debounce Time

The logic signal levels at the control inputs, DB0 and DB1, of the internal Debounce-Select logic determine the debounce times. Both inputs have internal pullup resistors allowing the inputs to be left open when selecting the debounce default value of 3 ms. Selecting other debounce times simply requires connecting one of the inputs to device ground (FGND). Table 1 provides the input states and their corresponding debounce times. For 0 ms, the debounce filters are bypassed internally, and external provisions can be made to filter the inputs with a simple R-C network.

Table 1. Debounce Times

DB0	DB1	FUNCTION
Open	Open	3-ms delay
Open	FGND	1- ms delay
FGND	X	0-ms delay (Filter bypassed)

Note, when operating the HVS880 in a noisy environment, the biasing through the internal 200-kΩ pullup resistors might prove to be too weak. In these circumstances, connecting an unused DB-input to an external 5-V supply, such as the 5VOP-pin, is recommended.

5 Controlling the Serializer

The serial interface of the SN65HVS880 requires a load pulse ($\overline{LD}$) to latch parallel input data into the serializer as well as clock (CLK) and clock-enable ($\overline{CE}$) signals to shift the serializer register content serially out.

INPUTS			FUNCTION
$\overline{LD}$	$\overline{CE}$	CLK	
L	X	X	Parallel Load
H	H	X↑	No Operation
H	L		Serial Shift

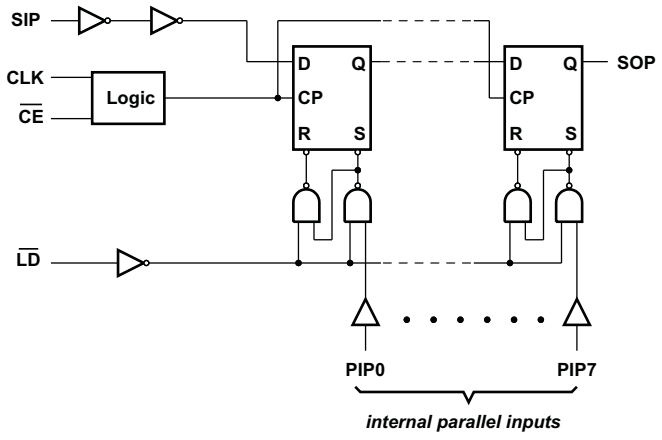

Figure 5. Simplified Serializer Block Diagram and Function Table

- The operation of the low-active load input, $\overline{LD}$, is independent from the other two inputs, $\overline{CE}$ and CLK. Thus, a logic low at $\overline{LD}$ initiates a parallel load while overriding the $\overline{CE}$ and CLK functions. Taking $\overline{LD}$ high latches the parallel input data into the serializer flip-flops.
- When both control inputs, $\overline{LD}$ and $\overline{CE}$, are held high, neither a parallel load nor a serial shift can be carried out.
- In order for CLK to shift the data out, $\overline{CE}$ must be logic low while $\overline{LD}$ must be held high.

5.1 Timing Diagrams

Figure 6 and Figure 7 show the timing diagrams for two possible interface options. For detailed timing specifications, see the SN65HVS880 data sheet.

5.1.1 Operation With $\overline{CE}$ = Low

$\overline{CE}$ in Figure 6 is held continuously low through a direct connection to device ground (FGND). This configuration is possible if the system controller clock is solely used to communicate with one SN65HVS880, or multiple, daisy-chained SN65HVS880 devices.

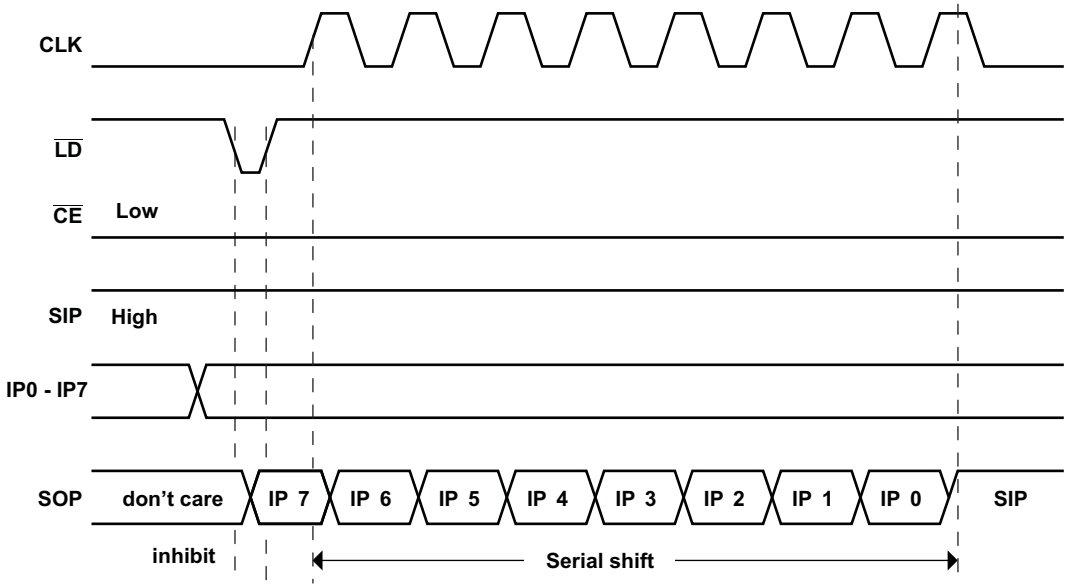

Figure 6. Driving the Serializer Without Clock-Enable

At any time, a load pulse of a 15-ns pulse-width minimum can be applied to $\overline{LD}$. Changes at the field inputs occurring prior to that pulse are latched into the serializer with the positive edge of $\overline{LD}$.

Because the serializer performs a serial shift on the positive edge of CLK, the system controller must wait a minimum of 10 ns after $\overline{LD}$ returns high, before initiating the first clock cycle. After eight clock cycles, the serializer content has been clocked out and the information of its serial input, SIP, appears at the serial output, SOP.

In the case of an 8-channel input module, the controller must stop generating further clock pulses to avoid reading logic high caused by the internal pullup resistor of SIP.

When daisy-chaining multiple SN65HVS880 devices to a 16- or 32-channel module, further clock cycles are required until the content of the serializer chain has been clocked out.

The application of low-cost 8-bit microcontrollers to read a 32-channel input module requires four 8-bit read cycles with a data store into a controller register in between read cycles.

5.1.2 Operation With $\overline{CE}$ Toggling

The timing diagram in Figure 7 shows continuous clock cycles. The method of toggling $\overline{CE}$ allows the windowing of the eight clock cycles for communicating with the SN65HVS880. This interface timing is necessary for applications where the interface clock generated by the controller is required by system functions other than reading digital input channels.

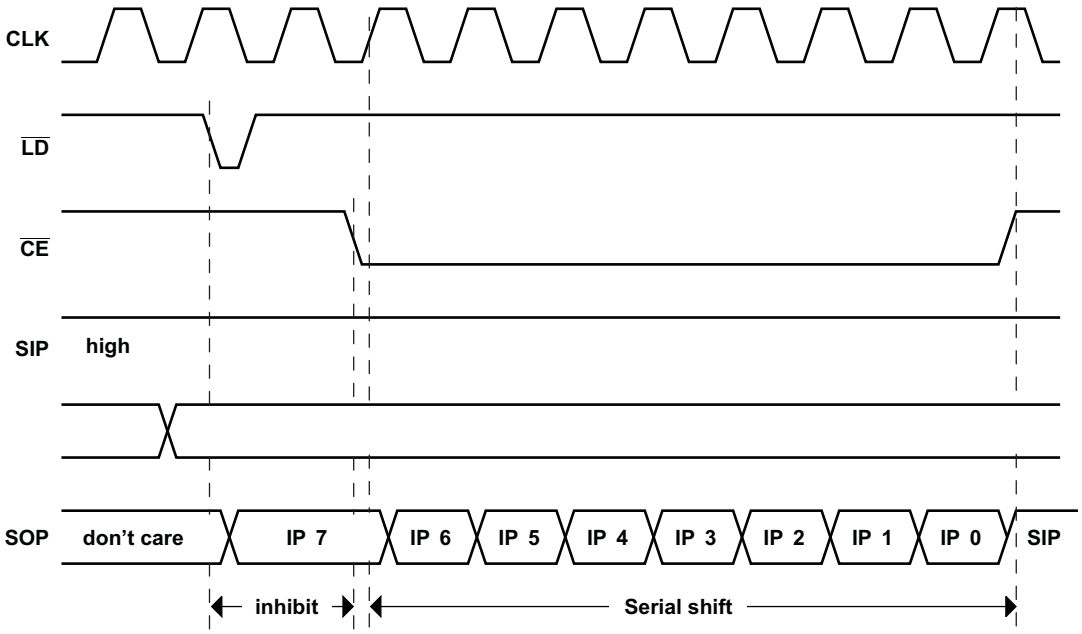

Figure 7. Driving the Serializer With Clock-Enable

The diagram shows that CLK is inhibited from the falling edge of $\overline{LD}$ till the falling edge of $\overline{CE}$. Again a set-up time of 10 ns is required before the controller initiates the first clock cycle. An 8-bit read-out is completed by taking $\overline{CE}$ high after the eighth and at least 10 ns prior to the ninth positive edge of CLK.

Note, to prevent external noise from coupling into the control and data lines, external R-C low-pass filters must be placed as close as possible to the SN65HVS880 device as well as to the digital isolator.

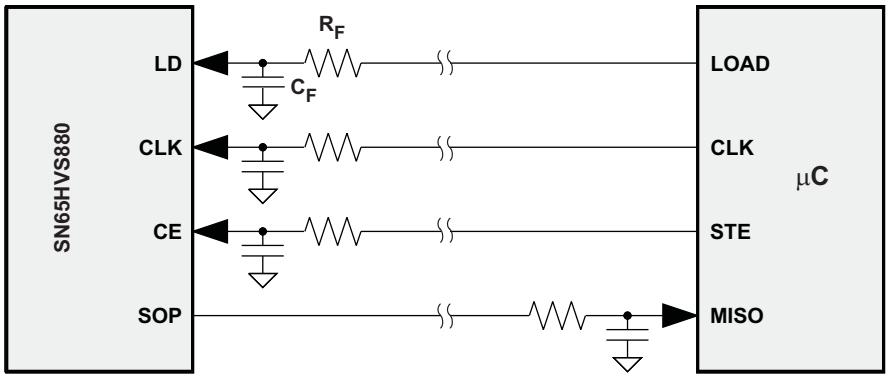

Figure 8. R-C Noise Filters for the Serial Interface

The corner frequency (–3 dB) of the filter must be 10-times the maximum clock frequency, (f_C = 10 f_{CLK}), to minimize phase shift and group delay. For example, for a 1-MHz clock, f_C = 10 MHz. Choose a ceramic capacitor with C_F = 100 pF, and calculate R_F via:

$$R_F = \frac{1}{2\pi \times f_C \times C_F} = \frac{1}{6.28 \times 10^7 \text{Hz} \ 10^{-10} \text{F}} = 159\ \Omega \quad (12)$$

6 Decoupling the 5-V Regulator Output

The on-chip linear voltage regulator provides a 5-V supply to the internal circuitry and external circuitry, such as digital isolators, with an output drive capability of 50 mA and a typical current limit of 115 mA. The regulator accepts input voltages from 30 V down to 10 V.

Because the regulator output is intended to supply external digital isolator circuits, proper output voltage decoupling is required. For best results, connect a 1-µF and a 0.1-µF ceramic capacitor as close as possible to the 5VOP-output. For longer traces between the SN65HVS880 and isolators of the ISO72xx family, use additional 0.1-µF and 10-pF capacitors next to the isolator supply pins.

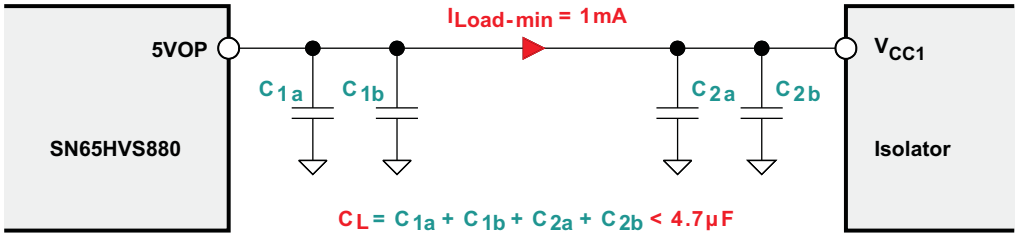

Figure 9. Decoupling the Regulator Output

Note, the total load capacitance must not exceed 4.7 µF. For good stability, the voltage regulator requires a minimum load current, $I_{L\text{-}MIN}$. Ensure that under any operating condition, the ratio of the minimum load current in mA to the total load capacitance in µF is greater than 1:

$$\frac{I_{L\text{-}MIN}}{C_L} > \frac{1\ mA}{1\ \mu F} \tag{13}$$

7 Using the Chip-Okay Indicator

The Chip-Okay (CHOK) output is the Boolean AND-function of the temperature sensor and supply monitor outputs. If either of these outputs turns low due to a fault condition, CHOK turns low. In the absence of a fault condition, CHOK remains high. As such, CHOK can be interpreted either as a device health indicator, or as an alarm indicator.

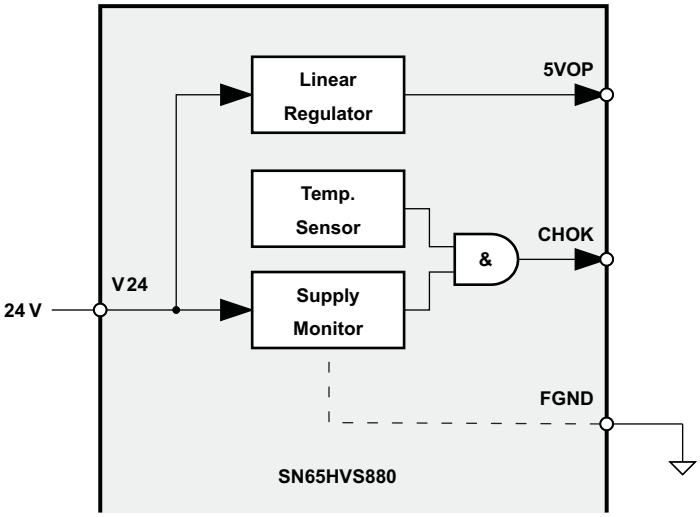

Figure 10. CHOK Provides Alarm for Over-Temperature and Under-Supply

When using CHOK as a health indicator, a green LED diode must be connected between CHOK and device ground (Figure 11a). Without a fault condition, the LED lights up. If a fault occurs the LED turns off.

However, when CHOK is used as an alarm indicator, a red LED must be connected between CHOK and 5VOP (Figure 11b). In this case, the LED turns on only during a fault condition.

A third option is to do without visual indication and connecting CHOK, either directly or via an isolator, to the interrupt input of a microcontroller (Figure 11c).

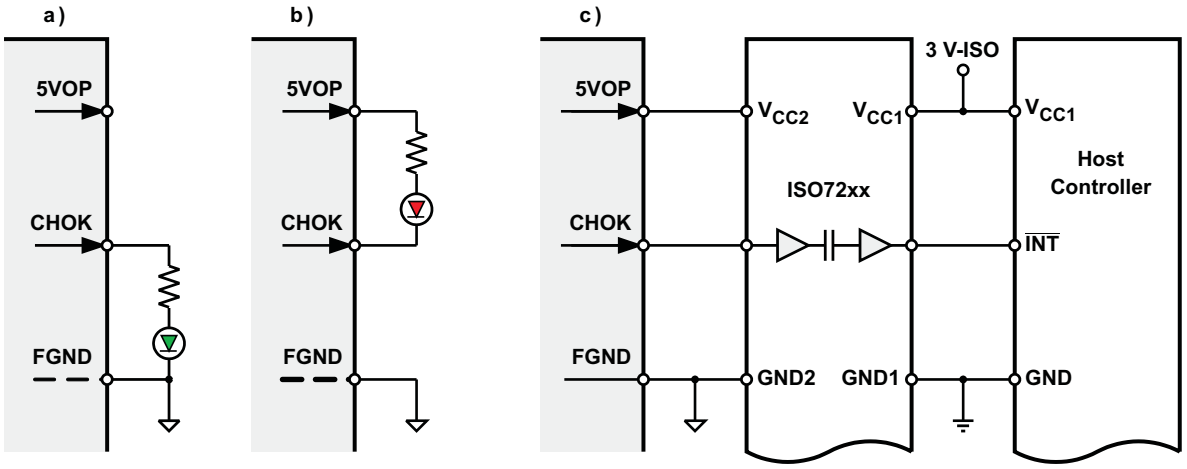

Figure 11. Using CHOK as: a) a Chip-Okay Indicator (Green LED), b) an Alarm Indicator (Red LED), or c) Connecting It to a Controller Interrupt Line (Directly or via an Isolator)

8 EMC Protection Circuitry

Because the SN65HVS880 builds the interface between the field and the controller side in a PLC application, the device is subject to a number of electromagnetic compatibility (EMC) tests, specified in the standard for programmable controllers, IEC61131-2.

Table 2 lists some of the more important tests and their test levels required in industrial automation.

Table 2. EMC Test Requirements

EMC Test	Standard	Test Condition	Test Line	Test Level
Electric Fast Transient/Burst Immunity	IEC61000 – 4.4		Supply and data lines	±4 kV
Electrostatic Discharge Immunity	IEC61000 – 4.2	Contact	Supply and data lines	±6 kV
		Air gap	Supply and data lines	±15 kV
Surge Immunity	IEC61000 – 4.5	1.2 / 50 µs – 8 / 20 µs, 42 Ω – 0.5 µF	Data lines	±0.5 kV
		1.2 / 50 µs – 8 / 20 µs, 2 Ω – 18 µF	Supply lines	±1 kV
Radiated, Radio Frequency, Electromagnetic Field Immunity	IEC61000 – 4.3	80 – 1000 MHz / 1.4 - 2 GHz	Data lines	10 V/m
Reversed Polarity	IEC61131–2	Tested at rated voltage (24 V)	Supply and data lines	> 10 s

In addition to high-voltage levels, noise transients present wide frequency spectra, which can range from 1 MHz up to 3 GHz. Therefore, an effective absorption of transient energy not only requires the attenuation of high voltages, but also the decoupling of high-frequency signals.

While the SN65HVS880 internally possesses robust clamping diode structures, external protection circuitry is recommended to increase transient immunity to the maximum possible level. Figure 12 gives an example of a protection circuit, protecting supply and input lines.

D_{TS}	39 V Transient Voltage Suppressor. SM15T39CA
D_{RP}	Super Rectifier: BYM10-1000, or General Purpose rectifier: 1N4007
D_Z	33 V – 36 V fast Zener Diode, Z2SMB36
R_S	56 Ω, 1/3 W MELF Resistor
R_{IN}	1.2 kΩ, 1/4 W MELF Resistor
C_{IN}	22 nF, 60 V Ceramic Capacitor
C_{HV}	4.7 nF, 2 kV Ceramic Capacitor
C_C	n x 220 nF, 60 V Ceramic Capacitors
C_B	1 µF - 10 µF, 60 V Ceramic Capacitor

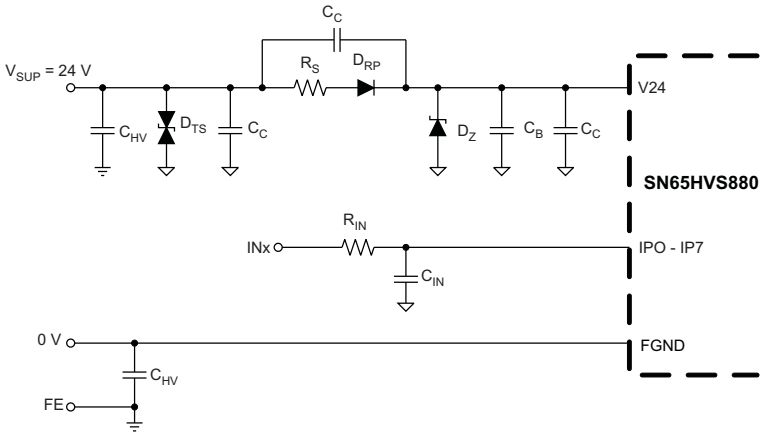

Figure 12. Typical EMC Protection Circuit

The field inputs are protected by a simple R-C low-pass filter with R_{IN} = 1.2 kΩ and C_{IN} = 22 nF. This simple filter structure is possible because of the high resistor value of R_{IN}. In normal operation R_{IN} determines the switch-on threshold of a field input. As a filter resistor, however, it also contributes to a significant reduction in transient current and voltage.

In contrast to the simple input filters, the protection mechanism of the low-impedance supply path is somewhat more complex. A transient suppressor diode, D_{TS}, provides a first level of protection. Due to its high clamp voltage, however, further signal attenuation is recommended through a resistor-Zener diode network, R_S– D_Z, to support the device internal power clamp in the case of high-energy surge transients.

An additional rectifier diode, D_{RP}, protects the device against prolonged, reversed polarity.

Numerous decoupling capacitors, C_C, are connected parallel to the diodes and the chip supply ensuring low impedance return paths for transient currents. Note, that depending on the PCB layout, the designator C_C can represent multiple capacitors per location.

Two further high-voltage capacitors, C_{HV}, are needed to form a return path for asymmetrical testing, where test signals applied to the supply and data lines are referenced to functional earth, FE.

9 PCB Layout

Figure 13 to Figure 15 suggest a test circuit and corresponding board layout for verifying the errorless capture and serial transmission of field input status information from the SN65HVS880 to a microcontroller during EMC testing.

The circuit schematic in Figure 13 shows the low-pass filtered field-inputs, IN0 to IN7, entering the SN65HVS880 via the terminals, IP0 to IP7. The status of the field inputs is indicated by the green LEDs, D1 to D8.

The low-pass filtered control and output signals of the serializer are connected to a digital isolator and made available across the isolation barrier via three surface-mount SMB connectors: $\overline{LD}$, CLK, and SOP.

Thorough event testing requires the application of a predefined bit pattern at the field inputs, which is also stored within the memory of a microcontroller communicating with the board via the SMB connectors. During a test, the controller repeatedly reads the field status stored in the serializer and verifies the information with the bit pattern of its memory. A test level is passed successfully, when the verification yields no loss or manipulation of data.

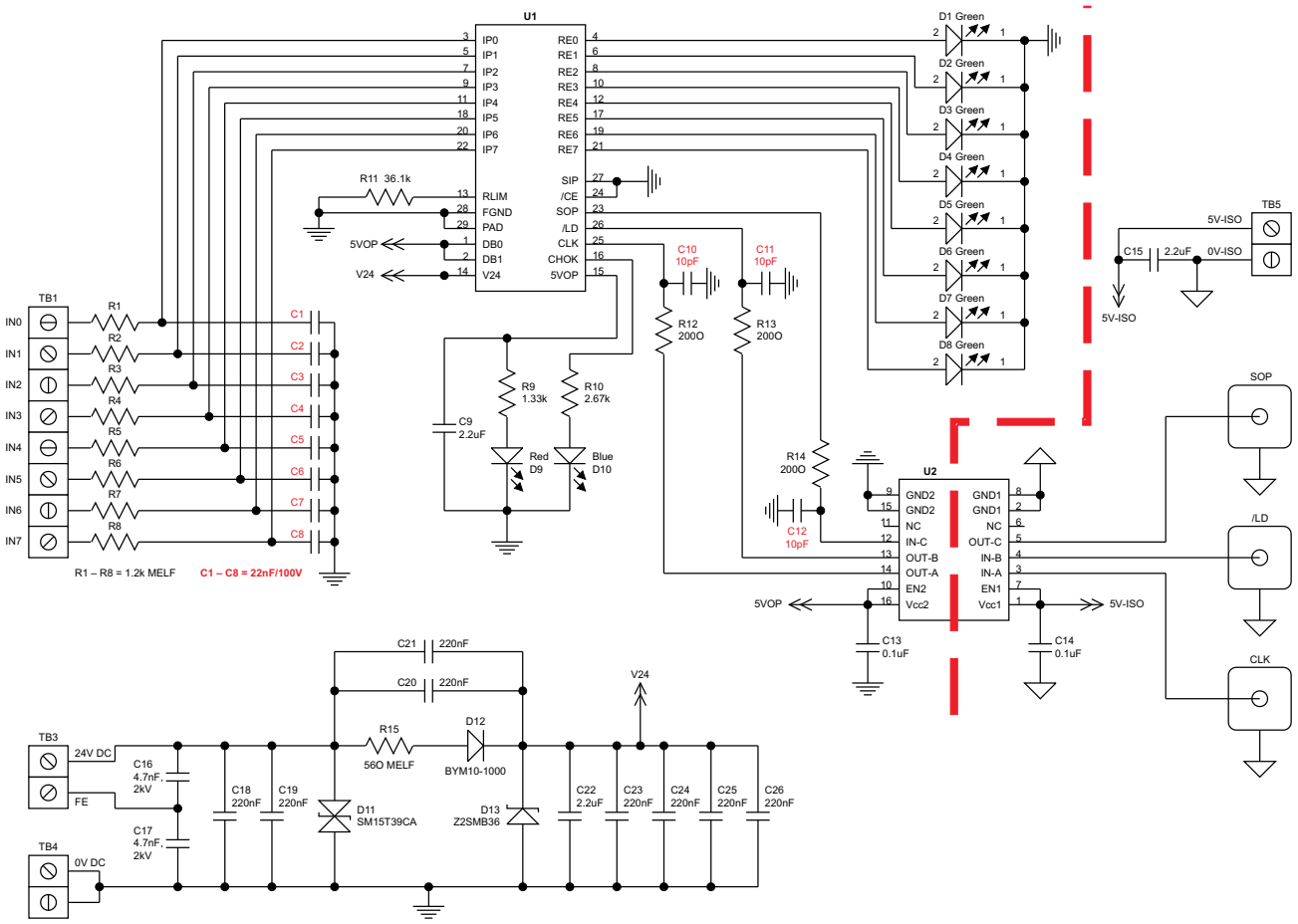

Figure 13. Transient Event Test Circuit

Figure 14 and Figure 15 show the top view and the individual layers of a suggested, four-layer, circuit board with the following layer sequence:

First layer: 0-V mini plane, and RE-lines (RE0 – RE7),

Second layer: full 0-V plane,

Third layer: Input lines (IP0 – IP7),

Fourth layer: V24-plane and 5-V output traces.

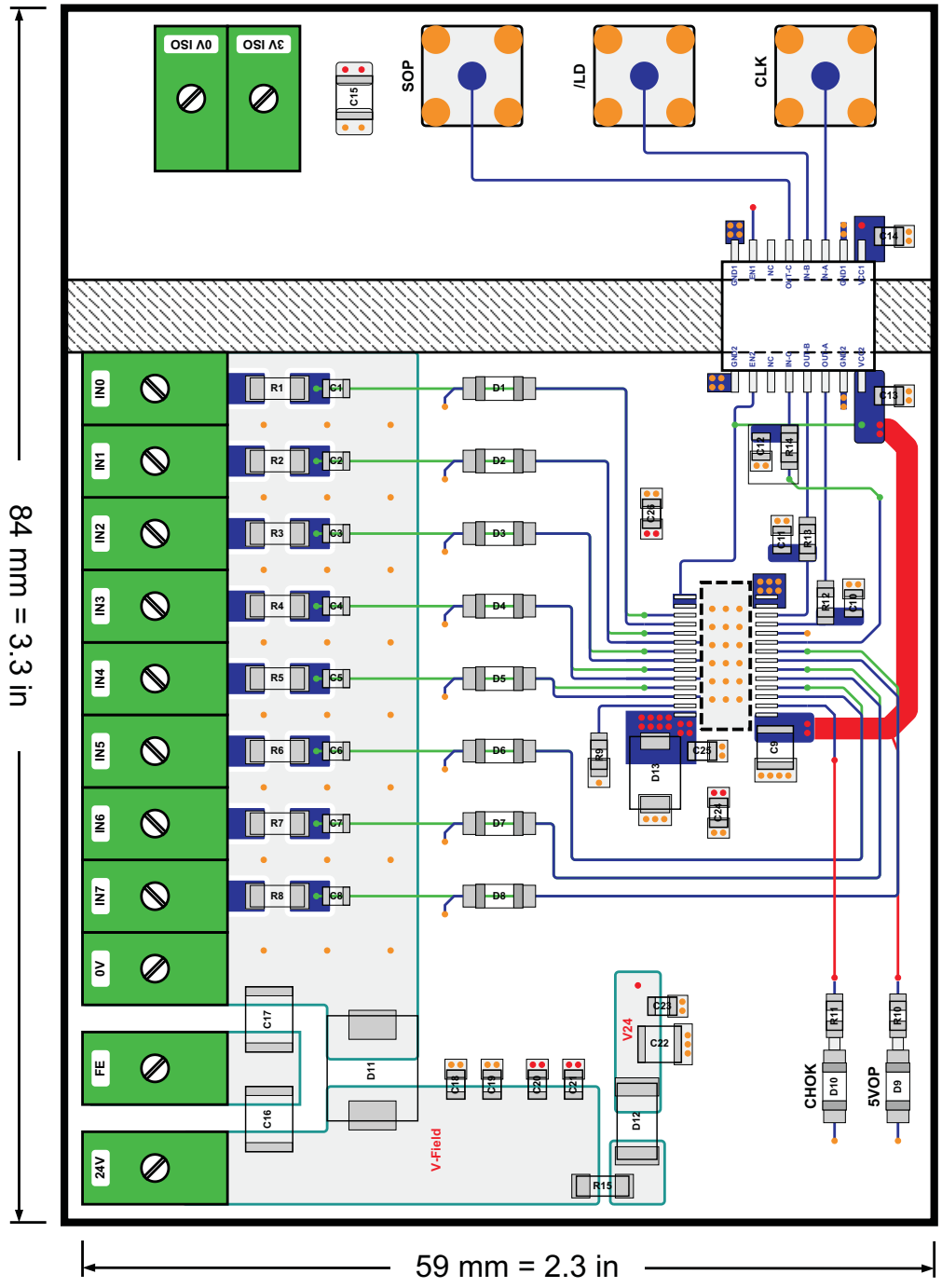

Figure 14. Transparent Top View of EMC Test Board

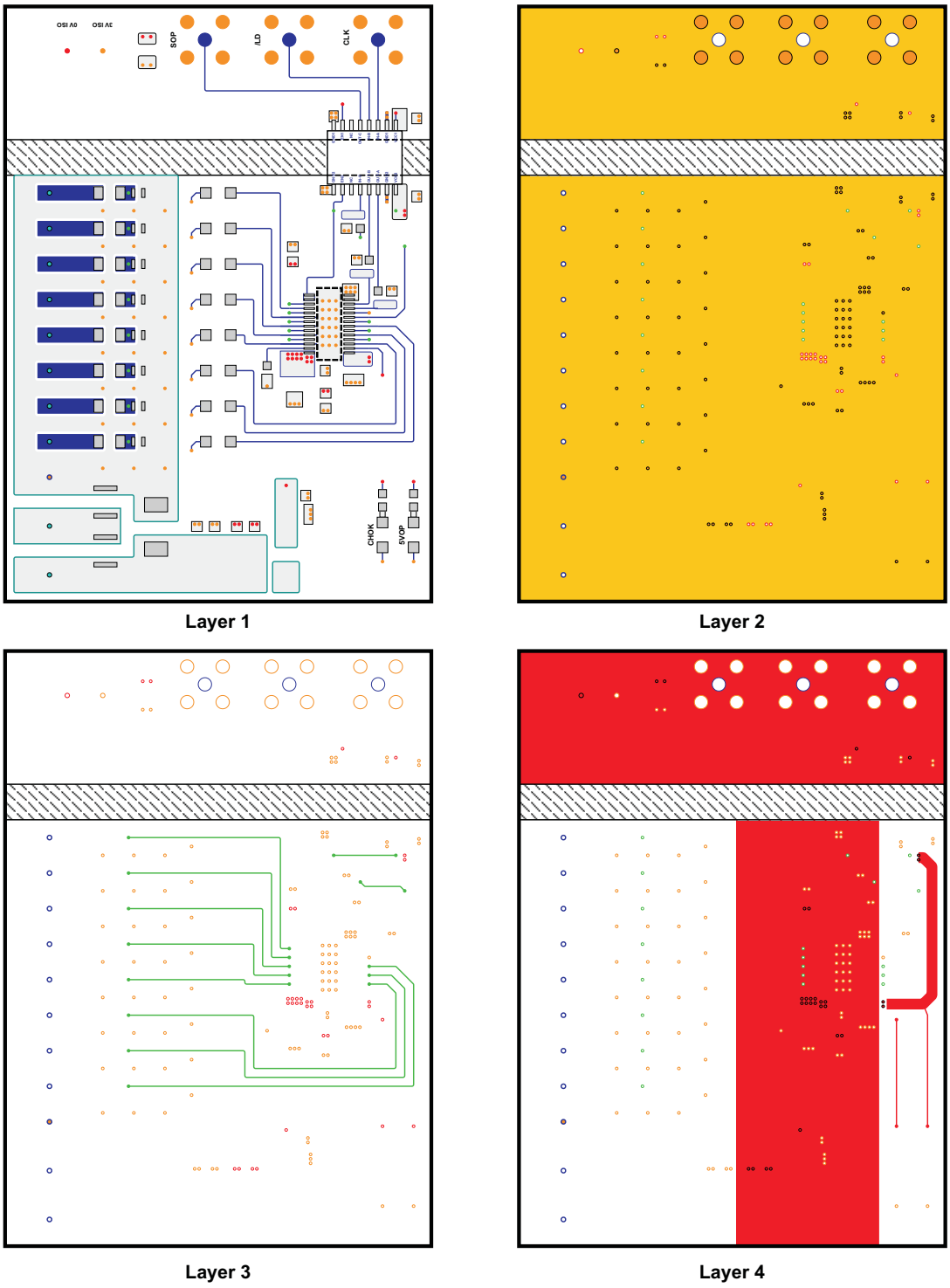

Figure 15. Individual Layers of EMC Test Board

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