User's Guide

ADS7881EVM, ADS7891EVM Evaluation Module

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ABSTRACT

This user's guide describes the characteristics, operation, and use of the ADS78x1 (ADS7881 and ADS7891) 12-bit and 14-bit, parallel, analog-to-digital converter (ADC) evaluation module (EVM). Throughout this document, the terms *evaluation board*, *evaluation module*, and *EVM* are synonymous with the ADS78x1EVM. A complete circuit description, schematic diagram, layout, and bill of materials (BOM) are included in this document.

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Trademarks

1 Introduction

The ADS78x1EVM showcases the 12-bit, 4-MSPS (ADS7881) and 14-bit, 3-MSPS (ADS7891) ADCs. The ADS7881 and ADS7891 devices include a capacitor-based successive-approximation register (SAR) ADC with inherent sample and hold. These devices offer either a 12-bit or 14-bit parallel interface. Both devices offer byte mode operation that enables easy interface with 8-bit processors. They also have a pseudo-differential input stage and a 2.5-V internal reference.

This evaluation module serves as a reference design and a low-cost method to test these converters in the end application. The following sections describe the pin outs of the various analog, power, and digital connectors and power requirements.

Table 1-1 lists documents related to the ADS78x1EVM.

Table 1-1. Related Documentation from Texas Instruments

Data Sheets	Literature Number
ADS7881	SLAS400
ADS7891	SLAS410
ADS8411	SLAS369
THS4031	SLOS224
OPA132	SBOS054
REF1004-2.5	SBVS032
SN74AHC138	SCLS258
SN74AHC245	SCLS230
SN74AHC1G04	SCLS318

1.1 Features

The ADS78x1EVM includes the following features:

- Full-featured evaluation board for the high-speed, SAR-type ADS7881(12-bit, 4-MSPS) or ADS7891(14-bit, 3-MSPS) single-channel, parallel interface ADCs
- Onboard signal conditioning
- Onboard reference
- Input and output digital buffers
- Onboard decoding for stacking multiple EVMs

1.2 Analog Interface

The ADS7881 and ADS7891 ADCs have both a positive and negative analog input pin. The negative input pin, which has a range of –200 mV up to 200 mV is shorted on the board. A signal for the positive input pin can be applied at connector P1, pin 2 (as shown in Table 1-2) or at the center pin of the SMA connector J2.

Table 1-2. Analog Input Connector

Connector.Pin#(1)	Signal	Description
P1.2	+IN	Noninverting input channel
P1.4	Reserved	—
P1.6	Reserved	—
P1.8	Reserved	—
P1.10	Reserved	—
P1.12	Reserved	—
P1.14	Reserved	—
P1.16	Reserved	—
P1.18	Reserved	—
P1.20	REF+	External reference input

(1) All odd-numbered pins of P1 are tied to AGND.

1.2.1 Signal Conditioning

The factory recommends the analog input to any SAR-type converter be buffered and low-pass filtered. The input buffer on the ADS78x1EVM uses the THS4031 (as shown in Figure 1-1) configured as an *inverting* gain of one. However, the amplifier is not stable at a gain of one, and is thus configured for inverting gain of one. The THS4031 was selected for its low noise, high slew rate, and fast settling time. The low-pass filter resistor and capacitor values were selected such that the ADS78x1EVM meets the 1-MHz AC performance specifications listed in the data sheet. The series resistor works in conjunction with the capacitor to filter the input signal, but also isolates the amplifier from the capacitive load. The capacitor to ground at the input of the ADC works in conjunction with the series resistor to filter the input signal, and functions as a charge reservoir. This external filter capacitor works with the amplifier to charge the internal sampling capacitor during sampling mode. Resistors R1 and R12 were selected to reduce offset.

The EVM has a provision to offset the input voltage by adjusting R25, a 10-kΩ potentiometer.

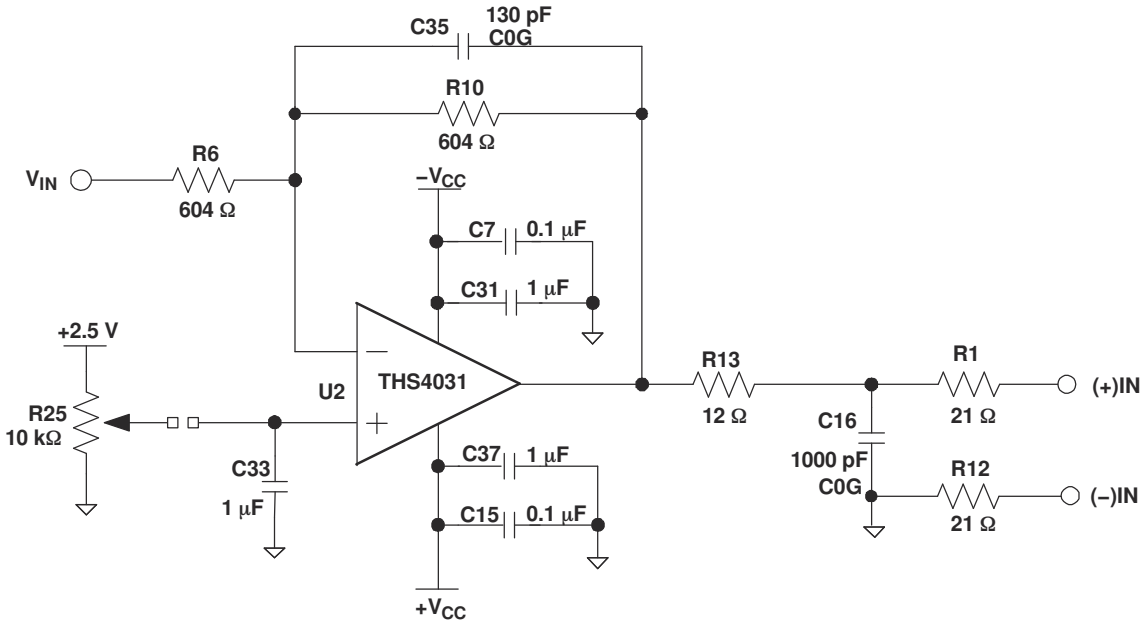

Figure 1-1. ADS7881 Input Buffer Circuit

1.2.2 Reference

The ADS78x1EVM provides an onboard 2.5-V reference circuit. The EVM also supplies a reference voltage via connecter P1 pin 20. This reference voltage can be filtered through amplifier U1. The converter itself has on-chip reference buffer, and therefore does not need to be buffered externally. The reference buffer circuit on the EVM is used to generate the offset voltage for the input amplifier, U2.

The EVM allows selection from three reference sources. Set SJP1, SJP2, and SJP4 to select either an onboard reference voltage (REF1004-2.5), ADC internal reference, or a user-supplied reference voltage via P1 pin 20. Table 1-3 lists jumper settings and Section 5 provides full schematics.

Table 1-3. Solder Short Jumper Setting

Reference Designator	Description	Pads	
		1–2	2–3
SJP1	Apply onboard reference directly to SJP2 pin 3	Installed(1)	—
	Apply buffered reference voltage to SJP2 pin 3	—	Installed
SJP2	Apply internal reference to REFIN pin	Installed(1)	—
	Apply external reference to REFIN pin	—	Installed
SJP4	Apply onboard reference to U1, reference buffer	Installed	—
	Apply user-supplied reference to U1, reference buffer	—	Installed
SJP5	Apply DC offset to input signal	Installed(1)	—
SJP6	Short to pin 4 of amplifier U1 to ground	Installed	—
	Short to pin 4 of amplifier U1 to –VCC	—	Installed(1)
SJP7	Short to pin 4 of amplifier U2 to ground	Installed	—
	Short to pin 4 of amplifier U2 to –VCC	—	Installed(1)

(1) Factory-set condition.

1.3 Digital Interface

The ADS78x1EVM is designed for easy interfacing to multiple platforms. Samtec part numbers SSW-110-22-F-D-VS-K, TSM-110-01-T-DV-P, SSW-116-22-S-D-VS, and TSM-116-01-T-D-V-P provide a convenient dual row header and socket combination at P1, P2, P3, and J3. Consult Samtec at www.samtec.com or 1-800-SAMTEC-9 for a variety of mating connector options.

Connectors P1, P2, and P3 allows the user to plug the EVM into the 5-6k interface card to interface directly with the TMS320C5000 and TMS320C6000 series of DSP. Table 1-4 lists the connector pin out.

Table 1-4. Pin Out for Parallel Control Connector P2

Connector.Pin(1)	Signal	Description
P2.1	$\overline{\text{DC\_CS}}$	Daughter card board select pin
P2.3	—	—
P2.5	—	—
P2.7	A0	Address line from processor
P2.9	A1	Address line from processor
P2.11	A2	Address line from processor
P2.13	—	—
P2.15	—	—
P2.17	—	—
P2.19	BUSY	Busy signal from converter. W4 must be shorted.

(1) All even-numbered pins of P2 are tied to DGND.

Read ($\overline{\text{RD}}$), conversion start ($\overline{\text{CONVST}}$) and reset ($\overline{\text{RESET}}$) signals to the converter can be assigned to two different addresses in memory via jumper settings. The jumper settings allow up to two ADS78x1EVMs to be stacked into processor memory. See Table 1-5 for jumper settings. The evaluation module does not allow the

chip-select ($\overline{CS}$) line of the converter to be assigned to different memory locations. Instead, ground or wire the $\overline{CS}$ line to an appropriate signal of the user processor.

Table 1-5. Jumper Settings

Reference Designator	Description	Pins	
		1–2	2–3
W1	Short U8 pin 14 to power-down or reset signal	Installed(1)	—
	Short U8 pin 13 to power-down or reset signal	—	Installed
W2	Short U8 pin 12 to $\overline{CONVST}$ signal	Installed(1)	—
	Short U8 pin 11 to $\overline{CONVST}$ signal	—	Installed
W3	Short U8 pin 10 to $\overline{RD}$ signal	Installed(1)	—
	Short U8 pin 8 to $\overline{RD}$ signal	—	Installed
W4	Short inverted BUSY to $\overline{INTC}$	Installed(1)	—
	Short BUSY to $\overline{INTC}$	—	Installed
W5	Short +5VD to +BVDD	Installed(1)	—
	Short +3.3VD to +BVDD	—	Installed

(1) Factory-set condition.

The data bus is available at connector P3. Table 1-6 lists the pin out information. This EVM supports two devices but the connector signals names are based on the ADS7981, which is the higher-resolution device. Depending on which device is being evaluated, care must be taken when connecting the EVM to a host processor.

Table 1-6. Data Bus Connector P3

Connector.Pin(1)	Signal Name	Description	
		ADS7881	ADS7891
P3.1	B_DB0	Not connected	Buffered data bit 0 (LSB)
P3.3	B_DB1	Not connected	Buffered data bit 1
P3.5	B_DB2	Buffered data bit 0 (LSB)	Buffered data bit 2
P3.7	B_DB3	Buffered data Bit 1	Buffered data bit 3
P3.9	B_DB4	Buffered data bit 2	Buffered data bit 4
P3.11	B_DB5	Buffered data bit 3	Buffered data bit 5
P3.13	B_DB6	Buffered data bit 4	Buffered data bit 6
P3.15	B_DB7	Buffered data bit 5	Buffered data bit 7
P3.17	B_DB8	Buffered data bit 6	Buffered data bit 8
P3.19	B_DB9	Buffered data bit 7	Buffered data bit 9
P3.21	B_DB10	Buffered data bit 8	Buffered data bit 10
P3.23	B_DB11	Buffered data bit 9	Buffered data bit 11
P3.25	B_DB12	Buffered data bit 10	Buffered data bit 12
P3.27	B_DB13	Buffered data bit 11 (MSB)	Buffered data bit 13 (MSB)
P3.29	Not connected	Not connected	Not connected
P3.31	Not connected	Not connected	Not connected

(1) All even-numbered pins of P3 are tied to DGND.

As described in Table 1-7, this evaluation module provides direct access all the analog-to-digital converter control signals via connector J3.

Table 1-7. Pin Out for Converter Control Connector J3

Connector.Pin(1)	Signal	Description
J3.1	$\overline{CS}$	Chip-select pin. Active low.
J3.3	$\overline{RD}$	Read pin. Active low.
J3.5	$\overline{CONVST}$	Convert start pin. Active low.
J3.7	BYTE	BYTE mode pin. Used for 8-bit buses.
J3.9	$\overline{PWD/RST}$	Active low input, acts as device power down or device reset signal.
J3.11	$\overline{A\_PDWN}$	Nap mode enable, active low.
J3.13	BUSY	Converter status output. High when a conversion is in progress.

(1) All even-numbered pins of J3 are tied to DGND.

1.4 Power Supplies

The EVM accepts four power supplies.

- A dual ±Vs DC supply for the dual-supply op amps. A ±12-V DC supply is recommended.
- A single +5.0-V DC supply for the analog section of the board (ADC + reference).
- A single +5.0-V or +3.3-V DC supply for the digital section of the board (ADC + address decoder + buffers).

There are two ways to provide these voltages.

1. Wire in voltages, as listed in Table 1-8, at test points on the EVM.

Table 1-8. Power-Supply Test Points

Test Point	Signal	Description
TP11	+BVDD	Apply a +3.3-V DC or +5.0-V DC voltage. See the respective ADC data sheet for the full range.
TP10	+AVCC	Apply a +5.0-V DC voltage.
TP12	+VA	Apply a +12.0-V DC voltage. Positive supply for the amplifier.
TP14	–VA	Apply a –12.0-V DC voltage. Negative supply for the amplifier.

1. Use the power connector J1 and derive the voltages elsewhere. Table 1-9 lists the pin out connections for J1. Set jumper W5 to short between pins 1-2 or pins 2-3 to short +3.3VD or +5VD, respectively, to be the buffer digital supply (+BVDD).

Table 1-9. Power Connector, J1, Pin Out

Signal	Power Connector - J1		Signal
+VA (+12VA)	1	2	–VA (–12VA)
+AVCC (+5VA)	3	4	N/C
N/C	5	6	AGND
N/C	7	8	N/C
+3.3VD	9	10	+5VD

2 Using the EVM

The ADS78x1EVM serves as a reference design, prototype board, and test platform for the software engineer to develop code.

As a reference design, the ADS78x1EVM contains the essential circuitry to showcase the ADC. This essential circuitry includes the input amplifier, reference circuit, and buffers. The EVM analog input circuit is optimized for a 1-MHz sine wave, therefore users may need to adjust the resistor and capacitor values of the ADC input RC circuit. In AC-type applications where signal distortion is a concern, use polypropylene capacitors in the signal path. In applications where the input is multiplexed, either adjust or remove the ADC input resistor and capacitor, as needed.

As a prototype board, the buffer circuit consists of a footprint in a standard 8-pin SOIC and resistor pads for inverting and noninverting configurations. The ADS78x1EVM can be used to evaluate both dual- and single-supply amplifiers. The EVM comes installed with a dual-supply amplifier that allows the user to take advantage of the full input voltage range of the converter. For applications that require signal supply operation and smaller input voltage ranges, the THS4031 can be replaced with a single-supply amplifier, such as the OPA300. Short pad jumper SJP7 between pads 1 and 2, because SJP7 shorts the minus supply pin of the amplifier to ground. The positive supply voltage can be applied via test point TP12 or connector J1 pin 1.

As a software test platform, connectors P1, P2, and P3 plug into the parallel interface connectors of the 5-6K interface card. The 5-6K interface card sits on the C5000 and C6000 digital signal processor starter kit (DSK). The ADS78x1EVM is then mapped into the processor memory space. This card also provides an area for signal conditioning. This area can be used to install application circuits for digitization by the ADS7881 or ADS7891 ADC. See the *5–6K Interface Board* user's guide for more information.

For the software engineer, the ADS78x1EVM provides a simple platform for interfacing to the converter. The EVM provides standard 0.1" headers and sockets to wire into prototype boards. The user must only provide three address lines (A2, A1, and A0) and one address valid line ($\overline{DC\_CS}$) to connector P2, as shown in Figure 2-1. To choose which address combinations generate $\overline{RD}$, $\overline{CONVST}$, and $\overline{RESET}$ set jumpers as shown in Table 1-5. Recall that the chip select ($\overline{CS}$) signal is not memory mapped or tied to P2, and therefore must be controlled via a general-purpose pin or shorted to ground at the J3 pin 1. If address decoding is not required, the EVM provides direct access to converter data bus via P3 and control via J3.

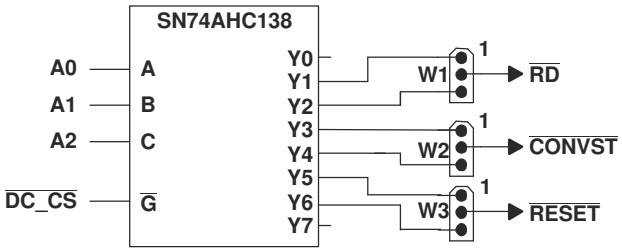

Figure 2-1. Decoding Control Signals Using the Address Bus

3 ADS78x1EVM Bill of Materials

Table 3-1 contains a complete bill of materials (BOM) for the ADS78x1EVM. The schematic diagrams are also provided for reference in Section 5.

Table 3-1. Bill of Materials

Item No.	Qty.	Value	Reference Designators	Footprint	Manufacturer	Manufacturer's Part Number	Description
1	2	21	R1 R12	805	Panasonic-ECG or Alternate	ERJ-6ENF21R	RES, 21.0 Ω, 1/10W, 1% 0805 SMD
2	3	NI	R2 R5 R11	805	Not installed	Not installed	
3	1	NI	R3	603	Not installed	Not installed	1/10W, 0805 Chip Resistor
4	3	100	R4 R14 R15	805	Panasonic-ECG or Alternate	ERJ-6ENF1000V	RES, 100 Ω, 1/10W, 1%, 0805 SMD
5	2	604	R6 R10	805	Panasonic-ECG or Alternate	ERJ-6ENF6040V	RES, 604 Ω, 1/10W, 1%, 0805 SMD
6	6	10k	R7 R16 R17 R18 R19 R20	603	Panasonic-ECG or Alternate	ERJ-3EKF1002V	RES, 10.0 kΩ, 1/16W, 1%, 0603 SMD
7	1	49.9	R8	1206	Panasonic-ECG or Alternate	ERJ-8ENF49R9V	RES, 49.9 Ω, 1/8W, 1%, 1206 SMD
8	1	49.9k	R9	805	Panasonic-ECG or Alternate	ERJ-6ENF4992V	RES, 49.9 kΩ, 1/10W, 1%, 0805 SMD
9	1	12	R13	805	Panasonic-ECG or Alternate	ERJ-6GEYJ120V	RES, 12 Ω, 1/8W, 5%, 0805 SMD
	1	10	R13(1)	805	Yageo America or Alternate	9C08052A10R0FKHFT	RES, 10 Ω, 1/8W, 1%, 0805 SMD
10	1	75	R21	805	Panasonic-ECG or Alternate	ERJ-6ENF75R0V	RES, 75.0 Ω, 1/10W, 1%, 0805 SMD
11	1	0	R24	603	Panasonic-ECG or Alternate	ERJ-3GEY0R00V	RES, 0 Ω, 1/16W, 5%, 0603 SMD
12	1	10k	R22	805	Panasonic-ECG or Alternate	ERJ-6ENF1002V	RES, 10.0 kΩ, 1/10W, 1%, 0805 SMD
13	1	10k	R25	BOURNS_ 32×4W	Bourns	3214W-1-103E	TRIMPOT, 10 kΩ, 4MM TOP ADJ SMD
14	4	10 µF	C1 C6 C12 C19	1206	TDK Corporation or Alternate	C3216X5R1C106KT	CAP, CER, 10 µF, 16V, X5R, 20%, 1206
15	2	1 µF	C2 C28	603	TDK Corporation or Alternate	C1608X5R1C105K	CAP, CER, 1.0 µF, 16V, X5R, 10%, 0603
16	5	1000 pF	C3 C5 C11 C16 C23	603	TDK Corporation or Alternate	C1608C0G1H102J	CAP, CER, 1000 pF, 50V, C0G, 5%, 0603
17	13	0.01 µF	C4 C10 C13 C20 C21C26 C41 C44 C46 C48 C50 C53 C56	603	TDK Corporation or Alternate	C1608X7R1H103KT	CAP, CER, 10000 pF, 50V, X7R, 10%, 0603
18	4	0.1 µF	C7 C15 C32 C36	805	TDK Corporation or Alternate	C1608X7R1E104K	CAP, CER, 0.10 µF, 25V X7R, 10%, 0603
19	8	2.2 µF	C8 C40 C42 C47 C51 C52 C54 C55	603	TDK Corporation or Alternate	C1608X5R1A225MT	CAP, CER, 2.2 µF, 6.3V, X5R, 20%, 0603
20	9	0.1 µF	C9 C18 C22 C25 C38 C43 C57 C58 C62	603	TDK Corporation or Alternate	C1608X7R1E104K	CAP, CER, 0.10 µF, 25V, X7R 10%, 0603
21	4	10 µF	C14 C24 C27 C29	6032	Panasonic-ECG or Alternate	ECS-T1EC106R	CAP, 10 µF, 25V, TANTALUM, TE, SMD
22	1	22 µF	C17	1206	Panasonic-ECG or Alternate	C3216XR0J226M	CAP, CER, 22 µF, 6.3V X5R, 20%, 1206
	1	1500 pF	C16(1)	603	TDK Corporation or Alternate	C1608C0G1H152J	CAP, CER, 1500 pF, 50V, C0G, 5%, 0603
23	4	NI	C30 C39 C61 C63	805	NOT INSTALLED	NOT INSTALLED	Multilayer Ceramic - 0805 Size
24	5	1 µF	C31 C33 C37 C59 C60	805	TDK Corporation or Alternate	C2012X7R1E105K	CAP, CER, 1.0 µF, 25V, X7R, 0805, T/R
25	1	130 pF	C35	805	TDK Corporation or Alternate	C2012C0G1H131	CAP, CER, 130 pF, 50V 5%, C0G, 0805
26	1	10 µF	C49	3528	Kemet or Alternate	T491B106K016AS	CAP, TANTALUM, 10 µF, 16V 10%, SMD
27	2	1K	RP1 RP3	CTS_742	CTS Corporation	742C163102JTR	RES ARRAY, 1 kΩ, 16TERM 8RES SMD
28	1	100	RP2	CTS_742	CTS Corporation	742C163101JTR	RES ARRAY 100 Ω 16TRM, 8RES SMD
29	4		L1 L2 L3 L4	805	TDK Corporation	MMZ2012R601A	Ferrite chip, 600 Ω, 500 mA
30	1		U1	8-SOP(D)	Texas Instruments	OPA132UA	DiFet amplifier
31	1		U2	8-SOP(D)	Texas Instruments	THS4031IDR	100 MHz, low-noise, high-speed amplifier
32	1	NI	U3	3-SOT-23	Not installed	Not installed	REF3040, 50 ppm/–C, 50-A in SOT23-3 CMOS voltage reference

Table 3-1. Bill of Materials (continued)

Item No.	Qty.	Value	Reference Designators	Footprint	Manufacturer	Manufacturer's Part Number	Description
33	1	ADS7881	U4	SOCKET_48 QFPP	Texas Instruments	ADS7881IPFBT	ADS7881, 12-bit, 4 MSPS
		ADS7891	U4(1)			ADS7891IPFBT	ADS7891, 14-bit, 3 MSPS
34	3	SN74AHC245	U5 U6 U7	20-TSSOP(PW)	Texas Instruments	SN74AHC245PWR	Octal bus transceiver, 3-state
35	1	SN74AHC138	U8	16-TSSOP (PW)	Texas Instruments	SN74AHC138PWR	3-line to 8-line decoder/ demultiplexer
36	1	REF1004-2.5	U9	8-SOP(D)	Texas Instruments	REF1004-2.5	Micropower voltage reference
37	1	SN74AHC1G04	U12	5-SOT(DBV)	Texas Instruments	SN74AHC1G04DBVR	Single inverter gate
38	2	10×2×0.1	P1 P2	10×2×0.1_SMT_PLUG_&_SOCKET	Samtec	SSW-110-22-S-D-VS	0.025" SMT socket - bottom side of PWB
39	2				Samtec	TSM-107-01-T-D-V-P	0.025" SMT plug - top side of PWB
40	1	Data Bus	P3	10×2×0.1_SMT_PLUG_&_SOCKET	Samtec	SSW-116-22-S-D-VS	0.025" SMT socket - bottom side of PWB
41	1				Samtec	TSM-116-01-T-D-V-P	0.025" SMT plug - top side of PWB
42	1	Power Supply	J1	5×2×0.1_SMT_SOCKET	Samtec	SSW-105-22-S-D-VS	0.025" SMT socket - bottom side of PWB
43	1				Samtec	TSM-105-01-T-D-V-P	0.025" SMT plug - top side of PWB
44	1	SMA_PCB_MT	J2	SMA_JACK	Johnson Components Inc.	142-0701-301	Right angle SMA connector
45	1	7×2×0.1	J3	7×2×0.1_SMT_PLUG_&_SOCKET	Samtec	SSW-107-22-S-D-VS	0.025" SMT socket - bottom side of PWB
46	1				Samtec	TSM-107-01-T-D-V-P	0.025" SMT plug - top side of PWB
47	1	SW-PB	S1	EVQ-PJ	Panasonic	EVQ-PJU04K	switch
48	5		W1 W2 W3 W4 W5	3POS_JUMPER	Samtec	TSW-103-07-L-S	3 Position jumper _ 0.1" spacing
49	1	SJP2	SJP5	SJP2	Not installed	Not installed	Pad 2 position jumper
50	5	SJP3	SJP1 SJP2 SJP4 SJP6 SJP7	SJP3	Not installed	Not installed	Pad 3 position jumper
51	1	TO_0.025	TP1	test_point2	Keystone Electronics	5002K-ND	Test point, PC, mini 0.040" D, white
52	10	TO_0.025	TP3 TP4 TP6 TP8 TP9 TP10 TP11 TP12 TP14 TP15	test_point2	Keystone Electronics	5000K-ND	Test point, PC, mini 0.040" D, red
53	4	TO_0.025	TP5 TP7 TP2 TP13	test_point2	Keystone Electronics	5001K-ND	Test point, PC, mini 0.040" D, black

(1) Used for the ADS7891EVM only.

4 ADS78x1EVM Layout

Figure 4-1 to Figure 4-4 illustrate the silkscreens for the ADS78x1EVM.

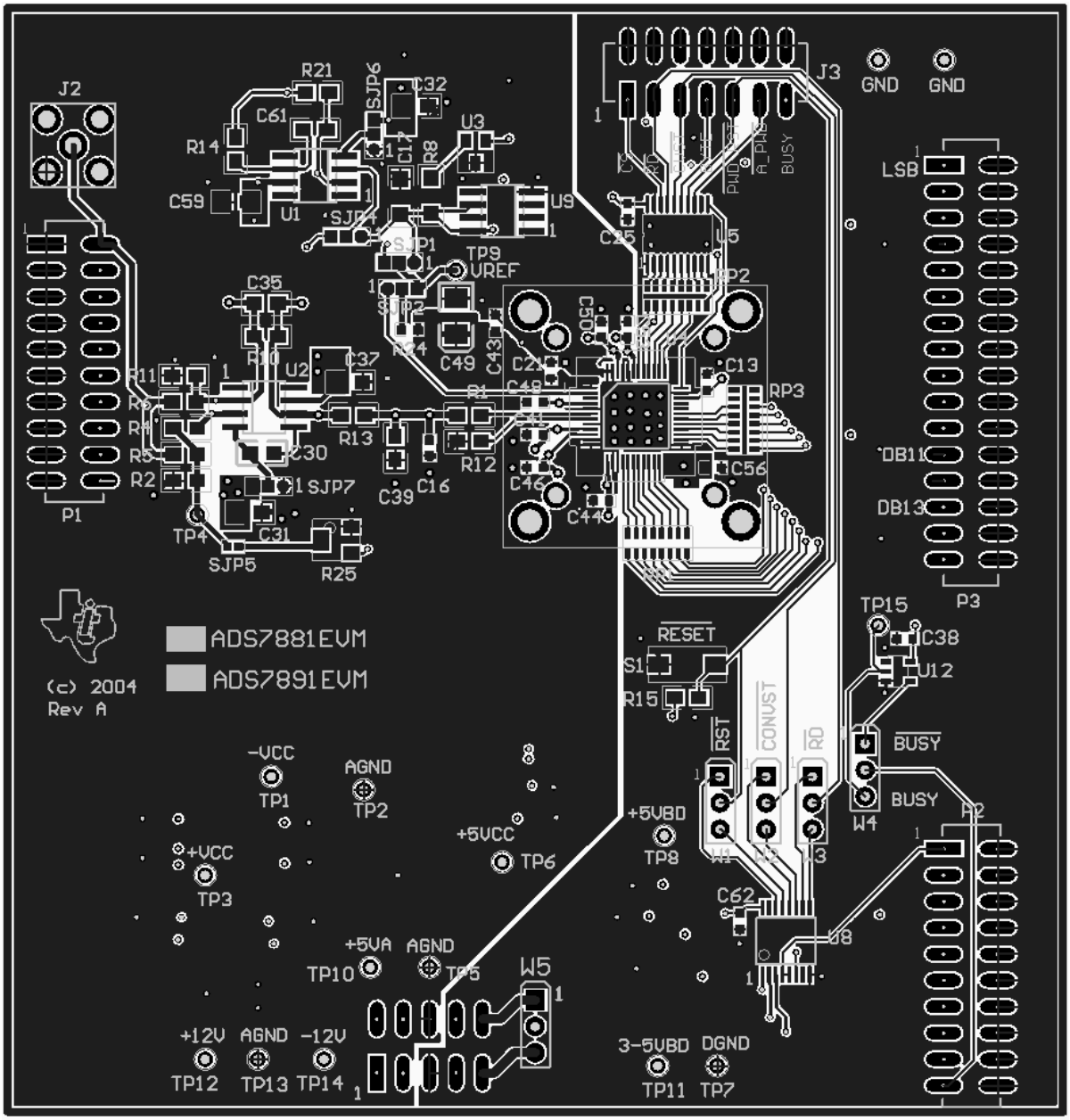

Figure 4-1. Top Layer – Layer 1

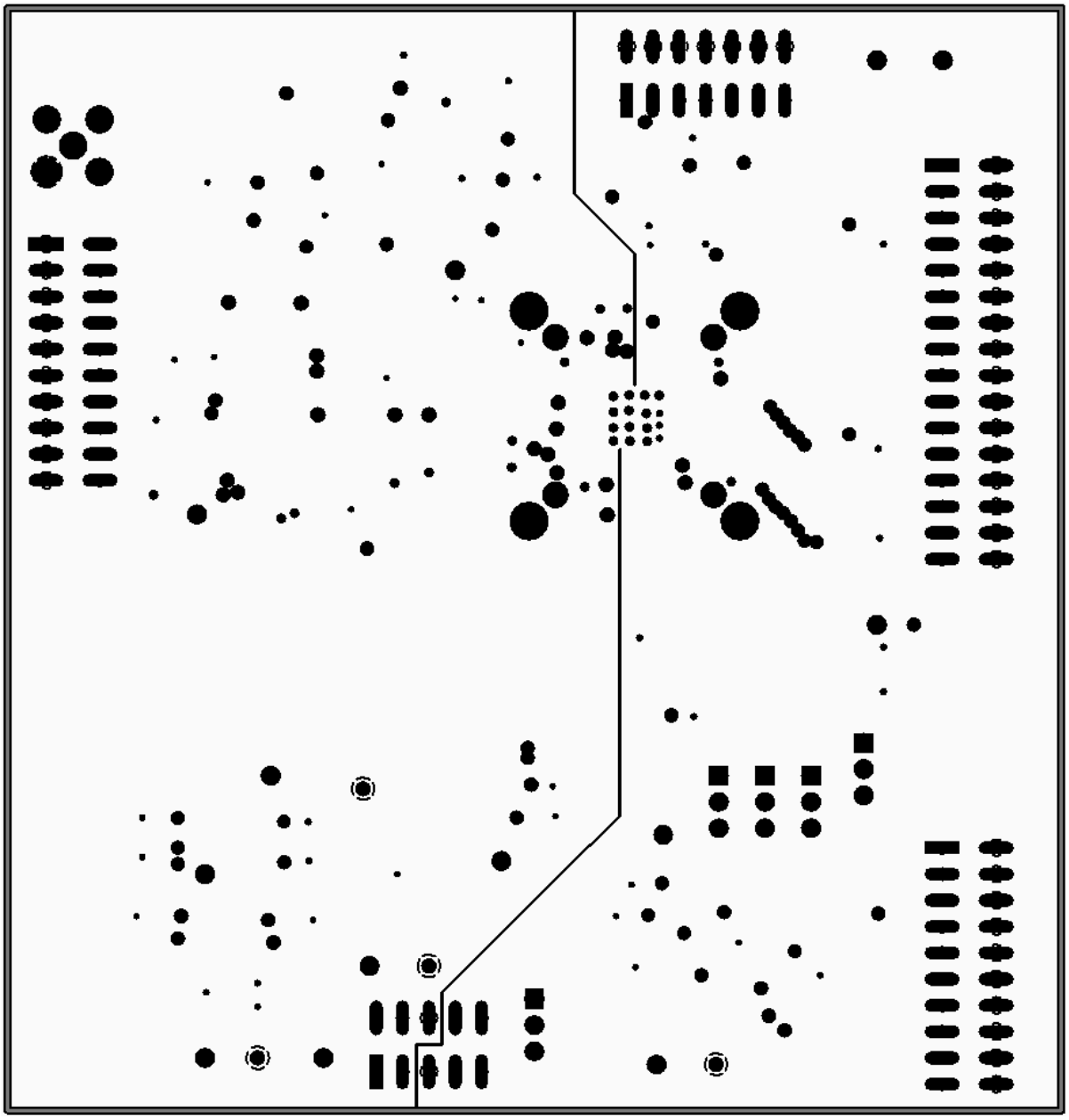

Figure 4-2. Ground Plane – Layer 2

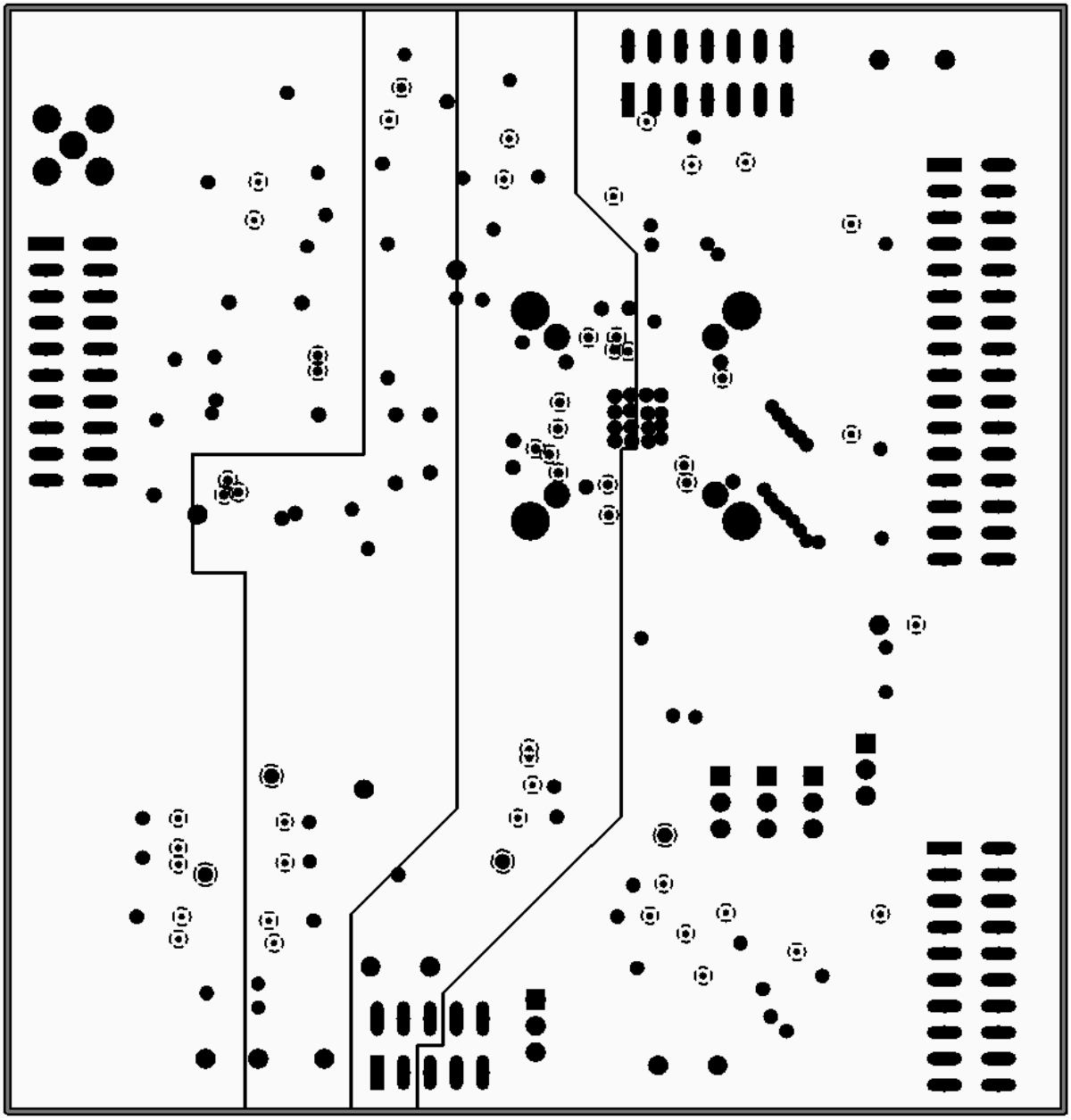

Figure 4-3. Power Plane – Layer 3

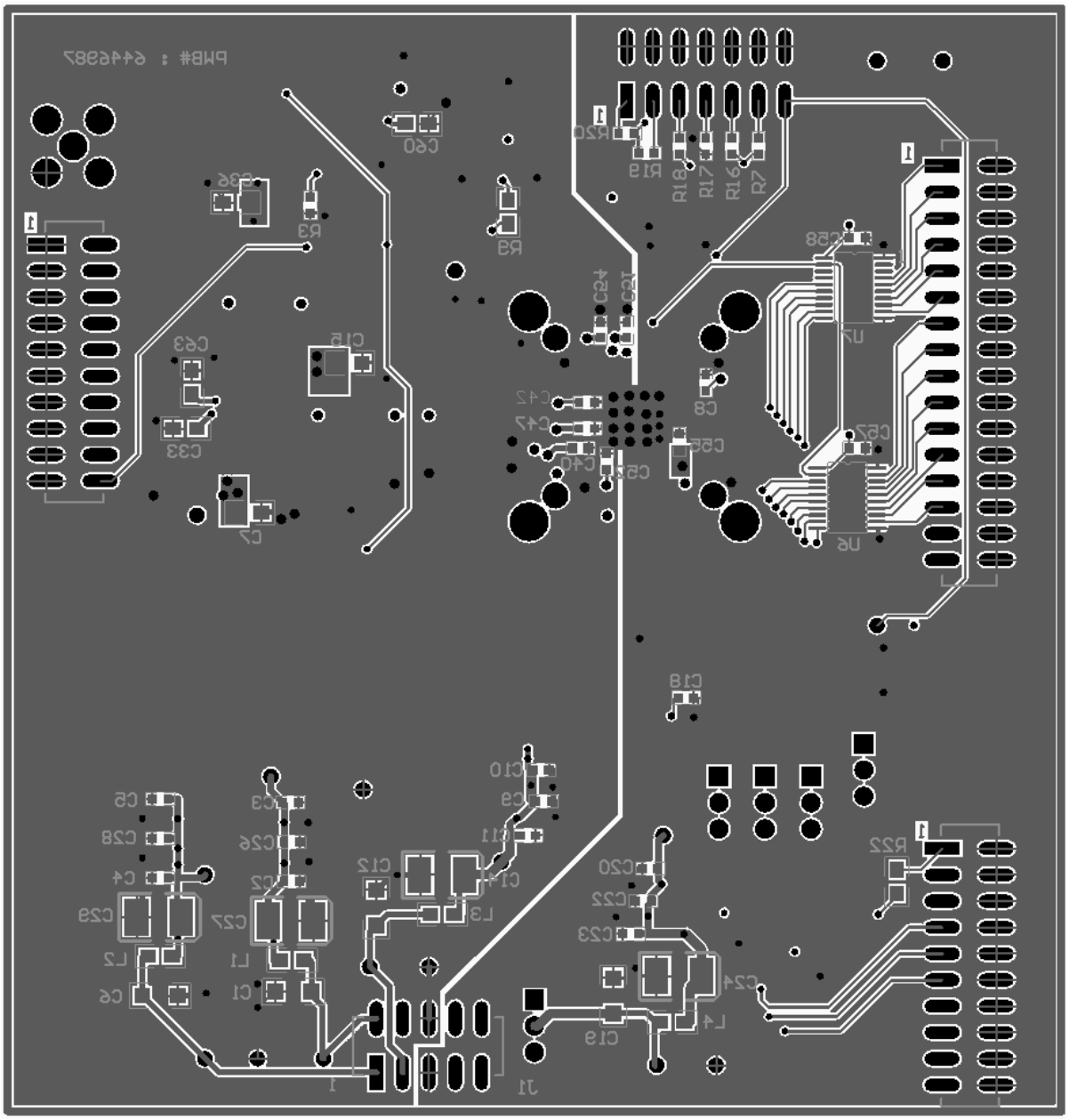

Figure 4-4. Bottom Layer – Layer 4

5 ADS78x1EVM Schematics

Figure 5-1 to Figure 5-3 illustrate the schematic drawings for the ADS78x1EVM.

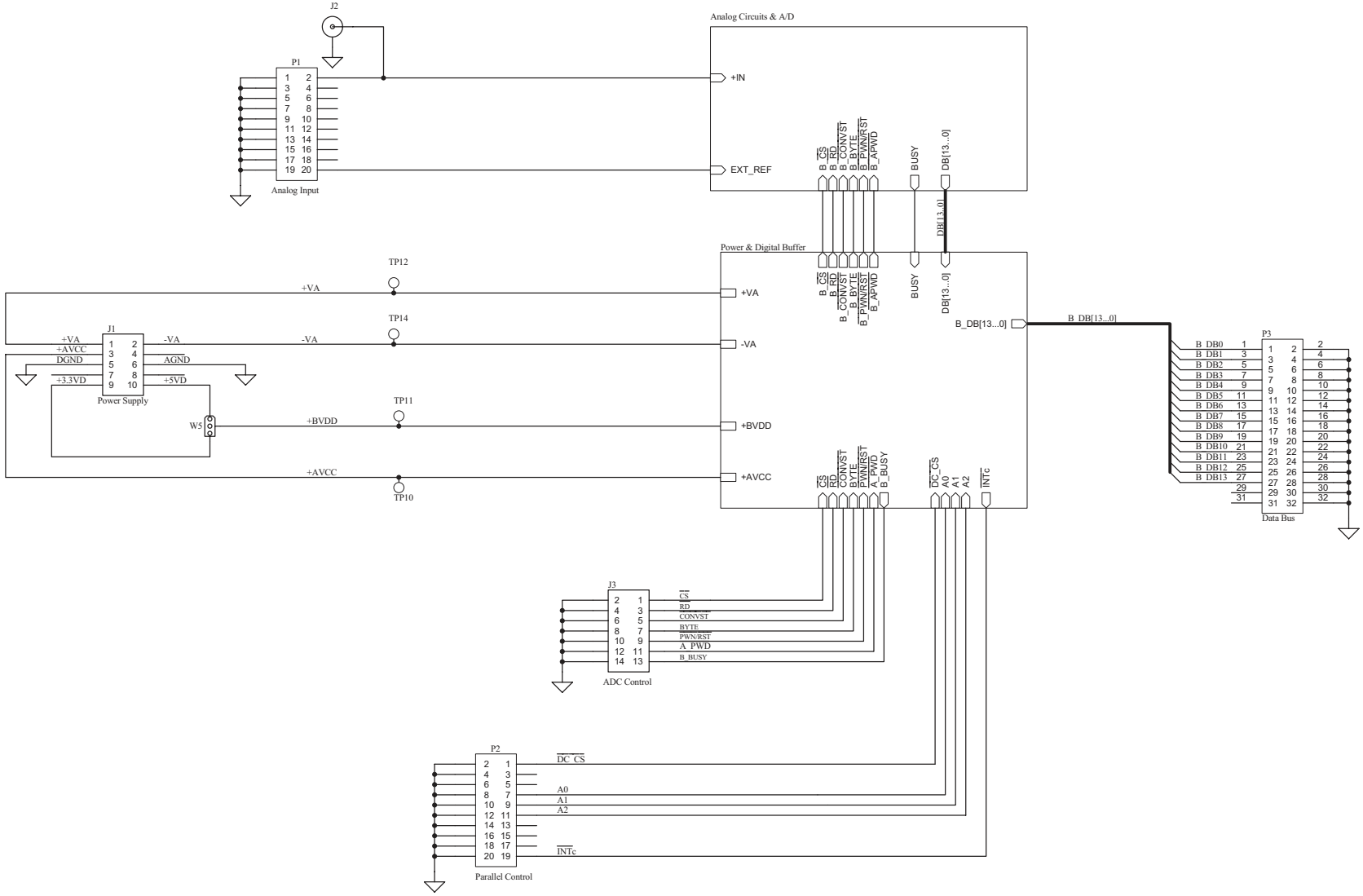

Figure 5-1. Schematic Page 1: Digital Buffer

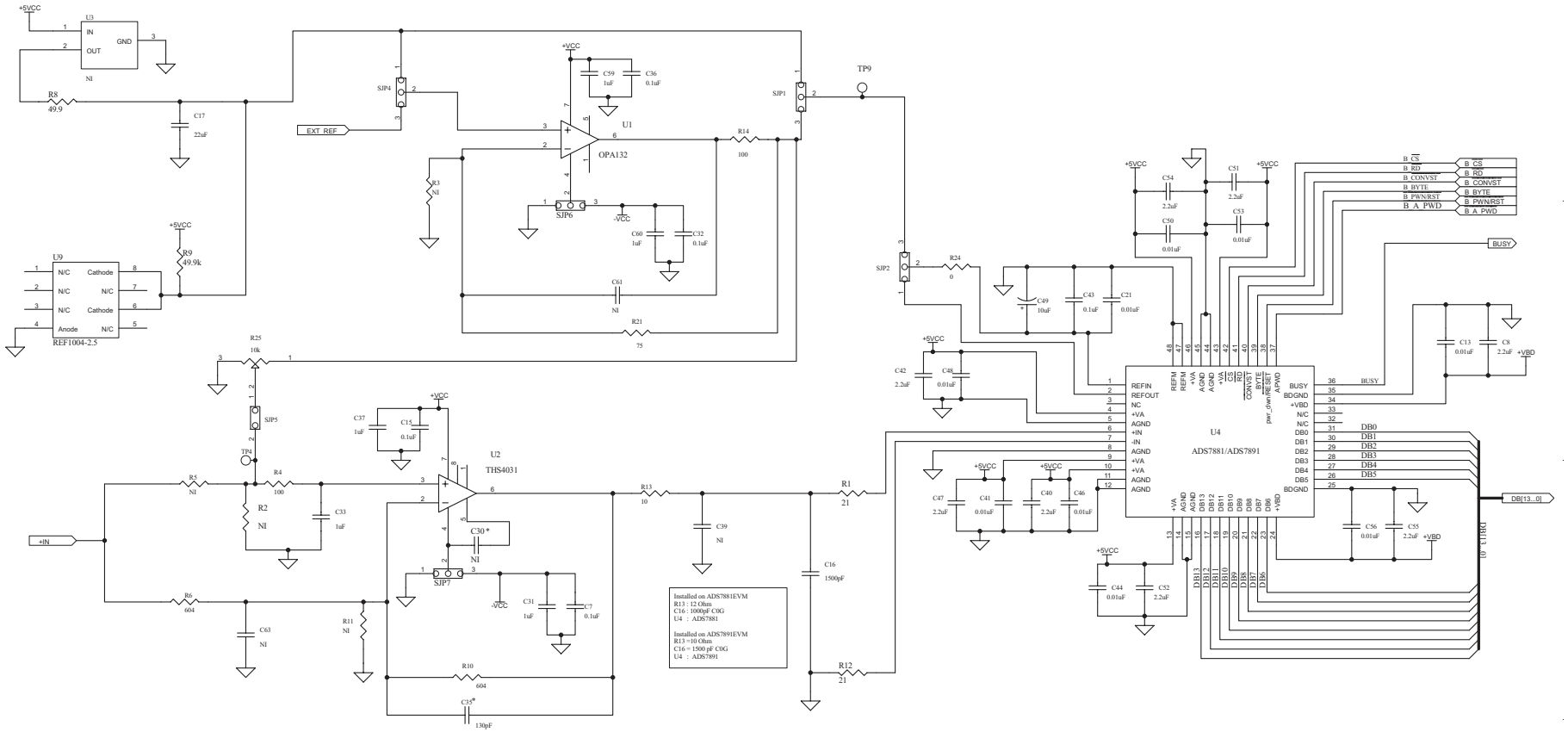

Figure 5-2. Schematic Page 2: ADS7881, ADS7891

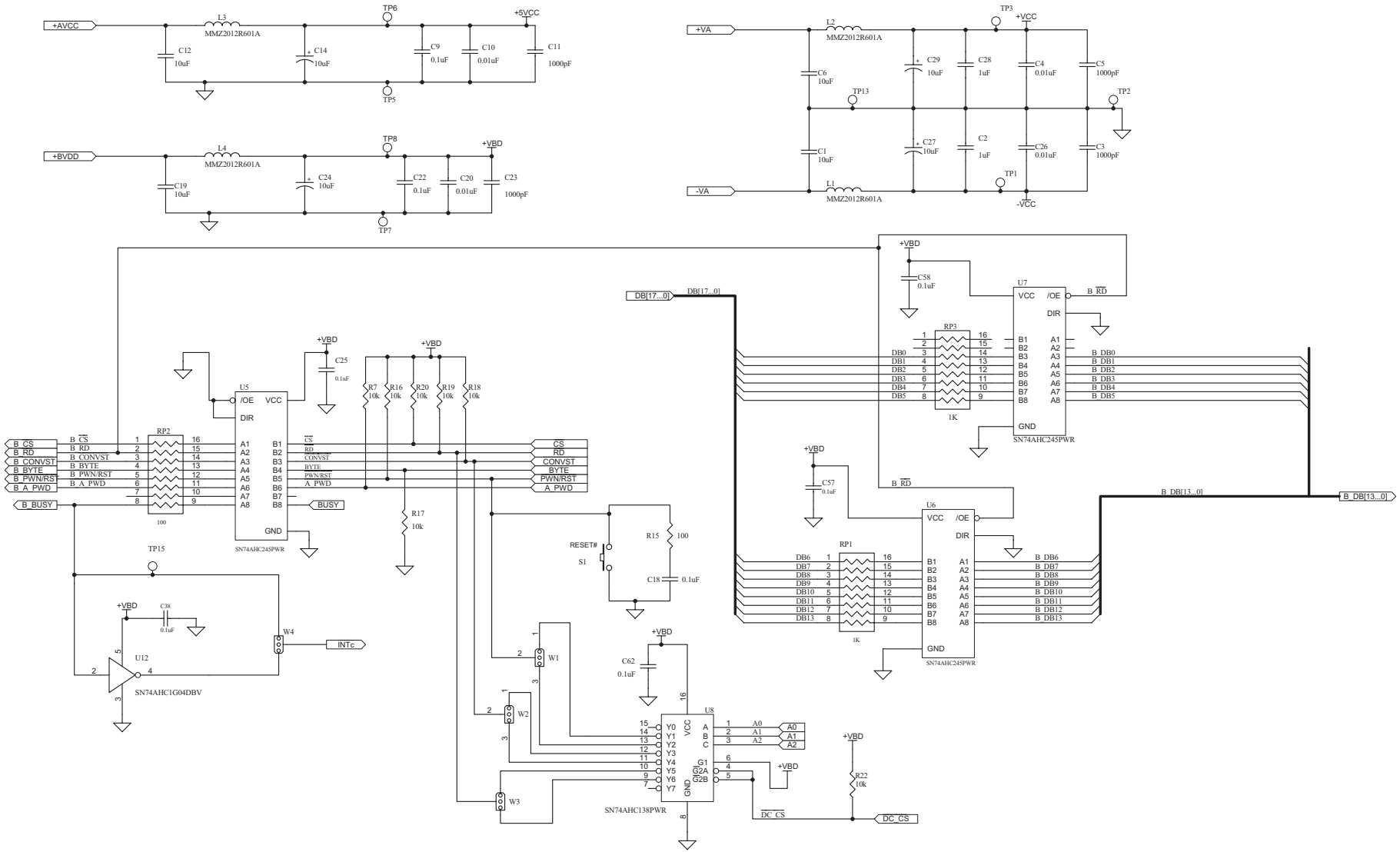

Figure 5-3. Schematic Page 3: Digital Communication

6 Revision History

Changes from Revision * (December 2004) to Revision A (October 2021)	Page
• Changed document title from *ADS7881/ADS7891EVM* to *ADS7881EVM, ADS7891EVM Evaluation Module*	1
• Changed *ADS7881/ADS7891EVM* to *ADS78x1EVM* throughout document	1
• Added *Related Documentation from Texas Instruments* table to *Introduction* section	2
• Changed paragraph preceding *Data Bus Connector P3*	4
• Changed *Data Bus Connector P3* table	4

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