Reliability Report

To Measure PCI-e Reference Clock With Multiplexers

ABSTRACT

PCI Express (PCIe) is widely used across a range of applications, including personal computers, storage devices, networking, communications, cluster interconnect etc. This application test report provides an overview of PCI Express (PCIe) reference clocking architectures. A test report with TI high speed multiplexers will be presented and discussed.

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Trademarks

1 Introduction

PCI Express (PCIe) is a serial point-to-point interconnect standard developed by the Peripheral Component Interconnect Special Interest Group (PCI-SIG). The PCIe standard has been widely adopted in a broad range of applications including desktop personal computers, servers, storage devices, embedded computing, and networking and communications. One of the key advantages of using PCIe is its scalable data bandwidth and flexible clocking solutions. This application report will explore some of the standard clocking architectures for PCIe first and a reference clock test result with TI high speed multiplexers will be presented and discussed later.

2 What is PCI Express (PCIe)?

2.1 PCIe Link

Before considering clocking architectures, examine the PCIe data link. It consists of one or more lanes that provide a transmit (Tx) and receive (Rx) differential pair. Figure 2-1 shows two devices that need to transfer data. One of the key advantages of PCIe is its bandwidth scalability enabling up to 32 lanes to be configured on a single link. Table 2-1 is the data rate vs different PCIe standard.

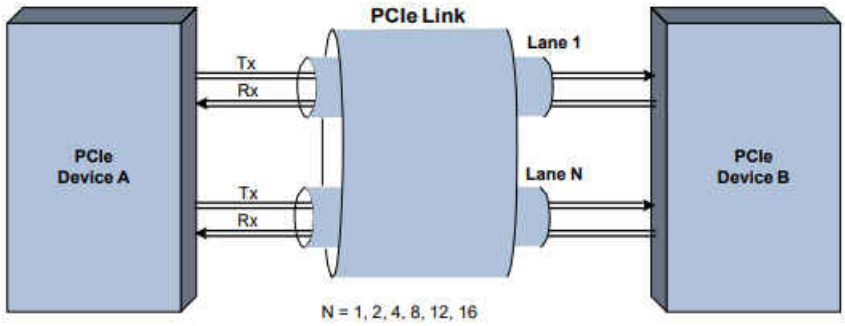

Figure 2-1. PCIe Link

Table 2-1. PCIe Standard Versus Bit Rate

PCIe Standard	Raw Bit Rate
PCIe 1.1	2.5 GBit/s
PCIe 2.1	5.0 GBit/s
PCIe 3.1	8.0 GBit/s
PCIe 4.0	16.0 GBit/s
PCIe 5.0	32.0 GBit/s

2.2 PCIe Clocking Architectures

The PCIe standard specifies a 100 MHz clock (Refclk) with at least ±300 ppm frequency stability for Gen 1, 2, 3 and 4, and at least ±100 ppm frequency stability for Gen 5, at both the transmitting and receiving devices. It also specifies support for three different clocking architectures: Common Clock, Data Clock, Separate Reference Clocks.

2.2.1 Common Reference Clock

Figure 2-2 shows the common refclk architecture. In the common refclk architecture, the same reference clock is distributed to both transmit (Tx) and receive (Rx) devices, so it does not introduce any difference in clock between the PCIe components. An advantage of this clocking architecture is that it supports spread spectrum clocking (SSC), which can be very useful in reducing EMI.

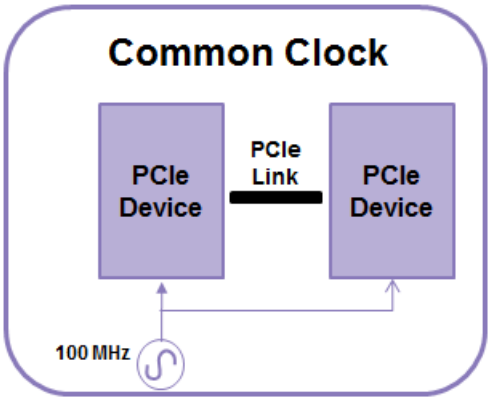

Figure 2-2. Common Clock Architecture

2.2.2 Data Reference Clock

Figure 2-3 shows the Data refclk architecture. The Data refclk architecture is the simplest to implement since it only requires one clock source located at the transmitter. Although the Data refclk architecture has a simpler block diagram, its jitter requirements are more difficult to meet because less filtering is applied. The data refclk architecture is only supported in PCIe Gen 2 and Gen 3.

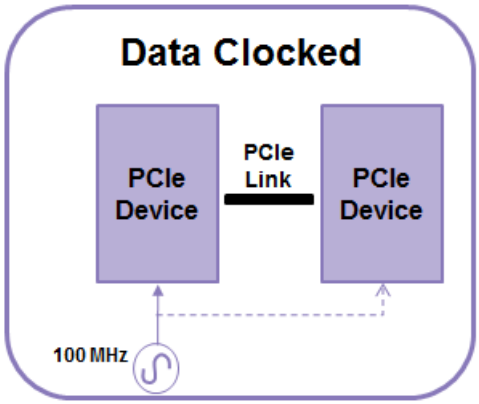

Figure 2-3. Data Clock Architecture

2.2.3 Separate Reference Clock

Another clocking architecture is the Separate Reference architecture where a different clock source is used at each end of the PCIe link. The advantage of this architecture is that tightly controlled reference clock distribution is no longer required over connectors and backplanes.

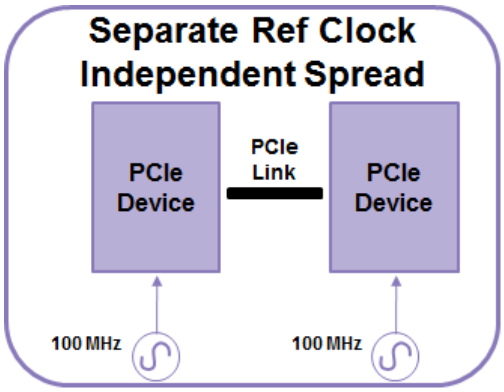

Figure 2-4. Seperate Clock Architecture

From three refclk architecture, the common refclk architecture is the easiest and most commonly used method for clock distribution among PCIe devices. Only test common refclk architecture is tested in this application report.

2.3 PCIe Reference Clock Specification

Table 2-2 shows the PCIe reference clock specification

Table 2-2. PCIe Reference Clock Specification

Parameter	Min	Max	Unit
Frequency	99.97	100.03	Mhz
Absolute Max Input Voltage		1.15	V
Absolute Min Input Voltage		-0.3	V
Crossing Voltage	+250	+550	mV
Duty Cycle	40	60	%
Max Jitter (Gen1)		86	PS (Rms)
Max Jitter (Gen2)		3.1	PS (Rms)
Max Jitter (Gen3)		1.0	PS (Rms)
Max Jitter (Gen4)		1.0	PS (Rms)

3 Reference Clock Measurement With TI Multiplexers

3.1 Test Setup and Procedure

A 100 Mhz reference clock from PCIe add-in card is used as clock source for the measurement. Three TI high speed multiplexers TMUXHS4412, TMUXHS221 and HD3SS3411 are used as pass though for the setup. Measurements were took at the output of the multiplexers by sampling scope DCA-X 86100D.

3.1.1 Test Setup

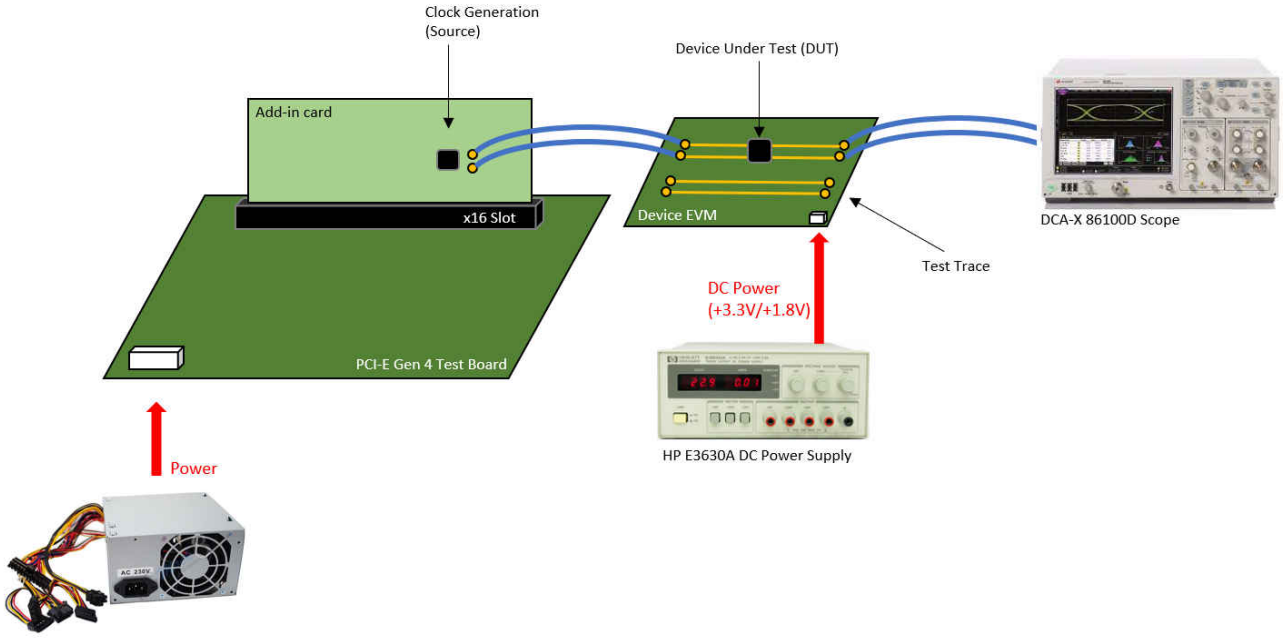

Figure 3-1. Test Setup for PCIe Reference Clock Mesurement

Figure 3-1 is the setup for PCIe reference clock test. It includes:

- 100 Mhz clock source (PCIe Add-in card)
- EVMs of TMUXHS4412, TMUXHS221 and HD3SS3411
- Power supply
- DCA-X 86100D sampling scope

3.1.2 Test Procedure

1. Directly measure electrical performance of the clock source with scope.
2. Connect clock source to the calibration trace on one of the Mux EVM and measure electrical performance of the clock signal passing though the trace with scope.
3. Connect clock source to the input of the Mux EVM and measure electrical performance of the output of the Mux with scope.
4. Repeat 1-3 and measure the electrical performance of the output of the other Muxes with scope.

3.2 Test Report

3.2.1 Test Result With Clock Source

Table 3-1 shows the test result with clock source only.

Table 3-1. Test Result With Clock Source

Parameter	Clock +	Clock-	Unit
Frequency	100.1+-14k	100.1+-19k	Mhz
Amplititude	587	589	mV
Jitter	1.08	1.08	Ps (Rms)
Duty Cycle	50.2	48.8	%
Rise Time	294	310	Ps
Fall time	228	261	Ps
Vcross	263/190	NA	mV

3.2.2 Test Result With HD3SS3411

Table 3-2 shows the test result with EVM trace only and trace + HD3SS3411.

Table 3-2. Test Result With HD3SS3411

Parameter	With Trace Only		With Trace +HD3SS3411		Unit
	Clock +	Clock-	Clock +	Clock -	
Frequency	100.1+-14k	100.1+-19k	100.1+-17k	100.1+-15k	Mhz
Amplitude	524	519	504	500	mV
Jitter	1.01	1.01	1.03	1.03	Ps (Rms)
Duty Cycle	50.1	48.6	50.2	48.6	%
Rise Time	367	382	396	416	Ps
Fall time	310	316	339	338	Ps
Vcross	266/196	NA	257/199	NA	mV

3.2.3 Test Result With TMUXHS4412

Table 3-3 shows the test result with EVM trace only and trace + TMUXHS4412.

Table 3-3. Test Result With TMUXHS4412

Parameter	With Trace Only		With Trace +TMUXHS4412		Unit
	Clock +	Clock-	Clock +	Clock -	
Frequency	100.1+-13k	100.1+-10k	100.1+-12k	100.1+-11k	Mhz
Amplitude	529	548	488	504	mV
Jitter	1.03	1.03	1.06	1.06	Ps (Rms)
Duty Cycle	50.3	49	50.3	49	%
Rise Time	327	396	329	341	Ps
Fall time	302	373	287	375	Ps
Vcross	265/193	NA	260/179	NA	mV

3.2.4 Test Result With TMUXHS221

Table 3-4 shows the test result with EVM trace only and trace + TMUXHS221

Table 3-4. Test Result With TMUXHS221

Parameter	With Trace Only		With Trace +TMUXHS221		Unit
	Clock +	Clock-	Clock +	Clock -	
Frequency	100.1+-11k	100.1+-15k	100.1+-16k	100.1+-16k	Mhz
Amplitude	521	520	512	504	mV
Jitter	1.02	1.02	1.03	1.03	Ps (Rms)
Duty Cycle	50.1	48.7	50.2	48.7	%
Rise Time	348	327	458	470	Ps
Fall time	312	301	427	398	Ps
Vcross	253/193	NA	239/181	NA	mV

4 Summary

The above test results show:

- Jitter performance and frequency almost same with or without Mux devices.
- Due to the loss of Mux, clock amplitude is reduced about 5% but still meet PCIe reference clock specification.
- Rise/fall time is slower with Mux devices.
- Vcross didn't change much with or without Mux devices.

Overall, the clock signal passing though TI high speed multiplexers can still meet PCIe Gen1 to Gen4 reference clock specification. To ensure proper compliance with the PCIe standard, systems that use the PCIe interface require careful attention to the timing subsystem and architecture. Designers must consider which of the three PCIe specified reference clock architectures – Common Clock, Data Clock, Seperate Clock– will meet their application’s functional and performance goals.

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