Application Note

Y-Bridge in TAS278x Class-D Amplifiers for Improving Efficiency

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ABSTRACT

As battery-powered devices such as laptops, tablets, and smart wireless speakers continue to integrate more advanced features, power efficiency has become a critical design consideration. To address this challenge, Texas Instruments (TI) has developed the Y-Bridge power architecture—an remarkable enhancement to conventional Class-D audio amplifier design. This advanced architecture is implemented in TI's latest TAS2781 and TAS2783 devices, which are digital-input Class-D smart audio amplifiers featuring integrated digital signal processing (DSP) and speaker protection algorithms. This application note provides an in-depth overview of the Y-Bridge architecture, detailing how this intelligently manages power supply selection to optimize voltage headroom, thereby improving overall amplifier efficiency and reducing battery power consumption. The application note also explores practical implementation scenarios and outlines the key advantages of the Y-Bridge design over traditional Class-D amplifier designs.

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Trademarks

1 Introduction

Traditional audio amplifier architectures rely on a single high-voltage supply rail (PVDD) for output stage switching and amplification, alongside a low-voltage rail for I/Os and LDOs. However, during idle periods—when no audio signal is present—amplifiers continue to switch, resulting in poor power efficiency. Because the switching occurs exclusively on the high-voltage rail, the excess voltage headroom leads to idle efficiencies falling below 20%. To overcome this limitation, Texas Instruments has introduced the Y-Bridge power architecture. This intelligent design allows the amplifier to seamlessly alternate between two supply rails based on the output power demand. By optimizing the supply voltage in real time, the Y-Bridge architecture significantly reduces idle power consumption—by up to 90%—and improves efficiency by 15% to 20% at lower output levels, all without compromising audio performance. Combined with TI's advanced speaker protection and signal processing algorithms, this design empowers OEMs to maximize battery life and overall system performance in next-generation portable audio applications.

2 What is Y-Bridge

As the name implies, the Y-Bridge power architecture resembles a "Y" configuration, in contrast to the conventional linear half-bridge topology. In a traditional half-bridge Class-D amplifier, the output stage operates solely from a single high-voltage supply rail (PVDD), regardless of the output power requirement. This results in substantial efficiency losses during low-power or idle conditions, where the full voltage headroom is unnecessary. The Y-Bridge architecture addresses this limitation by incorporating both a high-voltage rail (PVDDH) and a low-voltage rail (PVDDL) into the output stage.

At low output power levels, including idle states, the amplifier operates from the lower voltage rail (PVDDL), as the required headroom is minimal and can be met without risking signal clipping. This approach significantly improves power efficiency at lower output levels. When higher output power is demanded, the amplifier seamlessly transitions to the high-voltage rail (PVDDH), delivering the necessary headroom without compromising performance. In this state, the system's efficiency aligns with that of a traditional Class-D amplifier. As a result, the Y-Bridge architecture delivers the most notable efficiency gains at low to moderate output levels—where conventional amplifiers typically operate least efficiently.

Figure 2-1 illustrates the structural and operational differences between a traditional Class-D amplifier and one utilizing the Y-Bridge architecture.

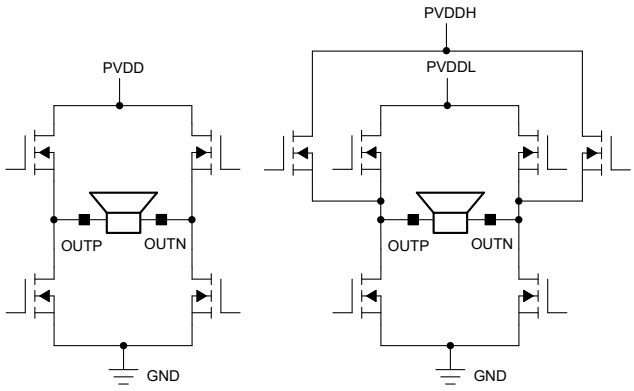

Figure 2-1. Traditional Class-D Amplifier vs Simplified Y-Bridge Architecture

Texas Instruments' latest audio amplifiers, the TAS2781 and TAS2783, incorporate the Y-Bridge architecture to enhance power efficiency during audio playback. Figure 2-2 shows the functional block diagram of the TAS278x device. The Y-Bridge feature can be enabled or disabled through device configuration, providing flexibility based on system requirements. Additionally, the amplifiers can be set to operate exclusively from either the low-voltage rail (PVDDL) or the high-voltage rail (PVDDH), depending on the desired performance characteristics. When configured to use only PVDDL or PVDDH, this is critical to make sure that the selected supply voltage is sufficient to avoid output clipping, particularly under higher output demands. Detailed description on these configurations and the operational implications is provided in Section 3.

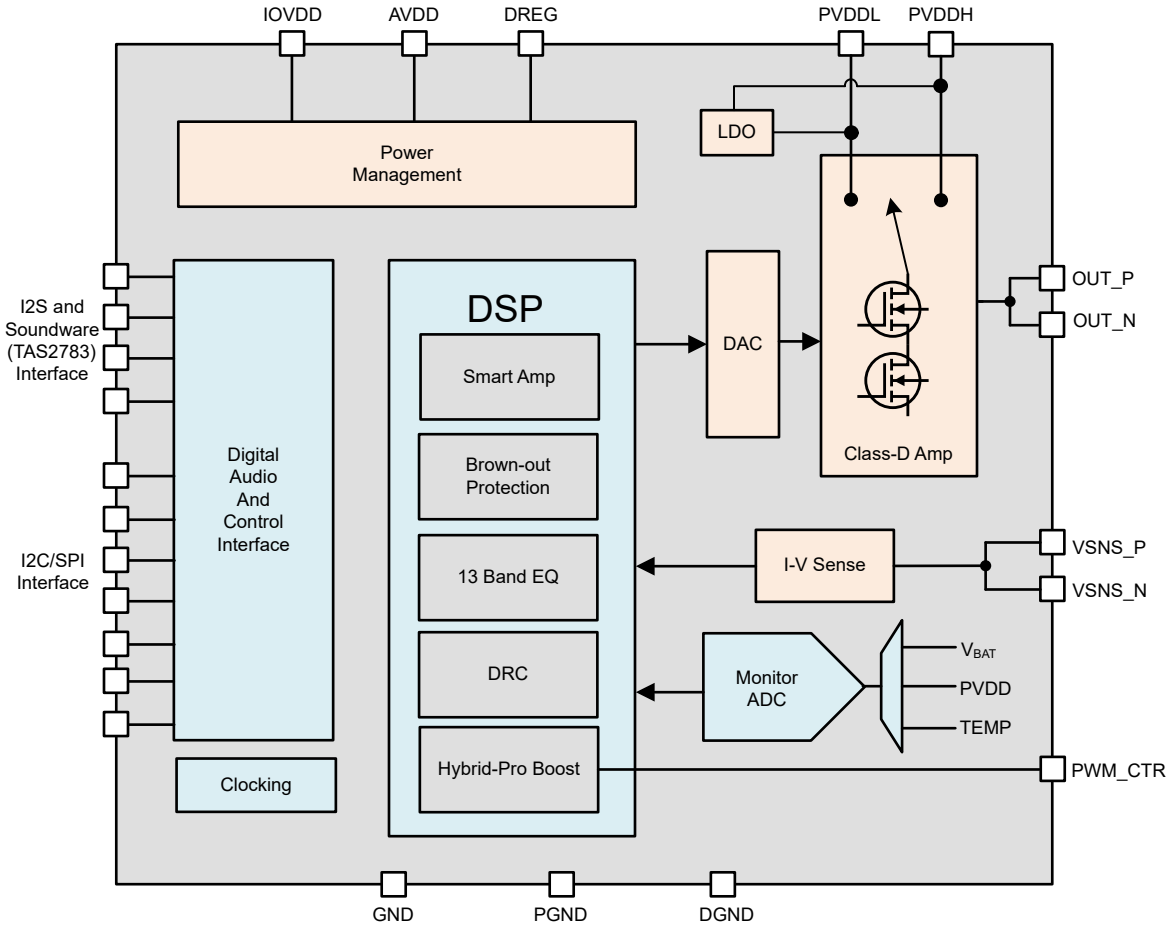

Figure 2-2. Functional Block Diagram of TAS278x with Y-Bridge Feature

3 Class-D Switching Modes and Register Settings

The TAS2781 and TAS2783 devices are highly configurable and support multiple power supply configurations to accommodate various system requirements. The devices can operate using both PVDDL and PVDDH supply rails for dynamic switching through the Y-Bridge architecture, or the devices can be configured to run exclusively from either PVDDH or PVDDL.

Table 3-1 summarizes the available power supply modes and the corresponding use cases, enabling designers to select the most efficient configuration based on application-specific needs.

Table 3-1. Class-D Switching Power Modes

Power Modes	PVDDL_MODE	CDS_MODE	Y-Bridge	Description
PWR_MODE0	0	10	Disabled	Both **PVDDH** and **PVDDL** are **externally** supplied to the device; however, only **PVDDH** is utilized for Class-D switching, while **PVDDL** powers the gate drivers and internal circuitry.
PWR_MODE1 (default)	0	00	**Enabled**	Both **PVDDH** and **PVDDL** are supplied to the device **externally** and used for Class D switching. The Y-Bridge feature is **enabled** in this mode.
PWR_MODE2	1	11	**Enabled**	Only **PVDDH** is supplied externally, while **PVDDL** is generated **internally** by the device. Both **PVDDH** and **PVDDL** are used for Class-D switching, and the Y-Bridge feature is **enabled**. When the audio signal level exceeds the default threshold of –71.5 dBFS, as defined by the LVS_TH_LOW[2:1], the Class-D output switches to the **PVDDH**. Only the idle channel switching occurs from **PVDDL**.
PWR_MODE3	0	01	Disabled	Only **PVDDL** is supplied to the device **externally**, and the device can be forced to operate solely from the **PVDDL** rail for Class-D switching. However, the **PVDDH** supply is still **required** and must satisfy the condition PVDDH > PVDDL + 0.7V to make sure of proper device operation, even though PVDDH is not actively used for audio switching in this mode.

Table 3-2. Power Mode Register Settings

Address	Field [Bits]	Type	Reset	Description
0x04	PVDDL_MODE[7]	RW	21h	PVDDL supply is 0h = Supplied externally (default) 1h = Internally generated from PVDDH
0x03	CDS_MODE[7:6]	RW	28h	Class-D switching mode 0h = PWR_MODE1 (default) 1h = PWR_MODE3 2h = PWR_MODE0 3h = PWR_MODE2

This application note focuses specifically on *PWR_MODE1* and *PWR_MODE2*, as these are the two configurations that support the Y-Bridge feature as shown in Table 3-1 and is discussed in detail in the following sections.

4 PWR_MODE1 [CDS_MODE = 00]

In this configuration, both PVDDH and PVDDL supply rails are externally provided and used for Class-D switching, and the Y-Bridge feature is enabled.

The TAS278x devices integrate a mechanism to monitor the absolute amplitude of the incoming audio stream to determine the appropriate supply rail—PVDDH or PVDDL. When the audio signal exceeds a programmable Low Voltage Signaling (LVS) threshold (configured as either fixed or relative), the Class-D stage switches to the higher voltage rail (PVDDH) to prevent signal clipping. If the signal remains below this threshold for a period longer than the hysteresis duration—defined by the *LVS_HYS[3:0]* register bits—the amplifier transitions to the lower voltage rail (PVDDL) to conserve power. When the signal again exceeds the threshold, the supply switches back to PVDDH.

By default, the LVS threshold is set relative to the PVDDL voltage (*LVS_DET = 1*). The relative threshold level is configured using the *LVS_RTH[3:0]* register bits, with a default value of 0.7V. Alternatively, setting *LVS_DET = 0* enables a fixed LVS threshold defined by the *LVS_FTH[4:0]* register bits. The LVS threshold is referenced against the output signal level and expressed in dBFS.

The relative threshold voltage at which the amplifier switches from PVDDL to PVDDH is calculated as:

Relative Threshold (Vp) = (PVDDL × Class-D Efficiency – Relative Threshold Headroom) / Inflection Factor

Where:

- Relative Threshold Headroom is defined by the LVS_RTH register
- Class-D Efficiency is typically 85% (0.85)
- Inflection Factor is a fixed design parameter of 1.2

For example, for PVDDL = 5V, Relative Threshold for Y-Bridge switching = (5 × 0.85 – 0.7) / 1.2 = 2.96 Vp

This intelligent rail-switching mechanism enables the Y-Bridge architecture to maintain audio performance while significantly improving power efficiency, particularly at lower output levels.

Table 4-1. PWR_MODE1 Register Settings

Address	Field [Bits]	Type	Reset	Description
0x37	LVS_DET[7]	RW	A8h	LVS detection threshold for PWR_MODE1: 0h = Fixed 1h = Relative to PVDDL voltage (default)
0x37	LVS_FTH[4:0]	RW	A8h	LVS Fixed threshold for PWR_MODE1: CDS_MODE=0h 00h = -18.5dBFS 01h = - 18.25dBFS ……... 08h = - 16.5dBFS (default) ……... 1Eh = -11dBFS 1Fh = - 10.75dBFS
0x6A	LVS_RTH[3:0]	RW	12h	LVS Relative Threshold Headroom for PWR_MODE1: CDS_MODE=0h 0h = 0.5V 1h = 0.6V 2h = 0.7V (default) …… Eh = 1.9V Fh = 2V

Table 4-1. PWR_MODE1 Register Settings (continued)

Address	Field [Bits]	Type	Reset	Description
0x36	LVS_HYST[3:0]	RW	ADh	PVDDH to PVDDL Hysteresis time (PWR_MODE1 and PWR_MODE2) 0h - 9h = Reserved Ah = 1ms Bh = 10ms Ch = 20ms Dh = 50ms (default) Eh = 75ms Fh = 100ms *For sampling rates fs < 48 ksps multiply the above values by 48/fs
0x14-0x17	CLASSD_EFF[31:0]	RW	6CCCCCCCh	Class-D Efficiency set to a EFF (%) value dec2hex [round (EFF*2^31)]

5 PWR_MODE2 [CDS_MODE = 11]

In this configuration, only the PVDDH rail is supplied externally, while the PVDDL voltage is generated internally by the device. Both PVDDH and PVDDL are used for Class-D switching, and the Y-Bridge feature is enabled in this mode.

The amplifier monitors the audio signal level and, when this exceeds a fixed Low Voltage Signaling (LVS) threshold of –71.5 dBFS (default, set through the *LVS_TH_LOW[2:1]* register bits), the Class-D output switches from PVDDL to PVDDH. In this mode, only idle channel switching occurs on the PVDDL rail, while active audio playback uses PVDDH once the signal crosses the threshold.

Table 5-1. PWR_MODE2 Register Settings

Address	Field [Bits]	Type	Reset	Description
0x34	LVS_TH_LOW[2:1]	RW	06h	LVS Fixed Threshold for PWR_MODE2: CDS_MODE=3h 0h = - 121.5dBFS 1h = - 101.5dBFS 2h = - 81.5dBFS 3h = - 71.5dBFS (default)

To fully utilize the Y-Bridge functionality in PWR_MODE2, this is essential that the PVDDH supply is at least 2.5V higher than the internally generated PVDDL. For example, if PVDDL is internally set to 4.8V, PVDDH needs to be no less than 7.3V. To safeguard this requirement, the under-voltage protection threshold for PVDDH needs to be configured using the *PVDDH_UV_TH[5:0]* register bits. Setting this threshold appropriately makes sure the voltage headroom is maintained for seamless Y-Bridge operation.

Table 5-2. PVDDH Under Voltage Threshold

Address	Field [Bits]	Type	Reset	Description
0x71	PVDDH_UV_TH[5:0]	RW	02h	PVDDH under voltage thresholds 00h = 1.753V 01h = 2.09V 02h = 2.428V (default) …… 3Fh = 23V

Note, that if PVDDH drops below (PVDDL + 2.5V), the Y-Bridge feature can be disabled and the Class-D output can remain on PVDDH, regardless of signal level.

Additionally, the transition from PVDDL to PVDDH (or vice versa) in response to the audio signal crossing the LVS threshold is not instantaneous. A programmable delay governs this transition and can be configured using the *CDS_DLY[1:0]* register bits. This delay setting allows fine-tuning of the switching behavior to balance responsiveness and audio performance.

Table 5-3. Class D Switching Delay

Address	Field [Bits]	Type	Reset	Description
0x6A	CDS_DLY[7:6]	RW	12h	Delay (1/fs) of Y bridge switching wrt input signal

6 External Component Requirements

Designers must pay close attention to the recommended external components when implementing the Y-Bridge feature, particularly regarding decoupling requirements. A 100nF decoupling capacitor on the PVDDL rail is mandatory across all power modes to make sure of stable operation.

In addition to the 100nF capacitor (C2), specific power modes require further decoupling:

- For PWR_MODE0, PWR_MODE1, and PWR_MODE3, an additional 10µF capacitor (C1) on PVDDL is required.
- For PWR_MODE2, an additional 1µF capacitor (C1) is recommended due to the internal generation of PVDDL.

These component requirements are summarized in Table 6-1 and are essential for proper supply stability and the designed for Y-Bridge performance.

Table 6-1. Recommended External Components

Component	Description	Specification	Min	Typ	Max	Unit
C1	PVDDL Decoupling Capacitor - PVDDL External Supply (PWR_MODE0/1/3)	Capacitance, 20% Tolerance		10		µF
		Rated Voltage		10		V
	PVDDL Decoupling Capacitor - PVDDL Internally Generated (PWR_MODE2)	Capacitance, 20% Tolerance		1		µF
		Rated Voltage		10		V
C2	PVDDL Decoupling Capacitor	Capacitance, 20% Tolerance		0.1		µF
		Rated Voltage		10		V
C3	PVDDH Decoupling Capacitor	Capacitance, 20% Tolerance		10		µF
		Rated Voltage		25		V
C4	PVDDH Decoupling Capacitor	Capacitance, 20% Tolerance		0.1		µF
		Rated Voltage		25		V

Figure 6-1 shows the TAS2783 typical application circuit for the multi-cell battery system for the PWR_MODE0/1/3 with the additional 10uF decoupling capacitor (C1) on the PVDDL pin.

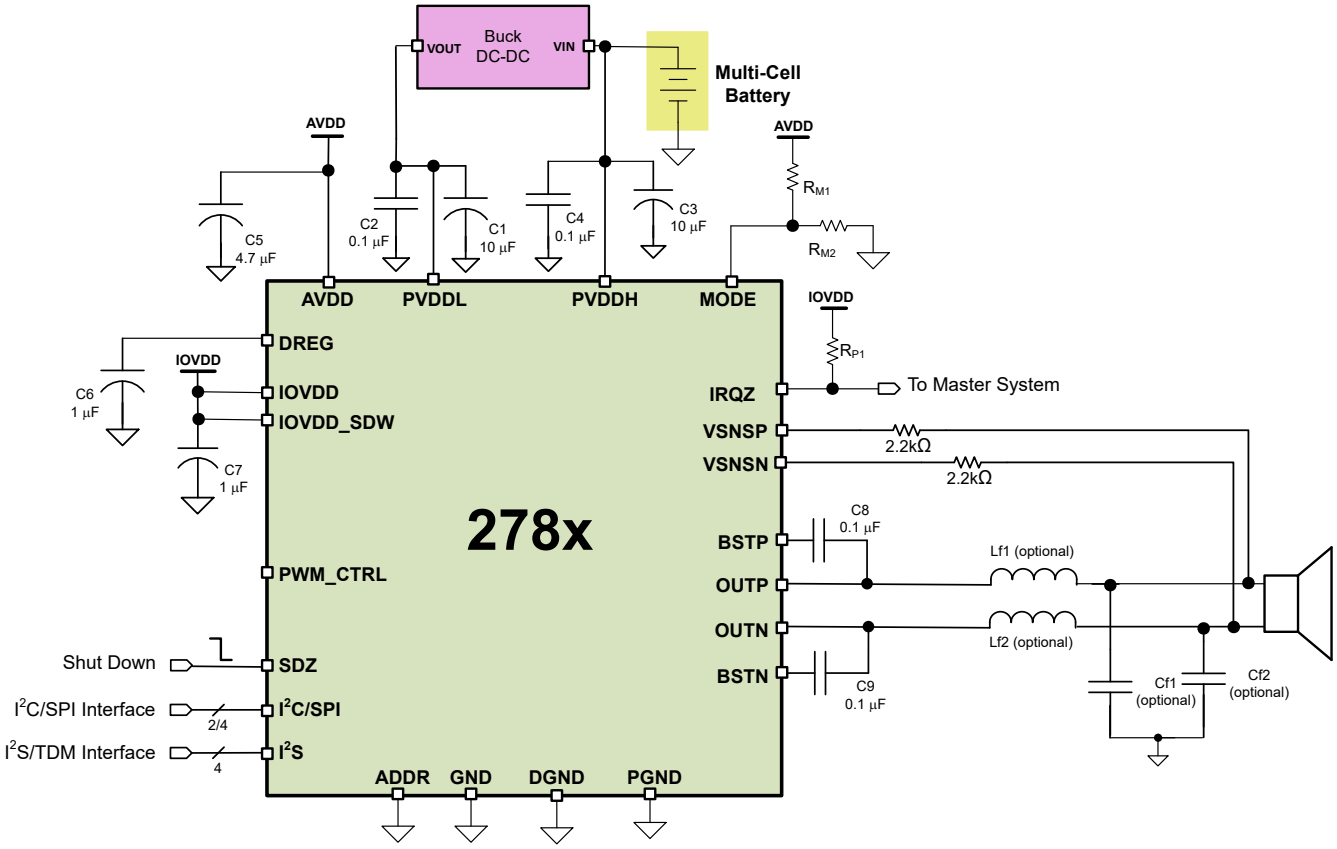

Figure 6-1. Typical Application Circuit - Multi-Cell Battery System

7 Benefits of Y-Bridge

The Y-Bridge architecture is particularly advantageous in systems that require a high-voltage power stage supply —such as those powered by 2S to 4S (2-cell to 4-cell) battery configurations (typically ranging from 7V to 14V). In the TAS2781 and TAS2783, this high-voltage input is supplied through the PVDDH pin, which supports a voltage range of 4V to 24V. PVDDH can be sourced either directly from a multi-cell battery or from the output of a boost converter in single-cell (1S) battery systems. The lower-voltage rail, PVDDL (ranging from 2.7V to 5.5V), is typically derived directly from a 1S battery or from a buck converter in 2S–4S configurations.

As illustrated in Figure 7-1, using the Y-Bridge architecture significantly improves efficiency at low output levels when compared to traditional Class-D amplifiers operating solely on a fixed high-voltage supply.

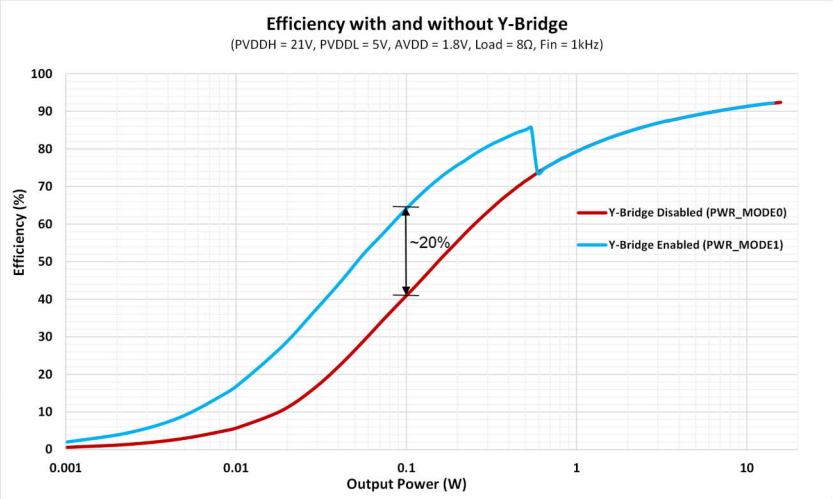

Figure 7-1. Efficiency Measured With and Without Y-Bridge

Figure 7-2 demonstrates that enabling the Y-Bridge feature can lead to up to 75% reduction in power consumption compared to operating without this. The extent of power savings varies depending on the application and audio content. For example, audio tracks with intermittent silence or low signal levels tend to realize greater efficiency gains than continuous high-energy content like music.

This reduction in power consumption can result in up to a 20% improvement in overall battery life, with no need for additional software control or system-level changes. The Y-Bridge functionality operates automatically based on signal conditions, providing a simple yet effective method to extend battery life in portable audio devices.

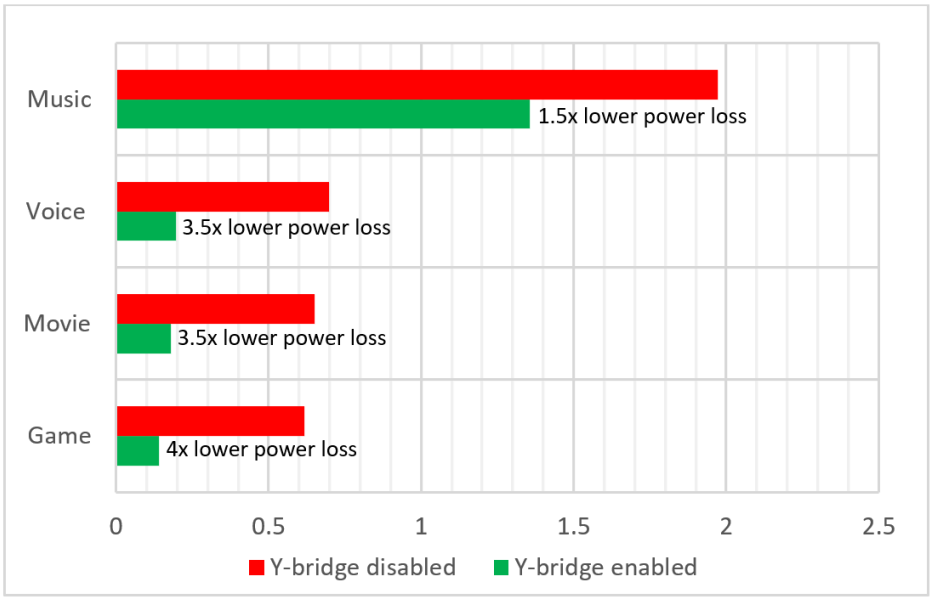

Figure 7-2. Power Consumption Measured in EVM Connected to Laptop Speakers (in W)

8 Summary

For audio designs requiring high efficiency and extended battery life, amplifiers with Y-Bridge architecture offer a compelling design. Texas Instruments' latest audio amplifiers integrate this architecture with advanced audio processing algorithms to deliver both power efficiency and high-performance sound quality. Implementing Y-Bridge technology enables reduced power consumption in AC-powered systems and significantly extends playback time in battery-operated devices.

To learn more about TI's portfolio of Y-Bridge-enabled audio amplifiers, visit TI.com.

9 References

- Texas Instruments, *TAS2781: 25 W, 4.5-V to 23-V, Digital-Input Integrated-Audio-Processing Speaker-Protection Class-D Amplifier*
- Texas Instruments, *Efficiency Improvement With Y-Bridge in TAS2x20, TAS257x*, application note
- Texas Instruments, *Audio Amplifiers: Amplify Your Audio System*

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