Application Note

EMC Improvement Guide for MSPM0

Eason Zhou

ABSTRACT

This application note outlines key EMC principles, compliance standards, and design optimization strategies for MSPM0 microcontrollers. The document provides practical guidance to troubleshoot EMS issues and enhance electromagnetic performance in MSPM0-based systems, while addressing international certification requirements through effective noise suppression and emission control techniques.

Table of Contents

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1 Introduction

This document presents an overview of Electromagnetic Compatibility (EMC) principles, standards, and implementation strategies for MSPM0 microcontrollers. Most of the content is provided in the checklist format.

Before product development with MSPM0, TI recommends to read these sections to have a better understanding to improve EMC in MSPM0-based systems from both software and hardware level.

- Section 2
- Section 3
- Section 4

When there is failure in EMC test, TI recommends to read these sections below to find the root cause and resolutions.

- Section 5
- Section 6

2 EMC and EMC Standards

2.1 EMC

Electromagnetic Compatibility (EMC) is a critical discipline in electronics engineering that verifies devices or systems to operate as intended within the electromagnetic environment without causing harmful interference to other devices (EMI) or being adversely affected by external electromagnetic disturbances (EMS). Thus, EMC encompasses two complementary aspects: Electromagnetic Interference (EMI) and Electromagnetic Susceptibility (EMS).

2.1.1 EMS

EMS (also called immunity) describes the ability of the device to function correctly when exposed to external electromagnetic disturbances. This measures resilience to:

- Radiated immunity: resistance to electromagnetic fields (for example, from radio transmitters).
- Conducted immunity: resistance to noise injected into power or signal lines (for example, voltage surges or electrostatic discharge).

2.1.2 EMI

EMI refers to unintentional electromagnetic energy emitted by a device or system that can disrupt the operation of nearby electronics. This is often categorized into two types:

- Radiated emissions: electromagnetic waves transmitted through the air (for example, radio frequency interference from a smartphone).
- Conducted emissions: noise propagated through power lines or cables (for example, harmonics from a motor affecting a power grid).

2.2 EMC Standards

Based on the EMC compliance requirement from different application scenarios, numerous EMC standards are established by international, regional, or industry bodies to define acceptable limits and testing methodologies for electromagnetic emissions and immunity. The most common communities are International Organization for Standardization (ISO), the International Electrotechnical Commission (IEC) and International Special Committee on Radio Interference (CISPR). Although there any many standard creators, the standard coverage can be listed into three key EMC standard categories as shown in Figure 2-1.

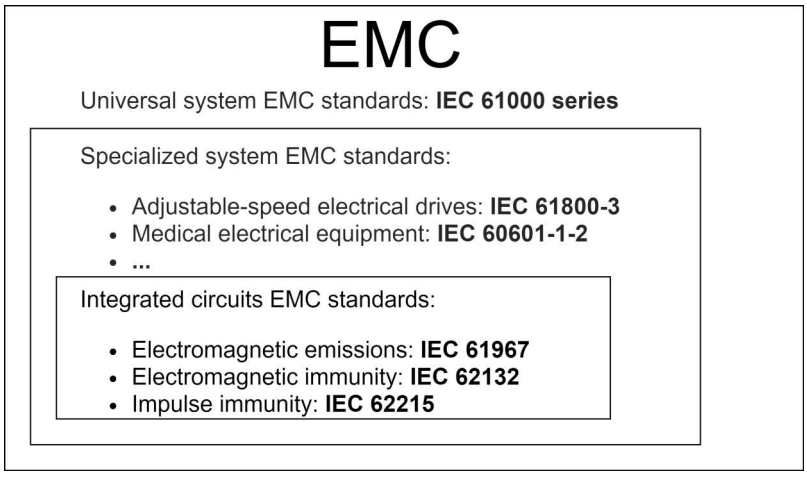


Figure 2-1. EMC Standards

The First EMC standard category is the universal system EMC standard, which describes the EMC test standards good for general products or PCB systems and sets minimum EMC performance metrics. An example is IEC 61000 series released by IEC. As IEC 61000 is the most common EMC standard, a more detailed introduction is given to the spread standards in the Section 2.2.1.

The second category is the specialized system EMC standards. To complement general requirements, some application-specific (for example, automotive, medical, aerospace) EMC standards are also developed to address unique EMC challenges, especially for EMI.

The third category is ICs EMC standards. Within the IEC framework, there are three core standards: IEC 61967, IEC 62132, and IEC 62215. These tests use standardized setups (for example, 100mm×100mm multilayer PCBs with predefined code) to evaluate IC behavior under controlled test environment. However, this dependency on system variables renders cross-IC comparisons statistically inconclusive, as differences in setup parameters (for example, PCB layer count, decoupling capacitor placement, or signal routing) can artificially amplify or mask intrinsic IC characteristics. As a result, this test data is provided by few semiconductor companies.

2.2.1 EMC Standards Category

The following section shows the EMC test coverage based on different EMC standards created by these organizations. First, use the IEC 610000 series as an example to show what EMS testing covers.

Table 2-1. EMS (Immunity) Testing Standards Overview

Test Type	Standard	Purpose	Test Method	Application Scope
ESD Immunity	IEC 61000-4-2	Evaluate immunity to electrostatic discharges from human/machine contact.	• Contact discharge (approximately 2 kV-8 kV); air discharge (approximately 2 kV-c15 kV). • Use an ESD Gun.	Consumer electronics, industrial equipment.
EFT/Burst Immunity	IEC 61000-4-4	Test immunity to fast transient disturbances (for example, relay switching).	• Approximately 50ns pulse bursts (0.5 kV to 4 kV, 5kHz repetition). • Coupled to power or signal lines by capacitive clamp.	Power supplies, motor drives, control systems.
Surge Immunity	IEC 61000-4-5	Assess immunity to high-energy surges (for example, lightning, load switching).	• Approximately 50µs voltage surge (line-to-line or line-to-ground, 0.5kV to 4kV). • Coupled via CDN or gas discharge tube.	Telecom systems, grid-connected devices.
Radiated RF Immunity	IEC 61000-4-3	Test immunity to radiated RF fields (for example, radio transmitters).	• RF signals (80MHz–6GHz) with a uniform field area (3V/m–30V/m). • Radiated by antenna at 3m distances.	Wireless devices, automotive electronics.
Conducted RF Immunity	IEC 61000-4-6	Evaluates immunity to RF interference coupled via cables/power lines.	• RF signals (150kHz–80MHz) with modulation (80% AM at 1kHz). • Injected via CDN or current clamp.	Medical devices, industrial automation.

Here are some EMI test standards listed to show what EMI testing covers. Compared with EMS, for EMI, the test standards and protection level is related to application.

Table 2-2. EMI (Electromagnetic Interference) Testing Standards Overview

Test Type	Standard	Purpose	Test Method	Application Scope
Radiated Emission	CISPR 25	Evaluates radiated emissions from automotive electronics	• RF signals (30 MHz–1 GHz). • Conducted in an anechoic chamber with antennas at 1m/3m/10m distances.	In-vehicle systems.
Conducted Emission	CISPR 22/32	Tests conducted emissions on power/signal lines.	• RF signals (150 kHz–30 MHz). • Uses LISN to measure quasi-peak and average values.	Power adapters, Industrial frequency converters.

2.3 EMC and IC Electrical Reliability in TI

IC electrical reliability is a part of the IC reliability. The related standards are HBM, CBM and latch up, which are released by JEDEC and ESDA, aim to verify long-term performance under stress.

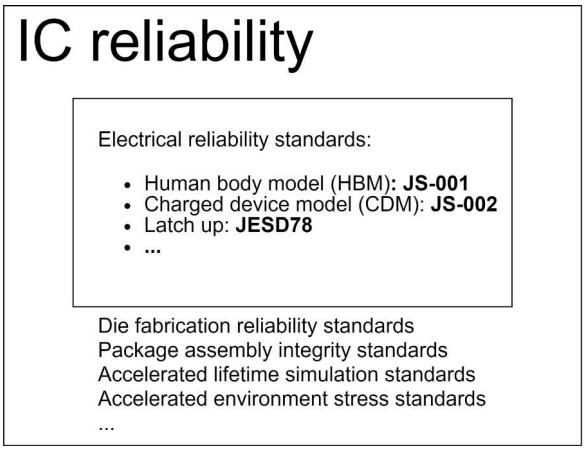


Figure 2-2. IC Reliability Standards

Some users confuse reliability with EMC, especially on ESD ratings. For IC electrical reliability, the related standards are JS-001 (HBM) and JS-002 (CBM). For EMC, the related standards are IEC 61000-4-2 and IEC 61967. These standards belong to two different standard categories. Table 2-3 gives an overview about the differences between EMC and IC electrical reliability.

Table 2-3. EMC and Electrical Reliability Comparison

Aspect	IC EMC Testing	IC Electrical Reliability Testing
Primary objective	Check the electromagnetic compatibility of a system under an electrical environment.	Verifies long-term stability and lifespan of ICs under electrical stress, preventing performance degradation or physical failure.
Noise injection	The IC-based system	IC
Test focus and example	System-level electromagnetic interactions. Example - ESD immunity: Validate system recovery from ESD events during usage.	IC endurance for electrical stress. Example - HBM, CBM: Tests IC tolerance to ESD events during manufacturing and assembly.
Optimization	Yes. Improved with HW/SW co-design.	No. Require IC redesign or silicon revisions.
SW Dependency	Yes. Firmware-dependent.	No
Failure impact	System-level malfunctions	Irreversible chip-level damage

In the IC design flow, the primary focus is on verifying reliability through methodologies that address physical degradation, manufacturing variability, and operational stresses. While EMC is not a direct consideration in traditional IC design frameworks, the scope is an IC-based system and not purely the IC. However, on-chip components like ESD structures can still provide foundational support for EMC improvements. For the related EMC improvement features on MSPM0, refer to Section 4.

For EMC testing, TI provides an EU Declaration of Conformity for every EVM with limited ICs on board, which shows these EVM boards can meet the EN61326-1:2013 requirement. Here is an example: LP-MSPM0G3507 EU RoHS Declaration of Conformity (DoC). For IC Reliability testing, TI provide qualifications for every orderable part number devices. Under Qualification Summary, users can find data for every typical IC part number as shown in Figure 2-3.

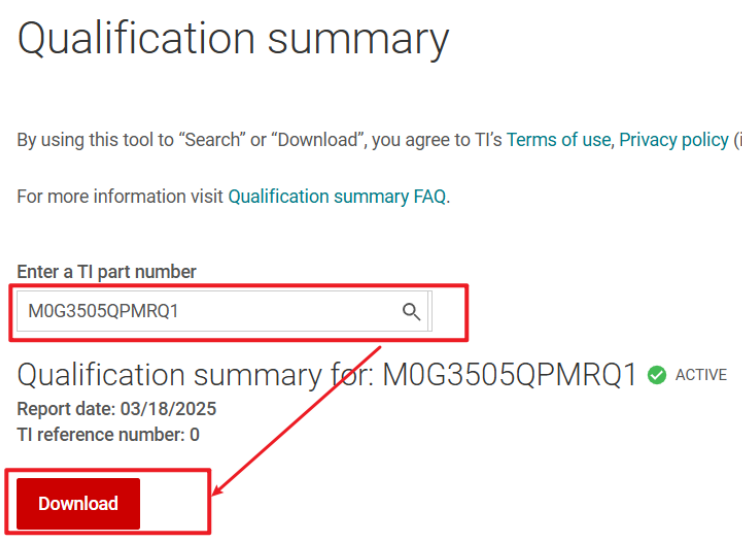


Figure 2-3. IC Reliability Entrance

For more about IC electrical reliability, refer to the Latch-Up, ESD, and Other Phenomena application report and Latch-Up white paper.

3 EMC Improvement Guidelines Summary

In this section, the guidelines are summarized for a quick check to help improve EMC in MSPM0-based systems at both software and hardware level. Detailed descriptions and analysis are described later in the document.

3.1 PCB Design Guidelines

PCB optimization is a key part for EMC improvement. The suggestions for optimization are presented as a check list format. All these suggestions are valid for both EMI and EMS.

Table 3-1. PCB Design Guidelines

Item	Suggestions Category	Suggestions
Schematic Design	MSPM0 minimum system	• Follow the guidance in the *Schematic* section of the data sheet to add resistors and capacitors on power supply, Vcore and Reset. An example is shown in Figure 3-1.
	EMC protection components	• Add EMC protection components shown in Table 3-2 at I/O ports and power inputs for more robust protection
PCB Layout	Power	• Place decoupling capacitors to be closed to the MCU and the 100pF capacitor is closest. • VDD line goes into the MCU by following this sequence: branch point->bypass capacitors-> MCU
	Ground	• Implement star grounding for mixed-signal systems • Use continuous ground planes (avoid splits under high-speed traces) • Add ground-filled zones in unused board areas • Add a solid GND under the MCU to reduce radiative noise • Place the GND pattern around the PCB perimeter and do not run the power supply (VDD) or signal lines • The power supply and GND pattern corners need to be 45 degrees or curved • Ground pins must be evenly distributed across all connectors
	Oscillator	• Reduce external oscillator loop to MCU GND pin • Surrounding oscillator wiring with a GND pattern • Separate the Oscillator GND and PCB GND to reduce radiative noise
	General signals	• Reduce trace lengths/loop areas (critical for clock and high-speed signals) • Signals must be curved at 45 degrees

Table 3-2 are the common used passive protection components to improve the EMC. If users want to have a deep understanding for the influence of passive protection components and PCB design on EMC improvement, then the Noise Suppression Basic Course provided by Murata is a good learning resource.

Table 3-2. Passive Protection Components

Category	MC Category	When to Use	Key Advantages	Critical Parameters	Design Tips
Resistor (Series)	EMS, EMI	High-frequency circuits requiring current control	Limits spikes, absorbs EMI, low inductance	Resistance value, parasitic inductance (<1 nH)	Use metal film; avoid carbon composition
Clamping Diodes	EMS	ESD-sensitive high-speed interfaces (USB, HDMI)	Ultra-fast response (<1 ns), low clamping voltage	Clamping voltage, peak pulse current, capacitance	Place near protected IC; pair with series resistors
Capacitor	EMS, EMI	Noise filtering or energy buffering	Ceramic (high-frequency), electrolytic (bulk)	SRF, voltage rating, capacitance	Match SRF to noise; avoid overlapping SRFs
TVS Diode	EMS	High-energy surges (lightning, inductive loads)	Ultra-fast clamping (<1 ps), handles 10kA surges	Reverse standoff voltage, clamping voltage	Standoff voltage > operating voltage by 20%

Table 3-2. Passive Protection Components (continued)

Category	MC Category	When to Use	Key Advantages	Critical Parameters	Design Tips
Ferrite Bead	EMI	GHz-range noise on power or data lines	Frequency-specific attenuation, no DC loss	Impedance at target frequency, DCR	Check impedance under DC bias
Common-Mode Choke	EMS/EMI	Common-mode noise in differential lines (CAN, USB)	Blocks noise without signal distortion	Impedance (for example, 600Ω at 100MHz), current rating	Balance winding inductance; minimize parasitics
EMI Filter (LC/Pi/T)	EMS/EMI	Broadband noise in power/signal lines	Multistage topology (Pi/T for high/low impedance)	Cutoff frequency, insertion loss	Pi-filter for power lines; T-filter for signals
Gas Discharge Tube	EMS	Extreme surges (telecom, lightning)	Handles 20kA surges, low capacitance, durable	Breakdown voltage, response time	Pair with TVS diodes for multi-stage protection

Here is an example of MSPM0 schematic design. For more description, refer to the data sheet of the specific MSPM0.

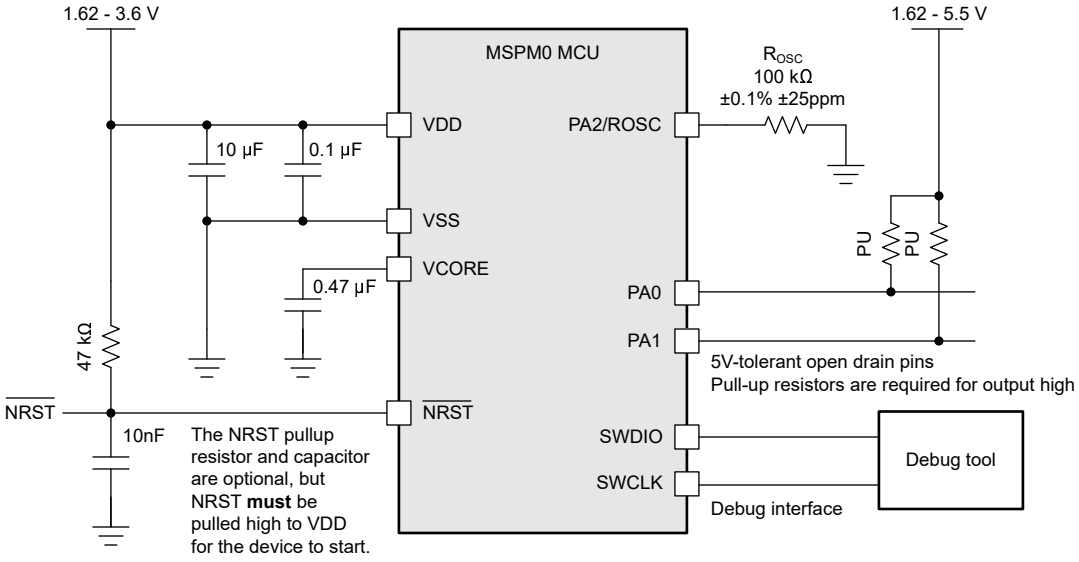


Figure 3-1. Basic Application Schematic of MSPM0G

3.2 Firmware Guidelines

Here are the MSPM0 related software configuration guidelines.

Table 3-3. MSPM0 Configuration Guidelines

Technique	EMS Coverage	Suggestions
BOR	EMS	Select higher BOR level if needed for data saving.
I/O Settings		Keep I/O setting to be default or output low. Need more protection for open-drain IOs if used.
Clock Source	EMI	Control the usage of clock.
Power Mode		Choose a valid power mode when running MCU.
Package		Choose the smaller and thinner package.

Here are the common firmware guidelines to improved EMS performance, which are also covered by applicable standards.

Table 3-4. Common Firmware Guidelines

Technique	Key Implementation	Applicable Standards	Standard Requirements
Watchdog and time control	Use independent or window watchdogs; refresh in main loop	IEC 60730, ISO 26262, IEC 61508	Mandate watchdog usage for fault detection and system recovery. ASIL D requires redundancy.
Securing unused memory	Fill unused Flash or ROM with valid instructions (for example, fault-handling routines)	IEC 60730, ISO 26262	Require program counter integrity checks and software robustness.
Input filtering and comparison	Multistage checks with averaging or debouncing	IEC 60730	Emphasize noise filtering for sensor reliability and input validation.
Unused interrupt management	Redirect unused vectors to a safe-state handler	IEC 61508, IEC 60730	Makes sure of controlled system states by handling all interrupt sources.
Critical and illegal byte handling	Avoid critical opcodes; replace uninitialized memory with non-executable patterns	ISO 26262, IEC 60730	Enforces code integrity to prevent latent faults.
ADC averaging	Multiple conversions with outlier rejection	IEC 60730, ISO 26262	Requires periodic ADC self-tests and redundancy for critical data.
Register reprogramming and checks	Periodic reconfiguration and verification of critical registers	IEC 61508, IEC 60730	Mandates cyclic self-tests for configuration integrity.
Redundant data storage	Dual storage with CRC, ECC; hash validation	IEC 60730, ISO 26262	Requires fault tolerance by redundancy; ASIL D enforces dual-channel redundancy.

4 EMC Improvement Features on MSPM0

The MSPM0 internal features are described in this section, which can be used to improve performance in EMC tests. If some features are not configured appropriately, then the features reduce the EMC performance.

4.1 Susceptibility Protection Features

In this section, the MSPM0 internal features protect MSPM0 against electromagnetic interference and are shown in Table 4-1.

Table 4-1. Susceptibility Protection Features Summary

Features	Adjustable	Suggestions
POR	No	N/A
BOR	Yes	Select higher BOR level if needed for data saving.
I/O ESD	No	N/A
I/O Settings	Yes	Keep I/O setting to be default or output low. Need more protection for Open-drain IOs if used.

4.1.1 POR and BOR

A power-on reset (POR) circuit indicates that the external supply has reached sufficient voltage to start the on-chip bandgap reference and BOR circuit. A user-programmable brownout reset (BOR) circuit makes sure that the external supply is maintained at a sufficient voltage to support correct operation of the device. In terms of EMS, the presence of the POR and BOR makes the MCU more robust. This also makes sure that if any outside disturbance affects the power supply, then the application can recover safely.

When the supply voltage (VDD) drops below POR-, the entire device state is cleared. Small variations in VDD that do not pass below the BOR0- threshold do not cause a BOR- violation, and the device continues to run. Behavior for BORx thresholds other than BOR0 (for example, BOR1-BOR3) is the same as shown for BOR0, except the BOR circuit is configured to generate an interrupt rather than immediately triggering a BOR reset.

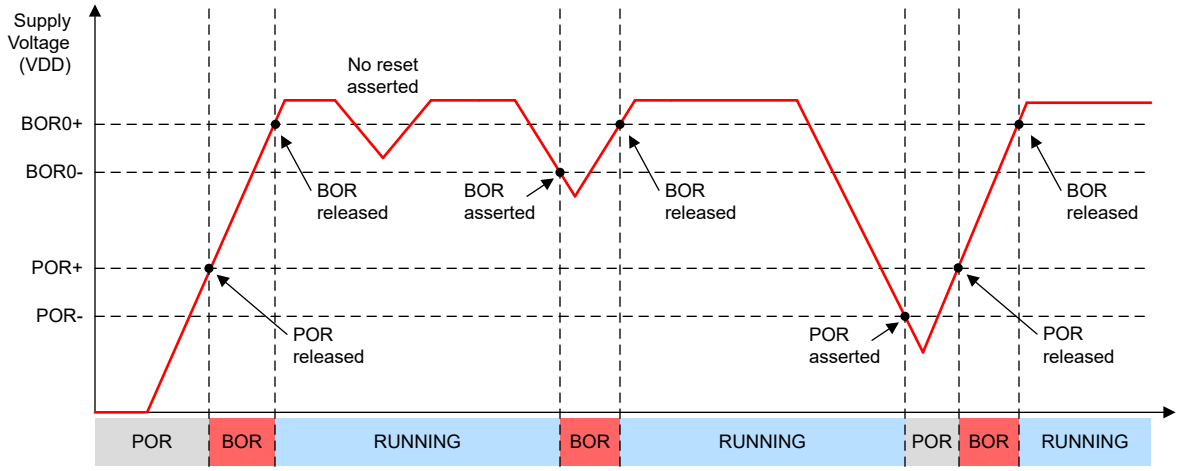
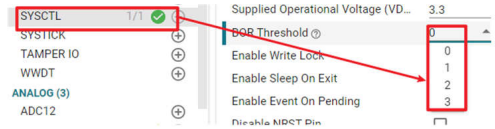


Figure 4-1. POR, BOR vs. Supply Voltage (VDD)

There are four selectable BOR threshold levels (BOR0-BOR3). During startup, the BOR threshold is always BOR0. After booting up, the software can reconfigure the BOR to use a higher threshold level (BOR1-BOR3). When the BOR threshold is BOR0, the violation generates a BOR reset. When the BOR threshold is reconfigured to BOR1, BOR2, or BOR3, the BOR generates a SYSCTL interrupt instead. This can be used to give the application an early warning that the supply has dropped below a certain level. Users can save the data and choose to reset the device in the interrupt service routine. To enable this functions, follow the instructions in Figure 4-2.



7.6.1 POR and BOR

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dVDD/dt	VDD (supply voltage) slew rate	Rising			1	V/us
		Falling (2)			0.01	
		Falling, STANDBY			0.1	V/ms
V_{POR+}	Power-on reset voltage level	Rising (1)	1.04	1.30	1.5	V
V_{POR-}		Falling (1)	0.99	1.25	1.48	V
$V_{HYS, POR}$	POR hysteresis		30	58	74	mV
$V_{BOR0+, COLD}$	Brown-out reset voltage level 0 (default level)	Cold start, rising (1)	1.48	1.54	1.61	V
V_{BOR0+}		Rising (1) (2)	1.56	1.58	1.61	
V_{BOR0-}		Falling (1) (2)	1.56	1.57	1.61	
$V_{BOR0, STBY}$		STANDBY mode (1)	1.54	1.56	1.60	
V_{BOR1+}	Brown-out-reset voltage level 1	Rising (1) (2)	2.15	2.17	2.23	V
V_{BOR1-}		Falling (1) (2)	2.12	2.14	2.19	
$V_{BOR1, STBY}$		STANDBY mode (1)	2.06	2.13	2.20	
V_{BOR2+}	Brown-out-reset voltage level 2	Rising (1) (2)	2.74	2.77	2.83	V
V_{BOR2-}		Falling (1) (2)	2.71	2.73	2.80	
$V_{BOR2, STBY}$		STANDBY mode (1)	2.68	2.71	2.82	
V_{BOR3+}	Brown-out-reset voltage level 3	Rising (1) (2)	2.88	2.96	3.04	V
V_{BOR3-}		Falling (1) (2)	2.85	2.93	3.01	
$V_{BOR3, STBY}$		STANDBY mode (1)	2.80	2.92	3.02	

Figure 4-2. BOR Level Setting in SysConfig

4.1.2 NMI and Hard Fault

MSPM0 has two interrupt mechanisms to handle unexpected behaviors from the MCUs, which are useful to analyze the root cause of EMS failure. The first is NMI, which is designed to handle critical system events that require immediate attention. The second is hard fault, which is a nonmaskable exception triggered by severe system errors that cannot be handled by other exception mechanisms.

When NMI happens, users can track the trigger sources by checking the NMI interrupt index and find a valid resolution. An example is shown in Table 4-2.

Table 4-2. MSPM0G Nonmaskable Interrupt Event

Index (IIDX)	Name	Description
0	NONE	No NMI pending.
1	BORLVL	Indicates that VDD has dropped below the specified VBOR- threshold.
2	WWDT0	A WWDT0 violation occurred.
3	WWDT1	A WWDT1 violation occurred.
4	LFCLKFAIL	Indicates that the LFXT or LFCLK_IN clock source is dead. This indication is useful for handling LFCLK errors when LFCLK is not sourcing MCLK but is sourcing a peripheral (for example, the RTC).
5	FLASHDED	Indicates that a flash memory double-bit uncorrectable error was detected.
6	SRAMDED	Indicates that an SRAM double-bit uncorrectable error was detected.

Hard fault serves as a last-resort handler for unrecoverable faults, such as memory access errors, unaligned memory operations, execution of undefined or illegal instructions and bus errors. Unlike higher-end Cortex®-M cores (for example, M3 and M4), the M0+ lacks configurable fault status registers (CFSR), making fault analysis more challenging and reliant on manual inspection. Hard fault generate a hard fault interrupt. Users can use this as an assert signal to adjust the system to pass the EMS test.

4.1.3 I/O ESD and Settings

Microcontroller input and output circuitry has been designed to take ESD and latch-up problems into account. However, self-protection is limited, especially when exposed to illegal voltages and high-current injections in EMS tests. TI strongly recommends to implement additional hardware protection if the features below do not work or the IO configuration cannot be satisfied.

Figure 4-3 shows the I/O structure in MSPM0. There are two possible routes to dissipate the energy from illegal voltages and high-current injections. The first and the default route is the two ESD diodes. The second is the P-channel Metal-Oxide-Semiconductor (PMOS) and N-channel Metal-Oxide-Semiconductor (NMOS) near the ESD diodes.

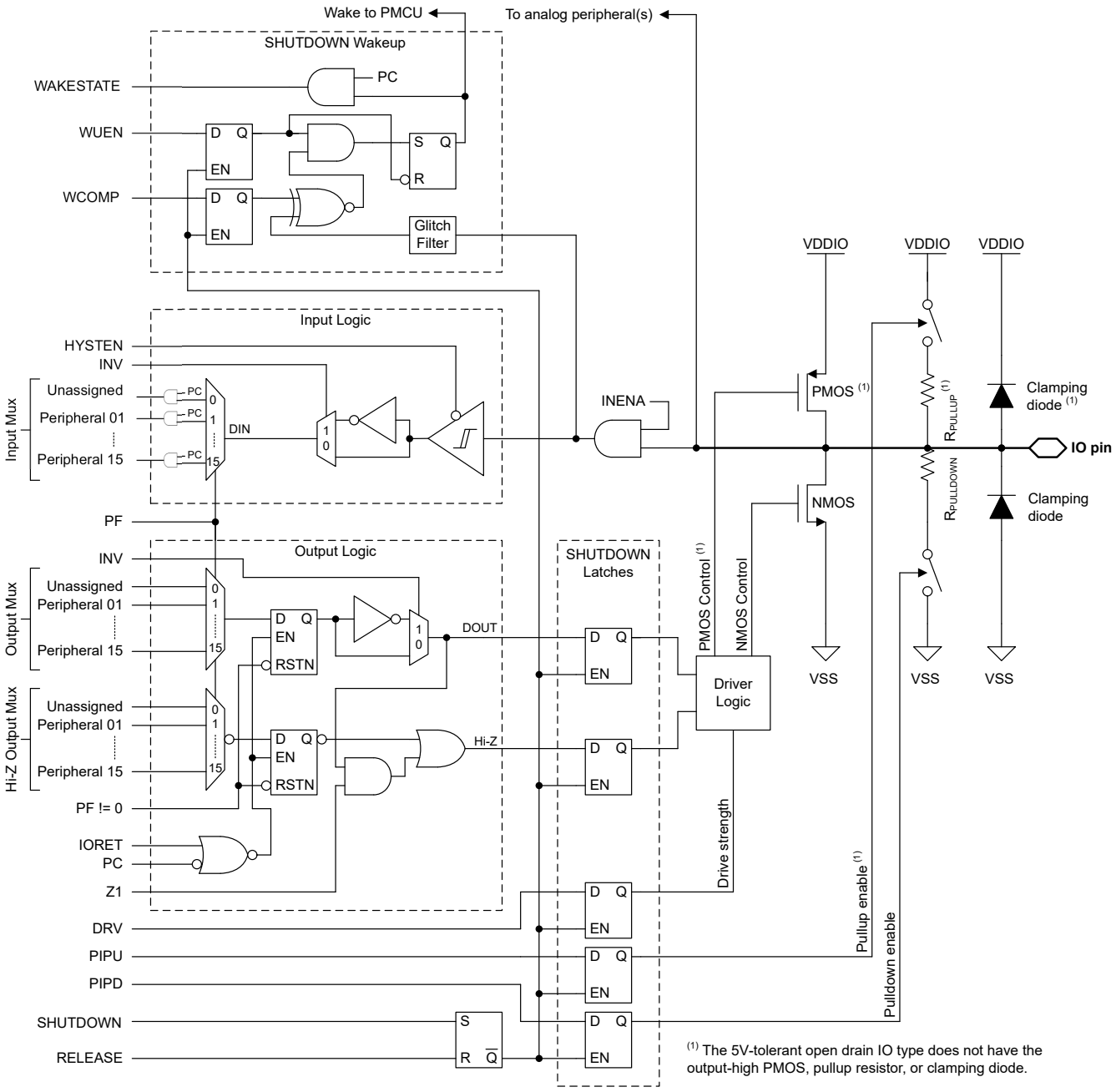


Figure 4-3. IO Structure of MSPM0G

The ESD diodes are triggered if a signal is applied that exceeds maximum input voltage range (-0.3V ≃ VCC+0.3V). The ESD diodes can withstand instantaneous ampere-level currents generated during typical electrostatic discharge events (per HBM or CDM standards). This ESD structure is also helpful to defend the illegal voltages and high-current injections in EMS tests.

For full featured IOs, with the output driver logic control, the PMOS and NMOS can also be a path to release the electrical stress. However, for open-drain IOs, the pull-up clamping diode and the PMOS do not exist yet. When the positive electrical stress happens, there is no route to release. The suggestions with different I/O settings are shown in Table 4-3.

Table 4-3. EMS Influence with IO Setting

IO Type	IO Setting	IO Status	Influence	EMS Protection
General IO	GPIO output and peripheral output (for example, UART)	Output mode	MOS and ESD structure release EMC noise	Best protection
	Default setting and analog functions	Hiz mode	ESD structure release EMC noise	Good protection
	GPIO Input And Peripheral Input (for example, UART)	Input mode	ESD structure release EMC noise Can introduce noise into MCU internal circuit	Good Protection
	GPIO and peripheral output low	Output mode	MOS and ESD structure release EMC noise	Best protection
Open-drain IO	GPIO and peripheral output high	Output mode	No route to dissipate the positive energy	Risk for positive noise and can need external protection
	Default setting and analog functions	Hiz mode	No route to dissipate the positive energy	Risk for positive noise and can need external protection
	GPIO input/ peripheral input (for example, UART)	Input mode	No route to dissipate the positive energy	Risk for positive noise and can need external protection

4.2 Emission Reduction Features

In this section, the MSPM0 internal features listed are shown in Table 4-4 to control the electromagnetic interference.

Table 4-4. Emission Reduction Features Summary

Features	Adjustable	Suggestions
Clock source	Yes	Control the usage of clock.
Power mode	Yes	Choose valid power mode for the related MCU operation requirement.
Package	Yes	Choose the smaller and thinner package.

4.2.1 Clock Source

Clock signals are a primary source of EMI in microcontroller systems. Clock noise propagates through the power supply introduced into the system, and also directly emits from the MCU package, contributing to radiated EMI.

For clock noise, clock frequency and current consumption are two critical factors to evaluate influence. The clock frequency determines the noise spectrum range. The current consumption serves as a reliable indicator of overall noise strength. High clock frequency and high current consumption typically increases clock noise.

The MSPM0 microcontroller series has flexible clock selection for users. Several internal and external oscillators are provided for generating low to high frequency clocks to be used by the system. A summary of the MSPM0 clock frequency and current consumptions is provided below for users.

Note

When enabling the external HFXT, remember to disable the SYSOSC.

Table 4-5. Clock Sources of MSPM0G

Clock Type	Clock Source	Clock Frequency Range	Test Conditions	Typical Current Consumption
SYSPLL	Internal	Up to 80MHz	fSYSPLLREF=32MHz, fVCO=160MHz	316uA
SYSOSC		≈4-32MHz	f_{SYSOSC}=4MHz	20uA
			f_{SYSOSC}=32MHz	80uA
			f_{SYSOSC}=32MHz, Enable ROSC	90uA
LFOSC		32.768kHz	LFOSC=32.768kHz	300nA
HFXT	External	≈4-48MHz	f_{HFXT}=4MHz, R_m=300Ω, C_L=12pF	75uA
			f_{HFXT}=48MHz, R_m=30Ω, C_L=12pF, C_m=6.26fF, L_m=1.76mH	600uA
LFXT		32.768kHz	XT1DRIVE=0, LOWCAP=1	200nA

Internal clock sources have shorter circuit trace and is shielded by MCU structure compared with external clock sources. External clock sources have lower clock jitter, which is also an important emission noise source. As a result, this is hard compare the emission noise between internal and external clock sources.

The general conclusion is that lower clock frequency generates lower emission noise. Internal and external clock selection are case-by-case.

4.2.2 Power Modes

The power modes of a microcontroller (MCU) significantly influence EMI due to variations in clock and peripherals activities. In MCU operation, high-frequency clock signals generate strong harmonics. Discrete spectral peaks from synchronized clock networks (for example, CPU, peripherals) amplify radiation.

The MSPM0 series provide five main operating modes (power modes) to allow for optimization of the device power consumption based on application requirements. The modes are: RUN, SLEEP, STOP, STANDBY, and SHUTDOWN. Different power modes represent the different available clock sources and different available peripherals. In every power mode, there are three mode policy options generated by limiting the max system clock frequency. An example of the supported functionality in each operating mode is shown in Table 4-6. For the full table and workable peripherals under different conditions, refer to the device-specific MSPM0 data sheet.

Table 4-6. Supported Functionality by Operating Mode of MSPM0G

Operating Mode		Run			Sleep			Stop			Standby	
		RUN0	RUN1	RUN2	SLEEP0	SLEEP1	SLEEP2	STOP0	STOP1	STOP2	STANDBY0	STANDBY1
Oscillators	SYSOSC	EN	EN	DIS	EN	EN	DIS	OPT	EN	DIS	DIS	DIS
	LFOSC or LFXT	EN (LFOSC or LFXT)										
	HFXT	OPT	DIS	DIS	OPT	DIS	DIS	DIS	DIS	DIS	DIS	DIS
	SYSPLL	OPT	NS	NS	OPT	NS	NS	NS	NS	NS	NS	NS
Clocks	CPUCLK	80MHz	32k Hz	32kHz	DIS							
	MCLK to PD1	80MHz	32k Hz	32kHz	80MHz	32kHz	32kHz	DIS				
	ULPCLK to PD0	40MHz	32k Hz	32kHz	40MHz	32kHz	32kHz	4MHz	4MHz	32kHz		DIS
	LFCLK	32kHz										DIS
Core functions	CPU	EN			DIS							
	DMA	OPT						DIS (triggers supported)				
	Flash	EN						DIS				
	SRAM	EN						DIS				

Analyze the working frequency and current consumption of digital peripherals and core function to evaluate the emission noise level. To find this information, refer to the device data sheet and the MSPM0G3507 Low Power Test and Guidance.

TI recommends to choose a valid power mode level and mode policy options for the related MCU operation requirement.

4.2.3 Package

In general, the EMI generated by IC packages exhibits an inverse relationship with package dimensions within the same family. Smaller packages tend to produce lower noise emissions due to reduced parasitic inductance and minimized current loop areas, which directly influence high-frequency radiation characteristics. This behavior stems from the decreased lead-frame length, optimized thermal resistance, and shorter interconnect paths inherent in miniaturized packaging technologies.

The following is a list of the package EMI contribution from the highest to the lowest:

- TSSOP (Thin Shrink Small Outline Package)
- SOT (Small Outline Transistor)
- VSSOP (Very Thin Shrink Small Outline Package)
- QFP (Quad Flat Package)
- QFN (Quad Flat No-lead
- BGA (Ball Grid Array)
- WCSP (Wafer-Level Chip Scale Package)

For best EMI performance, TI recommends users to choose the smaller and thinner package at the beginning.

5 Analysis for EMS Test

The model used to analyze EMS on MSPM0 perform improvements is shown in Figure 5-1. The EMS test first injects noise in the system, which can be a PCB or a product. Then, the noise is conducted into MSPM0 through IOs or power lines. To debug and improve focuses on the PCB optimization (propagation path) and MSPM0 configuration.

Figure 5-1. Noise Propagation Model for EMS

5.1 Root Cause Analysis

Considering the classification level in EMS standards, MSPM0 meets these different failure categories when doing EMC tests. Some failures can be acceptable, especially when system reset can be used in the test. More details are provided in the following sections.

Table 5-1. EMS Failure Category and Causes

Failure Category	Specific Manifestation	Root Cause	EMC Test Acceptability	Suggestions
Permanent damage	IO or peripheral functionality loss	Metallization defect	Unacceptable	Check whether beyond the Absolute Maximum ratings and Recommended Operating Conditions.
	Leakage current	Oxide breakdown		
	DVCC-GND short circuit	Burn-in Defect		
Recoverable malfunction	MCU reset abnormally	Trigger POR or BOOTRST	Conditionally acceptable	Check RSTCAUSE to know the reset cause.
	MCU function abnormally	Trigger hard fault or register and RAM changes		Check IPSR to know the interrupt source.

5.1.1 Permanent Damage

From the data sheet perspective, the abnormal MCU performance is due to going over the specifications. First, is the absolute maximum ratings. If users go over this specification, then permanent damage can happen. An example from MSPM0G3507 is shown in Table 5-2. In EMS tests, the input voltage for common tolerance pins are often not satisfied and causes damage to MSPM0 when the emission noise is injected into MSPM0 through IO pins. Another issue is the constant diode current specification. This is the current limit beyond which the ESD diode turns ON and starts clamping the voltage. If the ESD diode current is not allowed, like PA24 in MSPM0C1104, then this means the ESD diode starts clamping the voltage at the beginning.

Table 5-2. Absolute Maximum Ratings of MSPM0G

PARAMETER[1]		TEST CONDITIONS[2]	MIN	MAX	UNIT
VDD	Supply voltage	At VDD pin	–0.3	4.1	V
V_I	Input voltage	Applied to any 5V tolerant open-drain pins	–0.3	5.5	V
V_I	Input voltage	Applied to any common tolerance pins	–0.3	V_{DD} + 0.3 (4.1 MAX)	V
I_{VDD}	Current into VDD pin (source)	-40°C ≤ Tj ≤ 130°C		80	mA
	Current into VDD pin (source)	-40°C ≤ Tj ≤ 85°C		100	mA
I_{VSS}	Current out of VSS pin (sink)	-40°C ≤ Tj ≤ 130°C		80	mA
	Current out of VSS pin (sink)	-40°C ≤ Tj ≤ 85°C		100	mA

Table 5-2. Absolute Maximum Ratings of MSPM0G (continued)

PARAMETER[1]		TEST CONDITIONS[2]	MIN	MAX	UNIT
I_{IO}	Current of SDIO pin	Current sunk or sourced by SDIO pin		6	mA
	Current of HS_IO pin	Current sunk or sourced by HSIO pin		6	mA
	Current of HDIO pin	Current sunk or sourced by HDIO pin		20	mA
	Current of ODIO pin	Current sunk by ODIO pin		20	mA
I_D	Supported diode current	Diode current at any device pin		±2 [3]	mA

(1) Stresses beyond those listed under *Absolute Maximum Rating* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) Higher temperatures can be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.
(3) PA21 has an internal connection for testing purposes; there is no injection current allowed on this pin.

The second is the recommended operating conditions. If MSPM0 goes over this specification, then recoverable malfunction can happen. Therefore, the capacitor usages are suggested to follow the instructions.

Table 5-3. Recommended Operating Conditions

[3]		MIN	NOM	MAX	UNIT
VDD	Supply voltage	1.62		3.6	V
VCORE	Voltage on VCORE pin [2]		1.35		V
C_{VDD}	Capacitor connected between VDD and VSS [1]		10		uF
C_{VCORE}	Capacitor connected between VCORE and VSS [1] [2]		470		nF

(1) Connect C_{VDD} and C_{VCORE} between VDD and VSS and VCORE/VSS, respectively, as close to the device pins as possible. A low-ESR capacitor with at least the specified value and tolerance of ±20% or better is required for C_{VDD} and C_{VCORE}.
(2) The VCORE pin must only be connected to C_{VCORE}. Do not supply any voltage or apply any external load to the VCORE pin.
(3) Wait states are managed automatically by the system controller (SYSCTL) and do not need to be configured by application software unless MCLK is sourced from a high speed clock source (HSCLK sourced from HFCLK or SYSPLL)

5.1.2 Recoverable Malfunction

For the recoverable malfunction, MSPM0 devices include several diagnostic mechanisms to detect errors at runtime. Table 5-4 lists error sources and the corresponding handling mechanism. This can be used to give additional analysis information in EMS failure analysis.

Table 5-4. Error Sources and Handling Mechanisms

Error Source	Error	Handling Mechanism
Flash (if device has ECC)	Non-correctable ECC error (if device has ECC)	• For a CPU or DMA request, a FLASHDED nonmaskable interrupt is generated to the processor or a SYSRST is generated depending on configuration of the FLASHECCRSTDIS bit • The FLASHDED sticky bit is set in the SYSSTATUS register in SYSCTL
	Correctable ECC error (if device has ECC)	• A FLASHSEC interrupt is also generated in SYSCTL • The FLASHSEC sticky bit is set in the SYSSTATUS register in SYSCTL

Table 5-4. Error Sources and Handling Mechanisms (continued)

Error Source	Error	Handling Mechanism
SRAM	Non-correctable ECC error (if device has ECC)	• An SRAMDED nonmaskable interrupt is generated to the processor
	Correctable ECC error (if device has ECC)	• A SYSCTL SRAMSED interrupt is generated to the processor
	Parity error (if device has parity)	• Nonmaskable interrupt is generated to the processor if the request was from the CPU • DMA data error interrupt is generated if the request was from the DMA
	Address error on CPU access	• A hard fault is generated in the CPU
	Address error on DMA access	• A DMA address error interrupt is generated in the DMA controller
	ECC error on CAN SRAM (if device has CAN-FD)	• An interrupt is generated in the CAN-FD peripheral
SHUTDNSTORExMemory (if present)	Parity error	• A POR is generated
CKM	MCLK failure	• A BOOTRST is generated
	LFCLK failure (if present)	• A BOOTRST is generated if LFCLK is sourcing MCLK • An LFCLKFAIL nonmaskable interrupt is generated in the SYSCTL NMI registers.
CPUSS (if device has MPU)	Memory protection unit violation	• A hard fault is generated in the CPU
WWDT	WWDT0 violation	• A BOOTRST is generated or a nonmaskable interrupt is generated in the SYSCTL NMI registers depending on configuration of the WWDTLP0RSTDIS bit
	WWDT1 violation (if present)	• A BOOTRST is generated or a nonmaskable interrupt is generated in the SYSCTL NMI registers depending on configuration of the WWDTLP1RSTDIS bit
PMU	Trim parity error	• A POR is generated
	POR0- supply error	• A POR is generated
	BOR0- supply error	• A BOR is generated
	BOR1/2/3- supply error	• A BORLVL nonmaskable interrupt is generated in the SYSCTL NMI registers
CPUSS	Memory protection unit violation (if present)	• A hard fault is generated in the CPU

If MCU resets abnormally, then users can get the reset source information from RSTCAUSE register using DL_SYSCTL_getResetCause() software function. Then search the RSTCAUSE table to know the reset source, as shown in Table 5-5.

Table 5-5. RSTCAUSE Field Descriptions of MSPM0G

Bit	Field	Type	Reset	Description
31-5	RESERVED	R	0h	
4-0	ID	RC	0h	ID is a read-to-clear field which indicates the lowest level reset cause since the last read. 0h = No reset since last read 1h = POR- violation, SHUTDNSTOREx or PMU trim parity fault 2h = NRST triggered POR (>1s hold) 3h = Software triggered POR 4h = BOR0- violation 5h = SHUTDOWN mode exit 8h = Non-PMU trim parity fault 9h = Fatal clock failure Ah = Software triggered BOOTRST Ch = NRST triggered BOOTRST (<1s hold) 10h = BSL exit 11h = BSL entry 12h = WWDT0 violation 13h = WWDT1 violation 14h = Flash uncorrectable ECC error 15h = CPULOCK violation 1Ah = Debug triggered SYSRST 1Bh = Software triggered SYSRST 1Ch = Debug triggered CPURST 1Dh = Software triggered CPURST

If reset does not happen and MCU only functions abnormally, then the MCU is trapped in default handler. To know the exact interrupt source, users can read IPSR register, using __get_IPSR() software function. An example is shown in Table 5-6. For the detailed interrupt source, refer to the *MSPM0 Platform Processor Interrupt and Exception Table* section in the device-specific TRM.

Table 5-6. MSPM0 Platform Processor Interrupt and Exception

Exception Number	NVIC Number	Priority Group	Exception or Interrupt	Vector Table Address	Vector Description
-	-	-	-	0x0000.0000	Stack pointer
1	-	-3	Reset	0x0000.0004	Reset vector
2	-	-2	NMI	0x0000.0008	NMI handler
3	-	-1	Hard fault	0x0000.000C	Hard fault handler

5.2 Debug Flow

The key idea for the EMS debug flow is to classify the EMS failure into a typical root cause category in Table 5-1. Then, use some assert signals to find the propagation path. Lastly, use software and hardware change to help overcome the electrical stress.

1. Make sure to consistently recreate the EMS test failure and check whether this is a permanent damage issue or a recoverable malfunction issue. If there is a permanent damage issue, then go to step 4.
2. Check whether an oscilloscope or a logic analyzer can be used without being affected by test noise. If this is possible, then check the IO signals, power, reset pin for specifications that are over the conditions. This can help to find the propagation path directly.
3. Disable BSL in NONMAIN configuration and then check if the MCU is in a reset state or has entered the default handler with an assert signal. If MCU enters the default handler and reset is acceptable, please add a software reset in the default handler. Here are some methods to check the MCU states.
   - MCU is in a reset state:
     a. Output clock signal to see whether the signal stops for a while.
     b. Add a GPIO toggle at the top of main function to see if the GPIO toggles.
     c. Connect the device without re-programming or resetting, and then check RSTSOURCE register to know the reset source.
   - MCU has entered the default handler, triggered by NMI or Hard Fault:
     a. Output clock signal to see whether the signal does not stop.

   b. Add a GPIO toggle in the default handler to see if GPIO toggles.
   c. Connect the device without programming or a reset to check where the code is running in default handler.

4. Check whether IO status change can fix the issue.
   - Only enable a GPIO to toggle and keep other GPIOs in default state (Hiz mode). This GPIO is used to show whether the device still reset or enter the default handler. If the EMS failure disappears, then enable functions one by one to see which IO is the propagation path.
5. If the EMS failure still happens, then do temporary hardware modifications. First, check whether the noise is from power line.
   - Add strong protections to MCU power using the passive protection components as shown in Table 3-2. If the problem is solved, then enable functions one by one to see whether the problem is solved.
6. If the EMS failure still happens, then check whether the noise is from IO connection.
   - Physically isolate MCU IOs by removing the resistors or NPNs one by one to find which IO is the propagation path. Then add passive protection components shown in Table 3-2 to check whether the problem is solved.

6 Analysis for EMI Test

Here is the model to analyze and improve EMI on MSPM0. The emission is generated by the interaction between MSPM0 and the PCB or the system. What users can debug and improve focuses on analyzing the contribution of different MSPM0 operation settings and doing optimization on the MSPM0 configuration or the PCB.

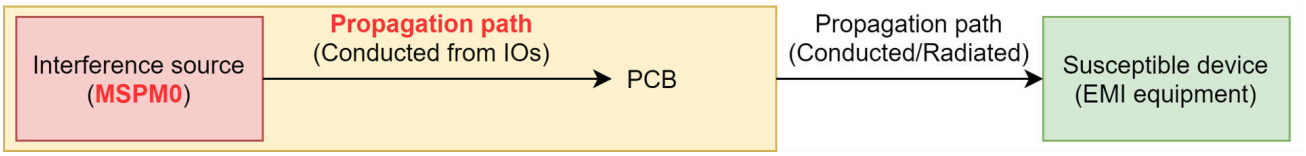


Figure 6-1. Noise Propagation Model for EMI

6.1 Root Cause Analysis

Table 6-1 summarizes EMI failures and the root causes from the MSPM0 perspective. A more detailed explanation is in the following sections.

Table 6-1. EMI Failure Category and Causes

Noise Source	Causes	Suggestions
Power line	• Inadequate decoupling capacitors near MSPM0 power pins and improper PCB layout • Improper grounding (for example, mixed analog or digital grounds; multipoint grounding; missing ground planes) • Large current loop areas in power / signal paths	Optimize PCB layout and add capacitors to cover the concerned frequency range
External Vcore	• Inadequate decoupling capacitors near Vcore pins and improper PCB layout	Optimize PCB layout and add capacitors to cover the concerned frequency range
IO	• Uncontrolled slew rate or drive strength in GPIOs • High transient currents during signal transitions	Use RC filter to reduce transient currents and high frequency voltage component.

6.1.1 Power Line

For digital circuits, there are three major noise sources as shown in Figure 6-2, which are the cause of EMI issues. The first is the voltage signal. As digital circuits process information by switching between high and low voltage states on signal lines, this generates signal transitions that decompose into discrete harmonic components across a broad frequency spectrum. The second is the signal current. During switching events, transient currents flow through signal lines as gate capacitance charges and discharges. The third is the short-circuit current. In CMOS digital ICs, a short-circuit current spike occurs when both PMOS and NMOS transistors briefly conduct simultaneously during logic transitions. This transient current flows directly between power and ground.

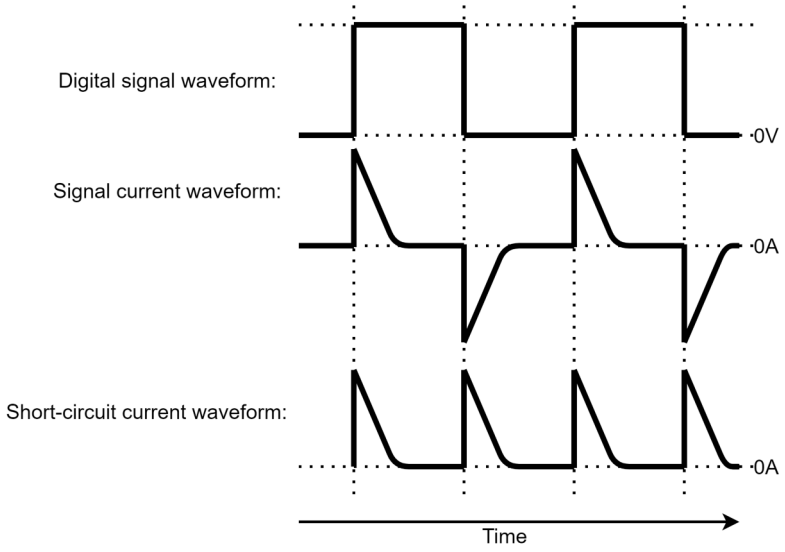


Figure 6-2. Noise Sources in Digital Circuits

For the signal line noise caused by the voltage signal noise and single current noise, use an RC filter to improve the EMI. For the power line noise caused by short-circuit current, use decoupling capacitors to help improve the EMI.

The issues to highlight are the decoupling capacitors near MSPM0 power pins and Vcore pins. For the decoupling capacitors, TI recommends a combination of a 10µF and a 0.1µF low-ESR ceramic decoupling capacitor to the VDD and VSS pins. Higher-value capacitors can be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that the capacitors decouple (within a few millimeters). Table 6-2 shows the impacts of improper PCB design of the power supply part, and all increase emission noise.

Table 6-2. Impacts of Improper PCB Design

Improper Design	Influence
Large-ESR capacitor	Large voltage drop with transient current
Long distance between capacitors and MSPM0	Large loop area of the high-frequency current from MSPM0
10uF capacitors are closer than 0.1uF to MSPM0	Larger loop area of the high-frequency current than low-frequency current

The impedance of a capacitor is different across the frequency as shown in Figure 6-3. Normally, 1uF capacitors can cover approximately 3-30MHz. The 0.1uF capacitors can cover approximately 6-60MHz. The 0.01uF capacitors can cover approximately 30-300MHz. The 1nF capacitors can cover approximately 60-600MHz. Users can select more capacitors with different capacitance to cover the target frequency range. Capacitors with a smaller capacitance value are more effective at a higher frequency and are more susceptible to the parasitic inductance. Therefore, minimize the loop area of the high-frequency current by placing the capacitors closer to the MCU.

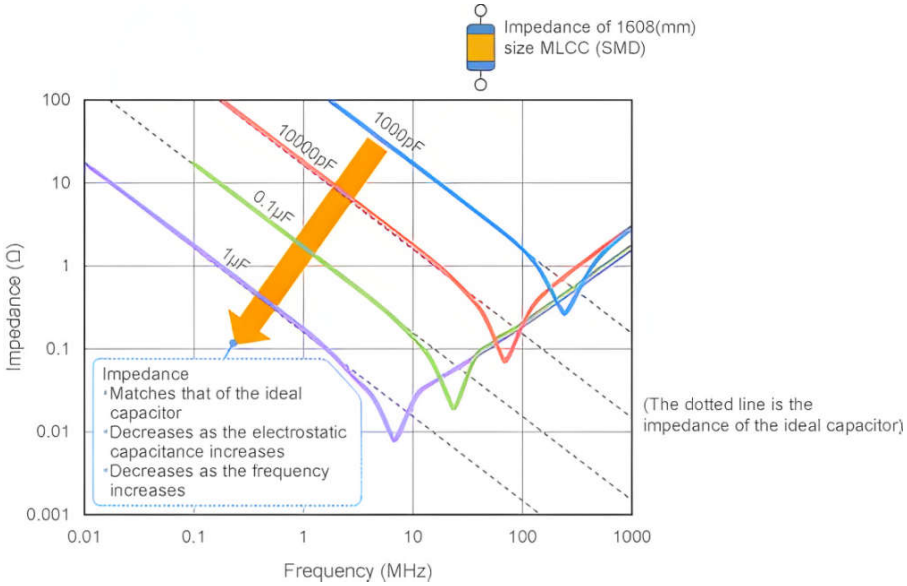


Figure 6-3. Capacitors Impedance Performance

6.1.2 External Vcore

The power management unit (PMU) of MSPM0 uses an on-chip, configurable, low-dropout LDO to generate a 1.35V supply rail to power the device core. In general, the core regulator output (VCORE) supplies power to the core logic, which includes the CPU, digital peripherals and the device memory. For some MSPM0 devices, the internal LDO requires an external capacitor (C_{VCORE}) which is connected between the device VCORE pin and VSS (ground). For some MSPM0 devices, the coupling capacitor is integrated into the IC.

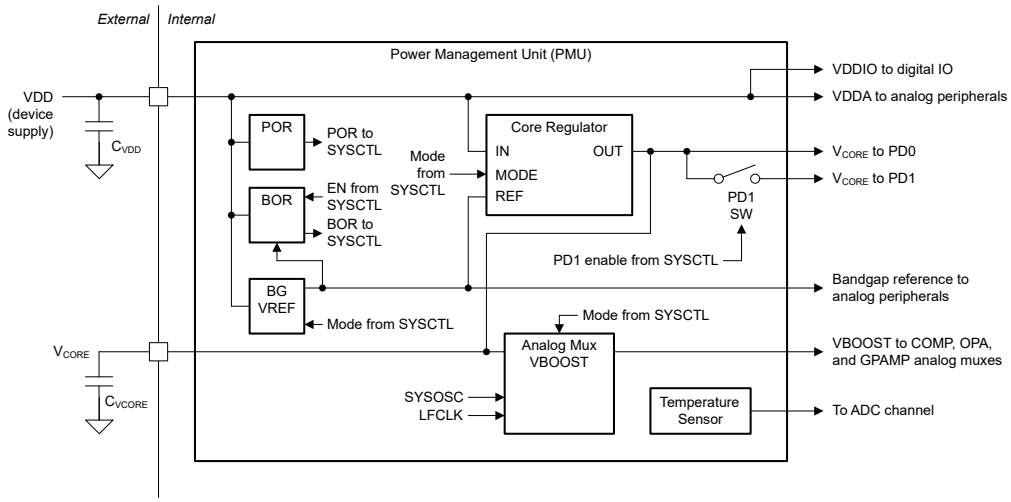


Figure 6-4. Power Module of MSPM0G

The LDO cannot respond instantaneously to transient conditions. A delay occurs before the current through the pass element adjusts to the increased load. During this delay time, the output capacitor is left to supply the entire transient current. Because of this, the amount of output capacitance and the associated parasitic elements greatly impact the transient response of the LDO circuit. Compared with the internal capacitor usage, the external capacitor usage is more sensitive to the parasitic inductance and causes bad performance on the load-transient response for the power noise generated by the high speed digital circuits. A conducted noise example on Vcore is shown in Figure 6-5. In this example, C_{VCORE} is 0.47uF and MSPM0 runs with one NOP.

Figure 6-5. Conducted Noise at Vcore on MSPM0L

To improve the EMI performance of the MCU, a low-ESR capacitor is suggested to reduce the parasitic inductance influence. Besides the suggested 0.47uF capacitors, users can add more capacitors with different capacitance to cover the target frequency range. For more information about output capacitor influence on LDO EMI performance, refer to the EMC Measures for LDOs and Understanding the load-transient response of LDOs analog design journal.

6.2 Debug Flow

The key for the EMI debug flow is to classify the EMI failure into a typical noise source category as shown in Table 6-1. Then, try to use software and hardware change to reduce the emission noise.

1. Check the contribution from IO functions.
   - Comment functions related to IO toggling one by one and record the noise level reduction.
2. Check the contribution from Clock, CPU, Memory access.
   - Try different power modes and different power mode policy options (RUN0, RUN1, RUN2, STANDBY0) and record the noise level reduction.
3. Calculate the noise contribution from IO functions, Clock, CPU and Memory access.
4. Control the usage of MSPM0 functions. If the problem is still not solved, then add passive protection components as shown in Table 3-2 or optimize the PCB layout described in Table 3-1.

7 Summary

This document provides a comprehensive introduction and description of protection of EMC-based on MSPM0. Users can receive a comprehensive introduction to enhancing EMC when developing systems based on MSPM0. At the same time, during EMC testing, this document also provides detailed and comprehensive debugging ideas and explanations of common problems.

8 References

- Texas Instruments, Latch-Up, white paper
- Texas Instruments, Latch-Up, ESD, and Other Phenomena, application note
- Texas Instruments, ESD Diode Current Specification, application note
- Texas Instruments, MSP430 System-Level ESD Considerations, application note
- Texas Instruments, MSPM0G3507 Low Power Test and Guidance, application note
- Texas Instruments, EMC Measures for LDOs, application note
- Texas Instruments, MSPM0 G-Series 80MHz Microcontrollers, technical reference manual
- Texas Instruments, MSPM0G350x Mixed-Signal Microcontrollers With CAN-FD Interface, data sheet
- Murata, Noise Suppression Basic Course, online trainning
- ROHM, Understanding the load-transient response of LDOs analog design journal, application note.

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