Application Note

Advanced Layout Optimization Guidelines for High-Speed FPD-Link™ SerDes Coax Channel

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ABSTRACT

In automotive applications, high-speed signal interfaces such as video serializer/deserializer (SerDes), Multi-Gigabit Ethernet, USB3.x, and DisplayPort (DP) are increasingly deployed to meet growing bandwidth demand. The single-link data rate of these interfaces can reach multi-gigabit or even tens of gigabits per second.

Signal integrity (SI) is critical for reliable high-speed signal transmission, as waveform distortions caused by reflections, impedance mismatches, crosstalk, or signal attenuation can lead to data corruption and communication failures. To provide robustness, these interfaces define stringent S-parameter requirements, including return loss (S11) and insertion loss (S21), across the entire high-speed channel to maintain maximum performance.

For instance, TI's latest FPD-Link SerDes can now support data rates up to 13.5Gbps over a single coax cable to support 4K+ resolution display. The total FPD-Link™ interface channel comprises a printed circuit board (PCB), passive components, connectors, and cables. Among these, PCB layout design plays a pivotal role in signal integrity preservation. Key design considerations include controlled trace impedance, strategic component placement and via placement, anti-pad sizing, parasitic capacitance mitigation, and so forth.

This application note takes the FPD-Link coax channel design as an example, focusing on PCB channel design requirements and actionable layout design guidelines to optimize PCB S-parameters.

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Trademarks

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1 S-Parameter Definition

S-parameters, or scattering parameters are a set of values that completely describe the electrical behavior of a network at a given frequency. S-parameters quantify the ratio of the power wave reflected or transmitted from a port to the power wave incident upon another port. S-parameters are widely used to characterize RF and high-speed digital components and systems. Figure 1-1 illustrates the simplified S-parameters model including S11 and S21.

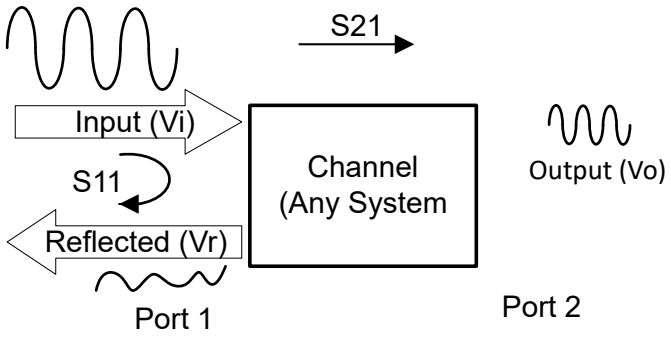


Figure 1-1. S-Parameter Model - S11 And S21

1.1 Insertion Loss (S21)

The following list describes *insertion loss* (S21).

- Quantifies the signal power attenuation caused by components (for example, cables, connectors, and PCB traces) inserted into a transmission path.
- Typically expressed in decibels (dB).

$$S21\left(dB\right) = 20 \times \log_{10}\left(\frac{V_{output}}{V_{input}}\right) \quad (1)$$

- Higher absolute values indicate greater signal degradation, which can reduce data throughput and cause communication errors.
- Primary contributors: transmission line resistance, PCB dielectric loss, impedance mismatches, and component absorption or component scattering.

1.2 Return Loss (S11)

The following list describes *return loss* (S11).

- Measures reflected power due to impedance mismatches in the transmission path.
- Expressed in decibels (dB).

$$S11\left(dB\right) = 20 \times \log_{10}\left(\frac{V_{reflected}}{V_{input}}\right) \quad (2)$$

- Higher absolute values indicate better impedance matching and lower reflected power.

Note

The primary focus in this application note is maximizing trace impedance to enhance return loss (S11) performance. Insertion loss (S21) can be minimized through trace length reduction or adoption of low-loss dielectric materials. In contrast, S11 is more challenging to manage as S11 requires stringent impedance control across the entire signal path. Impedance control is the key of a successful design as this control not only directly enhances S11, but also indirectly optimizes S21 by mitigating reflections and energy dissipation.

2 High-Speed Signal Design Example Of FPD-Link™ Serializer Body

2.1 Design Example Overview

This section presents a design example based on the FPD-Link serializer. The serializer is used to transmit video data to remote display over a single coax channel, the data rate runs up to 13.5Gbps to support 4K display. All the subsequent analysis and simulations are based on this example. Figure 2-1 depicts the total FPD-Link channel structure on the serializer PCB. Figure 2-2 is the corresponding PCB 3D model of the FPD-Link serializer channel.

Key design specifications:

- PCB stackup: this example is based on a six-layer stackup with standard FR-4 material (dielectric constant Dk = 4.3, dissipation factor Df = 0.02).
- Key components: the total FPD-Link serializer channel includes an IC pin, single-ended transmission line, ESD diode, AC coupling capacitor, signal via, and through-hole coax connector.
- Critical frequency points: FPD-Link line rate runs up to 10.8 and 13.5GHz to support 4K+ resolution display, the frequencies of interest are half of the line rate, that is, 5.4GHz and 6.75GHz.

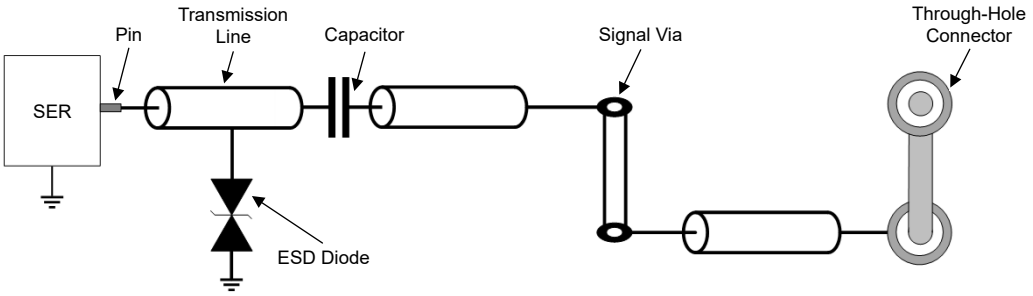


Figure 2-1. FPD-Link™ Channel Structure on Serializer PCB

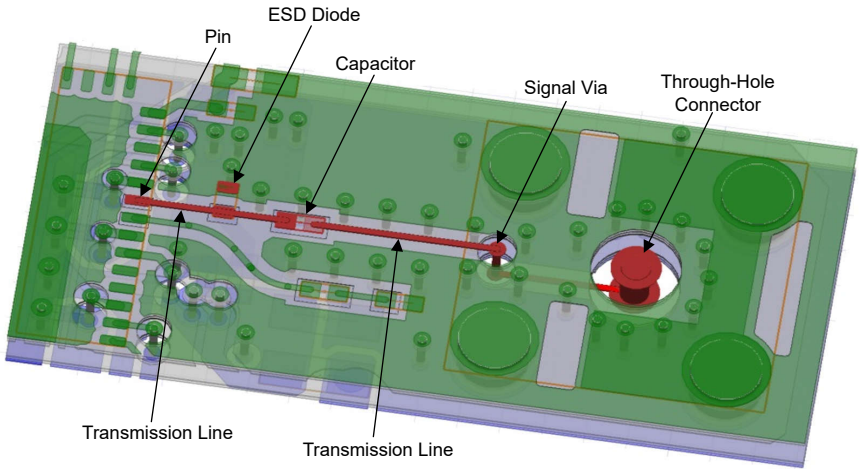


Figure 2-2. PCB 3D Model of FPD-Link™ Serializer Channel

2.2 Key Points in High-Speed FPD-Link Layout Design

In high-speed signal design, proper PCB layout is required to achieve maximum signal integrity. General guidelines focus on managing signal reflection, attenuation, and crosstalk.

- Reflection control:
  - Caused by impedance discontinuities (for example, vias, connectors, trace width change)
  - Signal reflections degrade return loss (S11)
  - Need to maintain a consistent 50Ω single-ended impedance across the entire signal path
- Attenuation control:
  - Caused by conductor resistance and dielectric losses in PCB substrates
  - Attenuation reduces signal amplitude and edge sharpness, which degrades insertion loss (S21)
  - Use low-loss dielectric PCB materials or reduce trace length to minimize attenuation
- Crosstalk control:
  - Caused by electromagnetic coupling between adjacent signal traces
  - Crosstalk induces noises, timing jitter, and logic errors
  - Increase spacing between high-speed traces, and add ground shielding to minimize crosstalk

Since reflection control is the most challenging aspect, critical factors and design variables are analyzed and optimized to achieve better reflection through simulation in this application note. This helps the designer address return loss degradation caused by capacitor landing pad, ESD diode parasitic capacitance, signal via, and through-hole connector. Optimization key points are highlighted in the following list:

- Transmission line impedance control:
  - Maintain 50Ω single-ended trace routing with impedance control of ±5%
  - Make sure the reference plane is complete above or below the high-speed trace
  - Route the high-speed trace as a microstrip on the top layer or bottom layer to avoid any stubs
- Impedance control at the component level in the following list:
  - AC coupling capacitor landing pad
  - ESD diode landing pad and inherent parasitic capacitance
  - Through-hole connector footprint
- Impedance control at the through-hole signal vias:
  - Minimize signal via numbers, eliminate via stubs
  - Optimize signal via anti-pad and add ground transition vias to minimize impedance discontinuity

In summary, the key principles for high-speed SerDes routing is *well-controlled impedance*. This requires maintaining a uniform 50Ω impedance profile across the entire signal path, even when traces change layers through vias or pass through ESD diodes or capacitors.

The following section analyzes all these optimization key points in detail. Design models, simulation results of return loss and Time-Domain Reflectometry (TDR) impedance, actionable layout design recommendations are provided for optimizing PCB S-parameters.

3 Factors Impacting Return Loss and Optimization Guidelines

This section elaborates on the optimization key points in high-speed FPD-Link layout design, providing corresponding optimization recommendations for each point based on design models and simulation results.

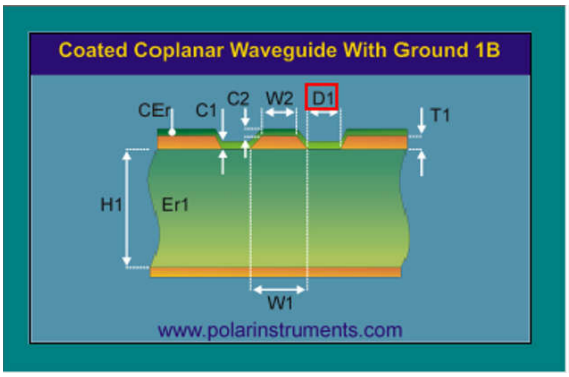
3.1 Transmission Line Impedance Impact

Figure 3-1 shows the transmission line model used in the design example. The impedance of a PCB transmission line is determined by the interplay of trace width, trace thickness, substrate height, trace-to-copper clearance, PCB dielectric constant (Dk), and coating above the trace.

- Trace width: A wider trace increases the capacitive coupling between the signal trace and the reference plane, which lowers the impedance.
- Trace thickness: A thicker trace increases capacitive coupling to the reference plane, this lowers the impedance slightly.
- Substrate height: A thinner dielectric layer (smaller distance between the signal trace and reference plane) increases the capacitive coupling, this lowers the impedance.
- Trace-to-copper clearance (ground strip separation): Narrower clearance from the trace to adjacent copper increases fringe capacitance coupling to neighboring copper. This reduces impedance by increasing parasitic capacitance.
- PCB dielectric constant (Dk): A higher dielectric constant increases the capacitance between the trace and reference plane, thereby lowering the impedance.
- Solder mask and solder coating: The solder mask and solder coating adds a dielectric layer over the signal trace. This increases the effective dielectric constant (Dk) near the trace and lowers the impedance.

To main a consistent 50Ω transmission line impedance:

- Make sure of a uniform trace width and spacing throughout the signal path.
- In PCB manufacturing, etched copper traces have distortions and irregular rectangular cross-sections due to the inherent etching factor. The resulting profile is trapezoidal. In this design example, the upper trace width is 5.3mil, while the lower width is 6.3mil. Align these geometric dimensions with the process capability of the PCB fabricator.



				Tolerance	Minimum	Maximum	
Substrate 1 Height	H1	3.8000	+/-	0.0000	3.8000	3.8000	Calculate
Substrate 1 Dielectric	Er1	4.0000	+/-	0.0000	4.0000	4.0000	Calculate
Lower Trace Width	W1	6.3000	+/-	0.0000	6.3000	6.3000	
Upper Trace Width	W2	5.3000	+/-	0.0000	5.3000	5.3000	Calculate
Ground Strip Separation	D1	6.0000	+/-	0.0000	6.0000	6.0000	Calculate
Trace Thickness	T1	1.4000	+/-	0.0000	1.4000	1.4000	Calculate
Coating Above Substrate	C1	1.0000	+/-	0.0000	1.0000	1.0000	
Coating Above Trace	C2	1.0000	+/-	0.0000	1.0000	1.0000	
Coating Dielectric	CEr	3.5000	+/-	0.0000	3.5000	3.5000	
Impedance	Zo	48.04			48.04	48.04	Calculate

Figure 3-1. Transmission Line Model For Impedance Calculation

Key recommendations for transmission line impedance:

- Use an impedance calculator to determine maximum impedance parameters
- Close trace-to-copper spacing can reduce the impedance by 2Ω–3Ω, consider the effects of the spacing
- Solder mask on the trace can reduce the impedance by 2Ω to 3Ω, consider the effects of the solder mask
- Maintain impedance control of fabricated the PCB within 50Ω ±5%

3.2 AC Coupling Capacitor Landing Pad Impact And Optimization

A capacitor landing pad can significantly reduce the trace impedance. When trace passes through the AC coupling capacitor, typically the surface-mount pad size is wider than the signal trace. Abrupt changes in trace geometry introduce additional parasitic capacitance between the pad and adjacent reference plane, degrading impedance continuity.

3.2.1 Mitigation Strategy: Anti-Pad Implementation

To counteract pad-introduced impedance deviation, create a ground cutout (anti-pad) under the landing pads on the adjacent reference layer (for example, layer 2). This forces the pad to reference a more distant layer (for example, layer 3), effectively increases the dielectric thickness and raising impedance to offset the capacitive effect of the bigger pad.

Anti-pad size requires careful consideration. Oversized or undersized anti-pad can disrupt the electromagnetic fields and affect signal coupling between the trace and reference plane, which in turn affects the signal impedance.

The best anti-pad size depends on various factors such as the dielectric thickness, trace width, and pad dimensions. Use simulation tools (for example, Ansys® HFSS) to analyze pad effects and determine the best possible anti-pad size.

3.2.2 Simulation Results With Ansys® HFSS

The following simulation results evaluate the impact of anti-pad size on return loss and impedance continuity in the design example:

- Figure 3-2: Simulation model for landing pad and anti-pad structure.
- Figure 3-3: Return loss (S11) simulation result with different anti-pad size.
- Figure 3-4: TDR impedance simulation result with different anti-pad size.

Key observations:

- Without anti-pad (red curve), the impedance deviation is maximized and the return loss (S11) is significantly degraded.
- Different anti-pad size results in different impedance change and return loss (S11) performance.
- In this design example, an anti-pad size 1.4 × wider than the landing pad achieves the best return loss (S11) performance.

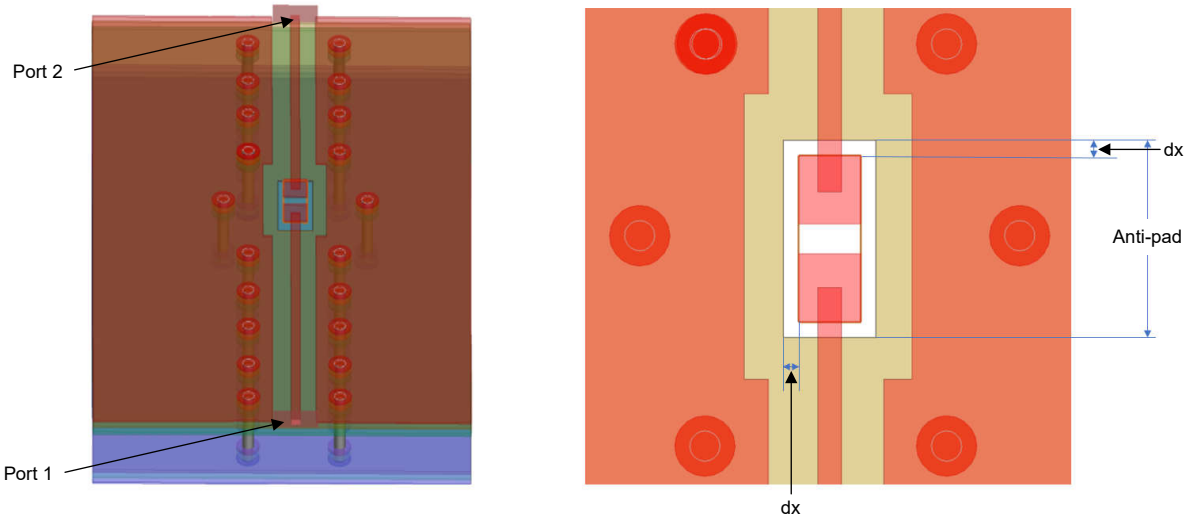


Figure 3-2. Simulation Model for Landing Pad and Anti-Pad

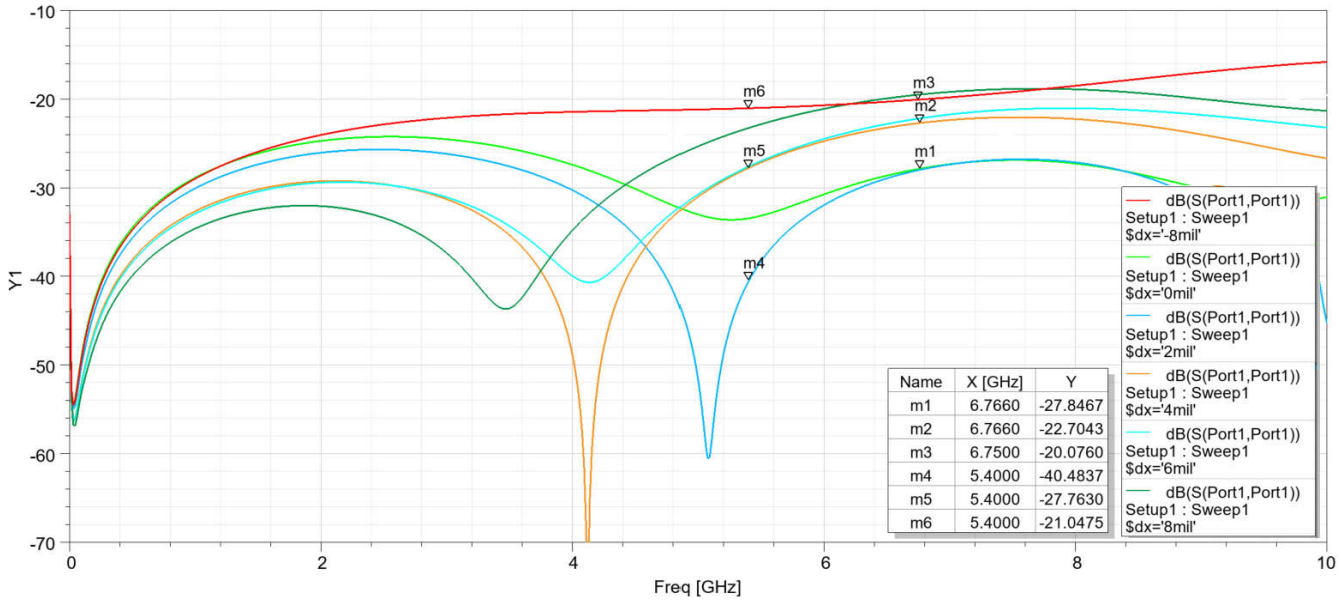


Figure 3-3. Return Loss (S11) With Different Anti-Pad Size

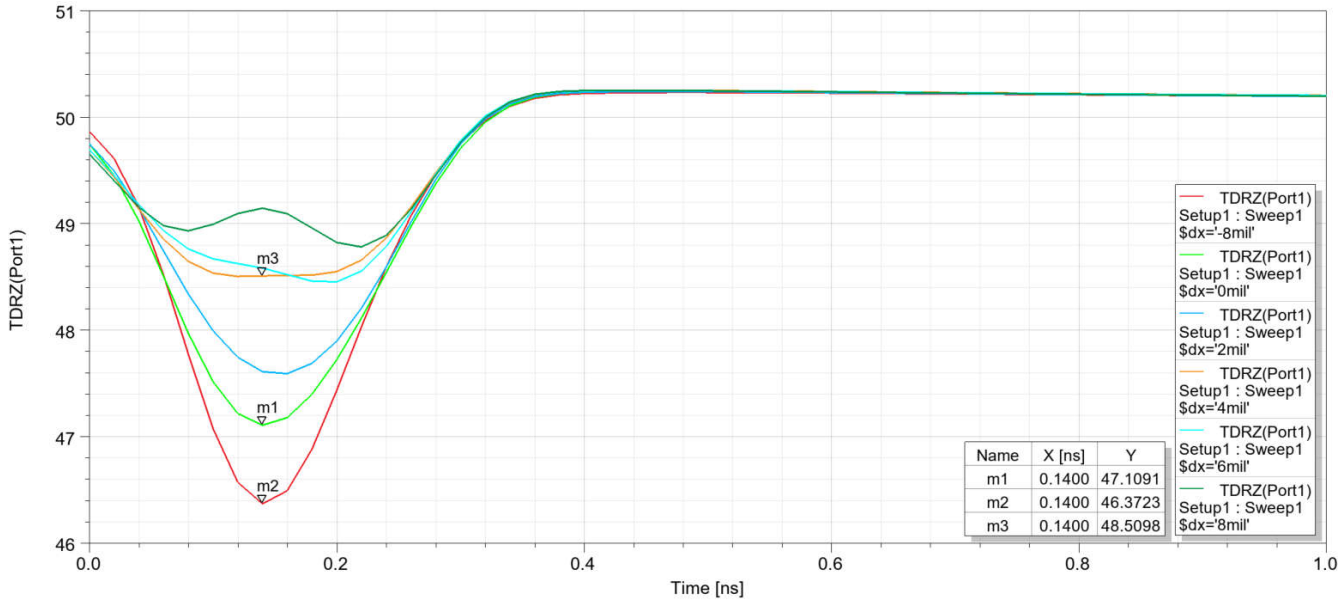


Figure 3-4. TDR Impedance With Different Anti-Pad Size

Key recommendations for AC coupling capacitor landing pad:

- Use anti-pad under the components when the landing pad size is larger than the matched 50Ω high-speed trace width (for example, IC pins, AC coupling capacitors, ESD diodes, line fault resisters).
- The size of the anti-pad depends on the specific PCB stackup, the recommendation is to perform a high-speed simulation to determine the proper anti-pad size.
- If possible, select a PCB stackup where the high-speed trace width matches the largest component pad size (for example, 0402 pad size). This approach helps to eliminate the need of anti-pads under the components and has the best impedance continuity.

3.3 Through-Hole Connector Footprint Impact and Optimization

The connector footprint is critical to minimize signal reflections to achieve good return loss performance. The designer is strongly recommended to simulate the connector footprint based on the board stackup.

3.3.1 Through-Hole Connector Via Anti-Pad Impact

The ground clearance around the through-hole connector signal via, also referred to as via anti-pad, can significantly impact the trace impedance due to the influence on the parasitic capacitance and return current path of the via. A larger anti-pad reduces parasitic capacitance between the signal via and the ground plane, resulting in an increase of impedance, while a smaller anti-pad lowers impedance. Proper anti-pad size is critical for minimizing impedance discontinuity.

3.3.1.1 Simulation Results With Ansys® HFSS

This section shows the simulation results using Ansys HFSS:

- Figure 3-5: Simulation model of the through-hole connector signal via
- Figure 3-7: Return loss (S11) simulation result with different connector via anti-pad size
- Figure 3-7: TDR impedance simulation result with different connector via anti-pad size

Both excessive anti-pad size and insufficient size can cause significant decrease or increase on the signal impedance and result in degraded return loss.

Anti-pads have a diameter of 42mil in this design example, reducing impedance variation and increasing return loss performance.

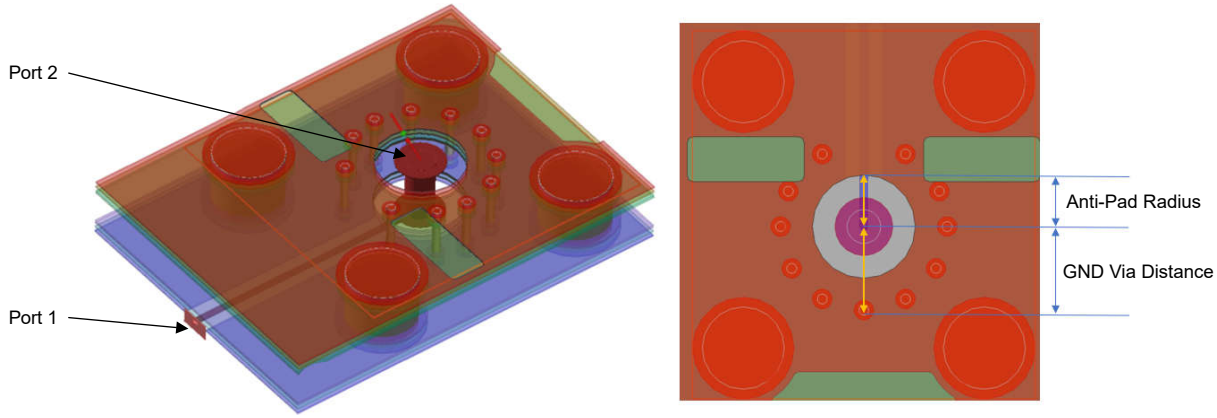


Figure 3-5. Simulation Model Of the Through-Hole Connector Signal Via

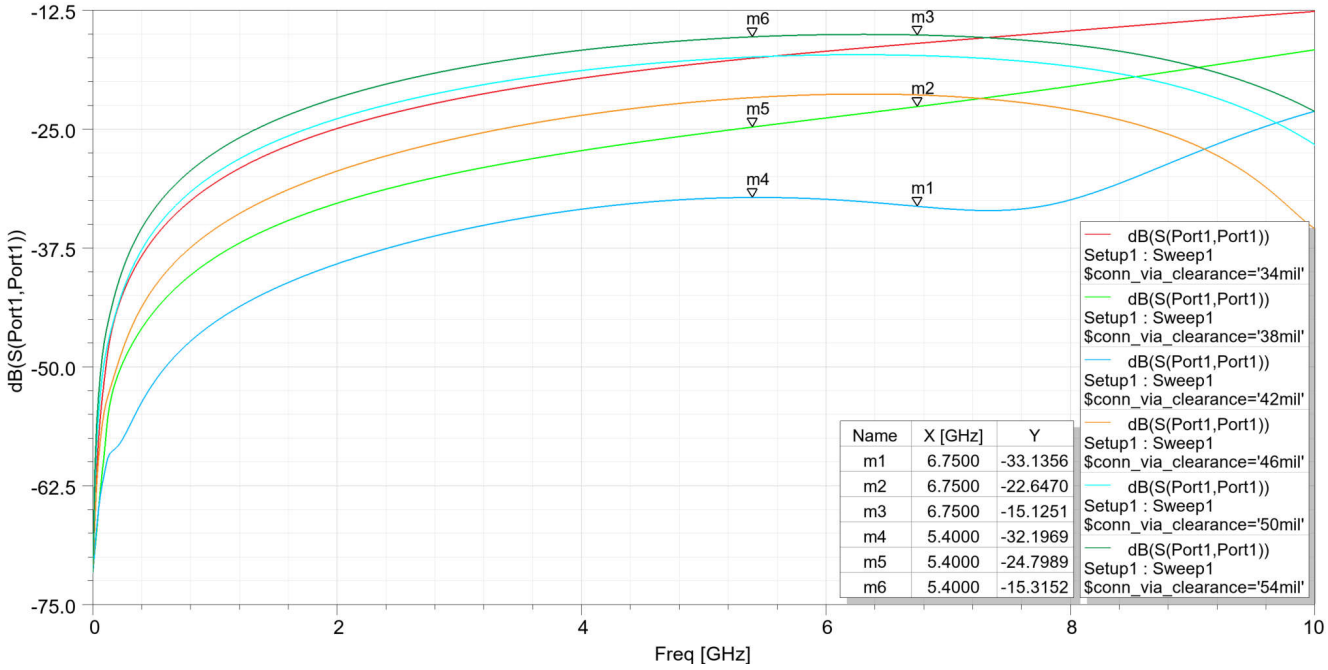


Figure 3-6. Return Loss (S11) With Different Connectors Via Anti-Pad Size

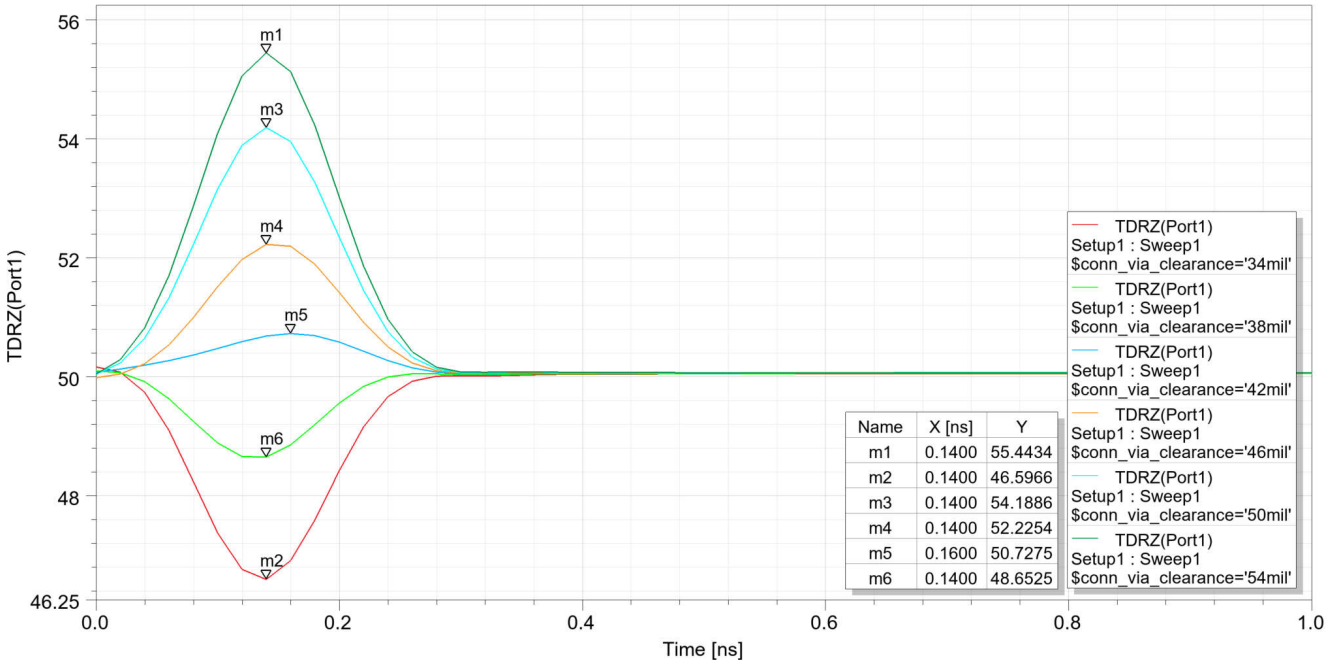


Figure 3-7. TDR Impedance With Different Connectors Via Anti-Pad Size

3.3.2 Surrounding Ground Vias Impact

TI recommends adding a circle of ground vias around the signal via because the spacing of ground vias directly influence the impedance stability. Closer ground vias shorten the return current path, minimizing loop inductance and stabilizing impedance. Wider spacing increases inductance, degrading high-frequency performance.

3.3.2.1 Simulation Results (Surrounding Ground Vias Impact)

This section provides the simulation results of the surrounding ground vias impact:

- Figure 3-8: Return loss (S11) with different ground via spacing
- Figure 3-9: TDR impedance simulation result with different ground vias spacing

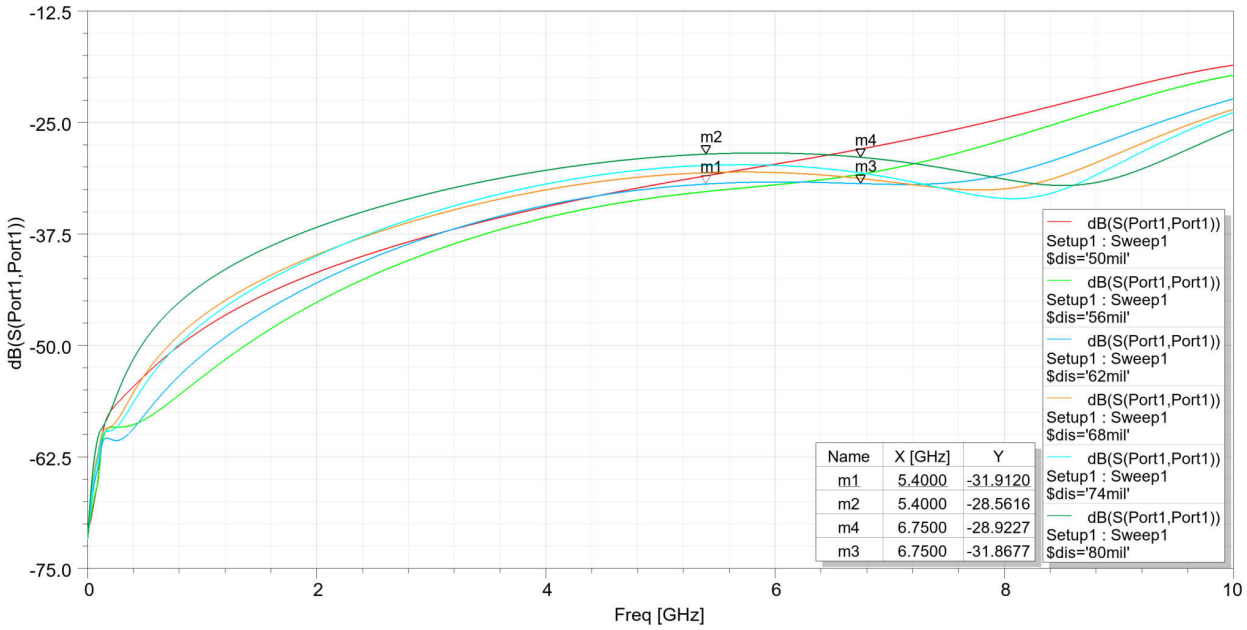


Figure 3-8. Return Loss (S11) With Different Ground Vias Spacing

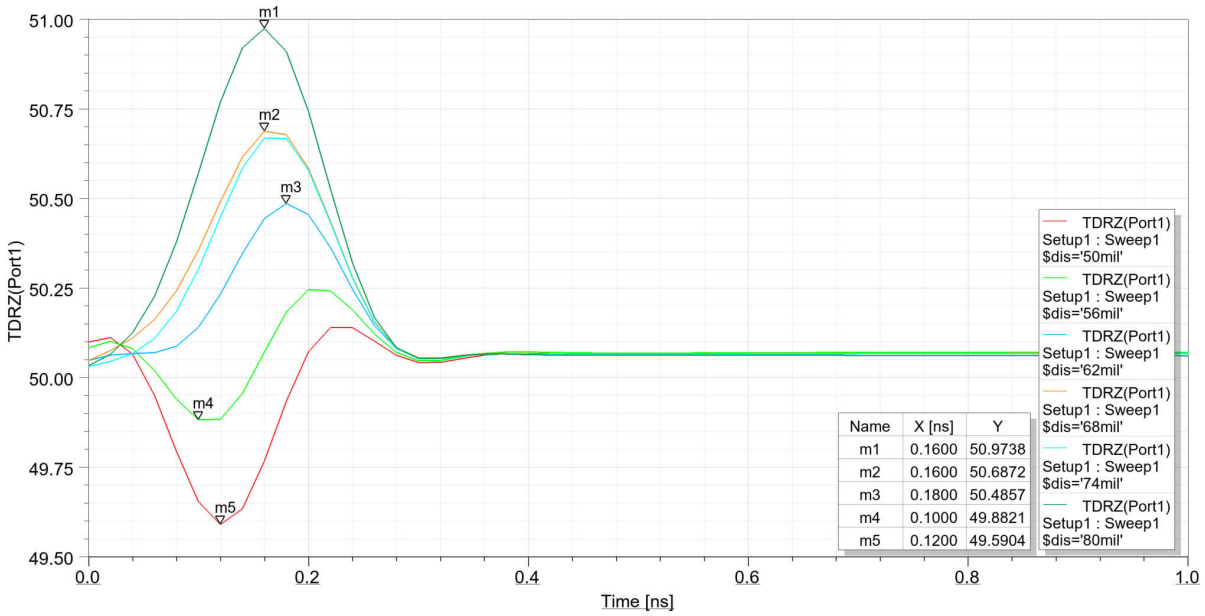


Figure 3-9. TDR Impedance With Different Ground Vias Spacing

The simulation results from Figure 3-6 to Figure 3-9 demonstrate that anti-pad size is the dominant factor for connector signal via impedance control due to the direct impact on capacitance; however, ground vias spacing is also important for managing impedance and cannot be neglected.

3.3.3 Non-Functional Pad Impact

Non-functional pads (NFPs) on unconnected via layers are often overlooked in high-speed PCB design, but NFPs introduce significant signal integrity risks. NFPs add parasitic capacitance (0.1pF–0.3pF per layer) and stubs, reducing impedance and degrading return loss.

3.3.3.1 Simulation Results (Non-Functional Pad Impact)

This section provides the simulation results of the non-functional pad impact:

- Figure 3-10: Pad-stack structure with and without NFPs in the middle layers
- Figure 3-11: Return loss (S11) with and without NFPs
- Figure 3-12: TDR impedance simulation result with and without NFPs

NFPs can severely influence return loss performance, the developer recommends removing the non-functional pads on unconnected layers.

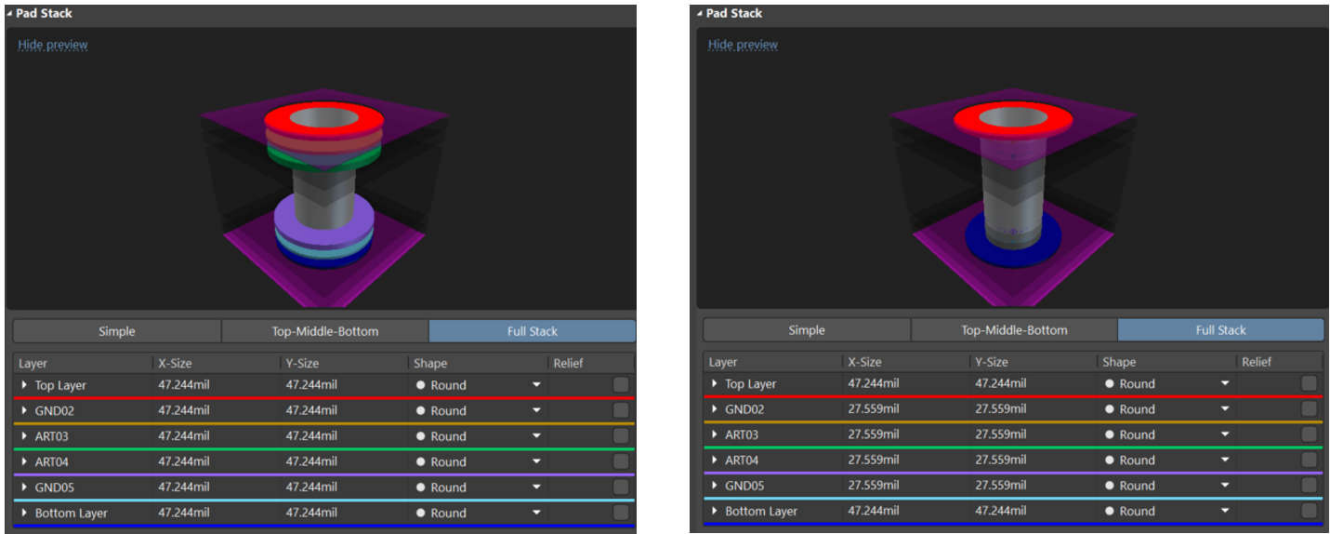


Figure 3-10. Pad-Stack Structure With and Without NFPs

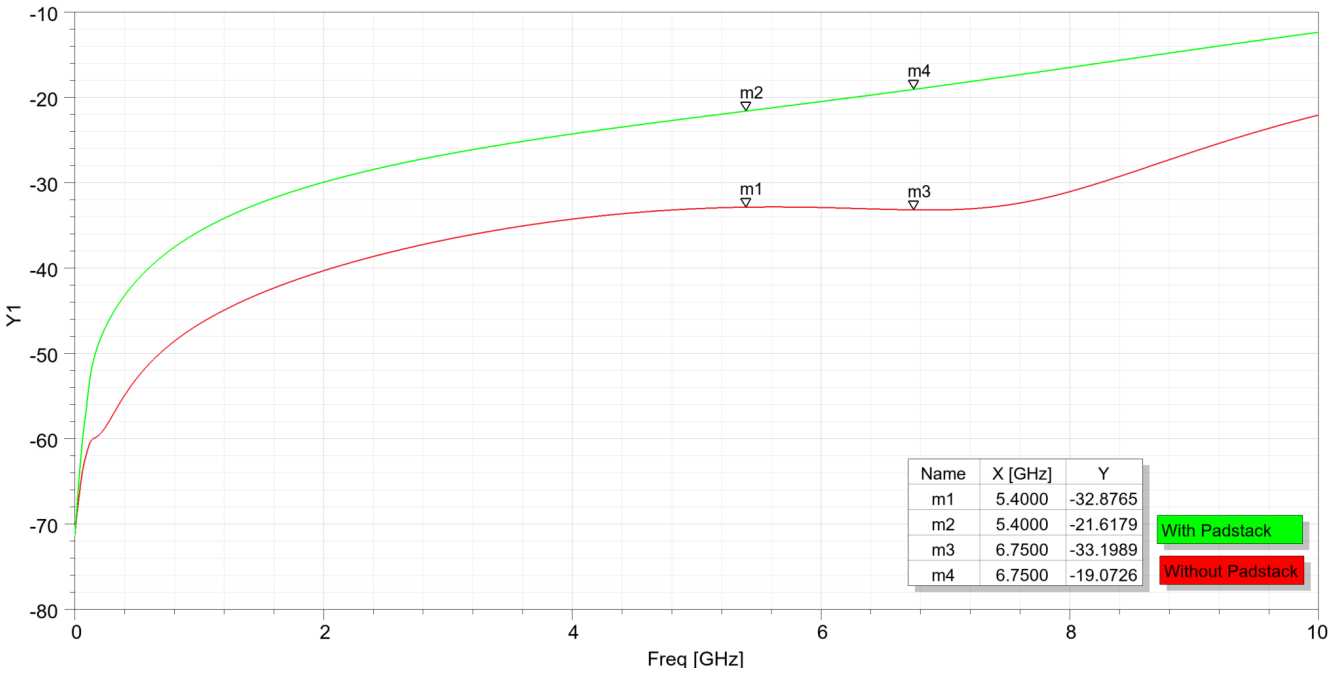


Figure 3-11. Return Loss (S11) Comparison With and Without NFPs

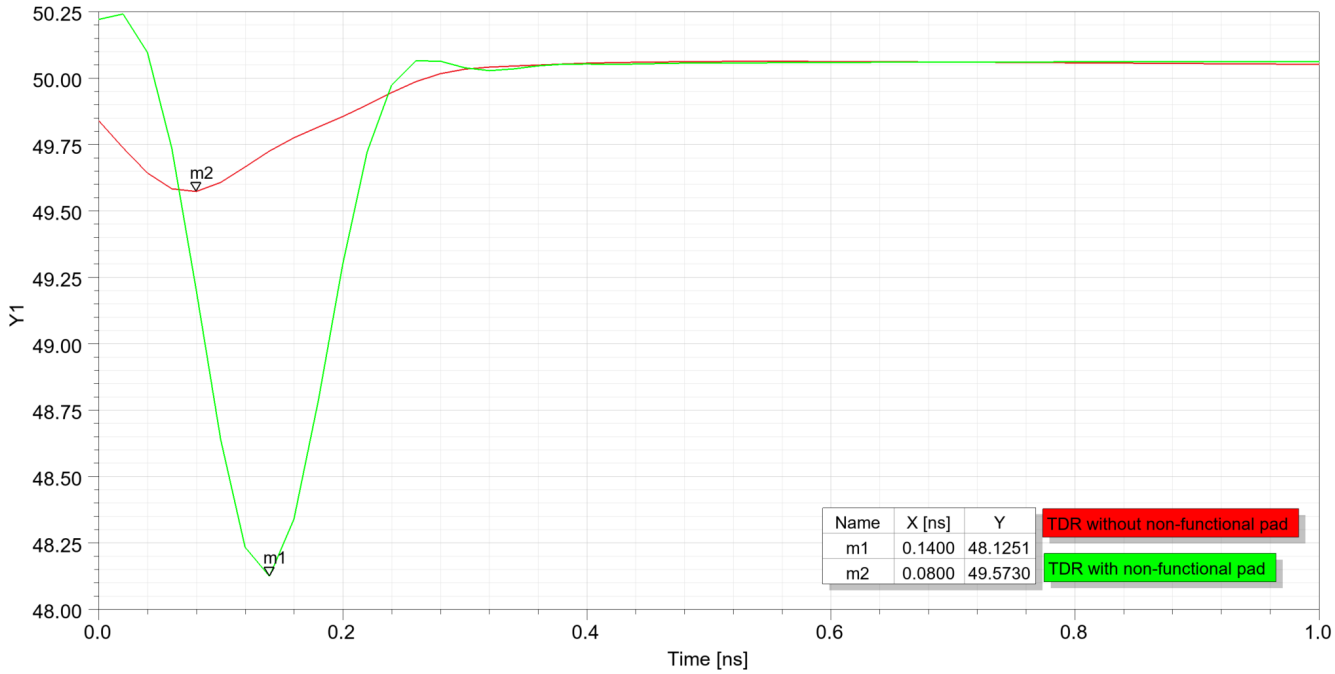


Figure 3-12. TDR Impedance Comparison With and Without NFPs

Key recommendations for through-hole connector footprint:

- The developer strongly recommends simulating the connector footprint based on board stackup.
- Connector signal via anti-pad size is the dominant factor for impedance control; therefore, requiring meticulous consideration in the design.
- Add surrounding ground vias, the ground vias spacing can also affect impedance and needs to be taken into account.
- Remove the NFPs on unused layers.
- Follow the footprint recommendations of the connector vendor.

3.4 Generic Signal Via Impact and Optimization

The generic signal via is similar to the connector signal via analyzed in Section 3.3. Both vias require optimization of anti-pad size and ground via spacing to manage parasitic capacitance and inductance to maintain impedance continuity. Figure 3-13 depicts the simulation model for a generic signal via, including adjacent ground plane with variable anti-pad clearances and symmetric ground vias arranged in a four-via quadrant configuration.

3.4.1 Simulation Results

This section provides the simulation results of the generic signal via impact and optimization:

- Figure 3-14 compares return loss (S11) performance across anti-pad radius (18–26 mil) and ground via spacing (26–42 mil).
- Figure 3-15 shows the TDR impedance profiles with different via anti-pad size and ground vias spacing as a reference.

In this specific design example, the best possible combination is 18mil anti-pad and 26mil ground via spacing, which can achieve S11 < –30dB at 6.75GHz. This high-risk combination is large anti-pad (26mil) + wide spacing (42mil) causing S11 degradation to 14.7dB at 6.75GHz.

The key recommendations for a generic signal via include:

- Implement a four-via quadrant configuration around the signal via to enhance return current path.
- Select the best possible combination of anti-pad size and ground vias spacing based on simulation.
- Remove the non-functional pads (NFPs) on unused layers.

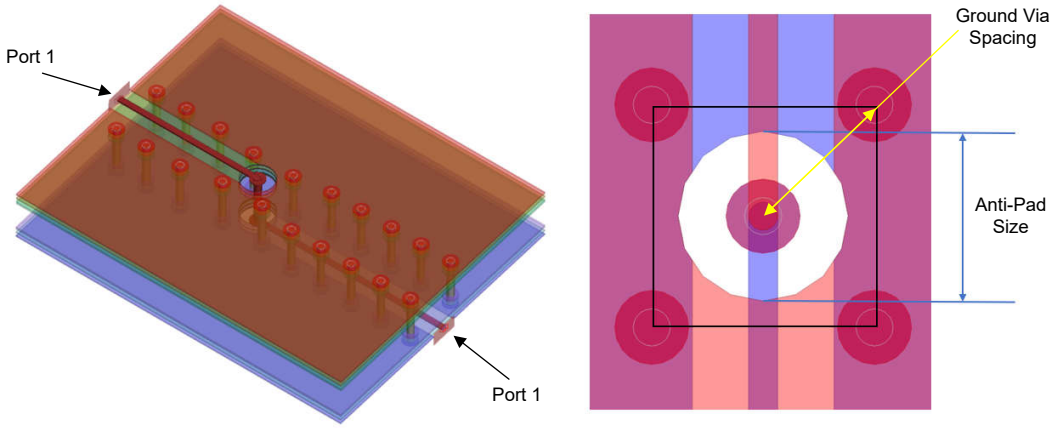


Figure 3-13. Simulation Model For Generic Signal Via

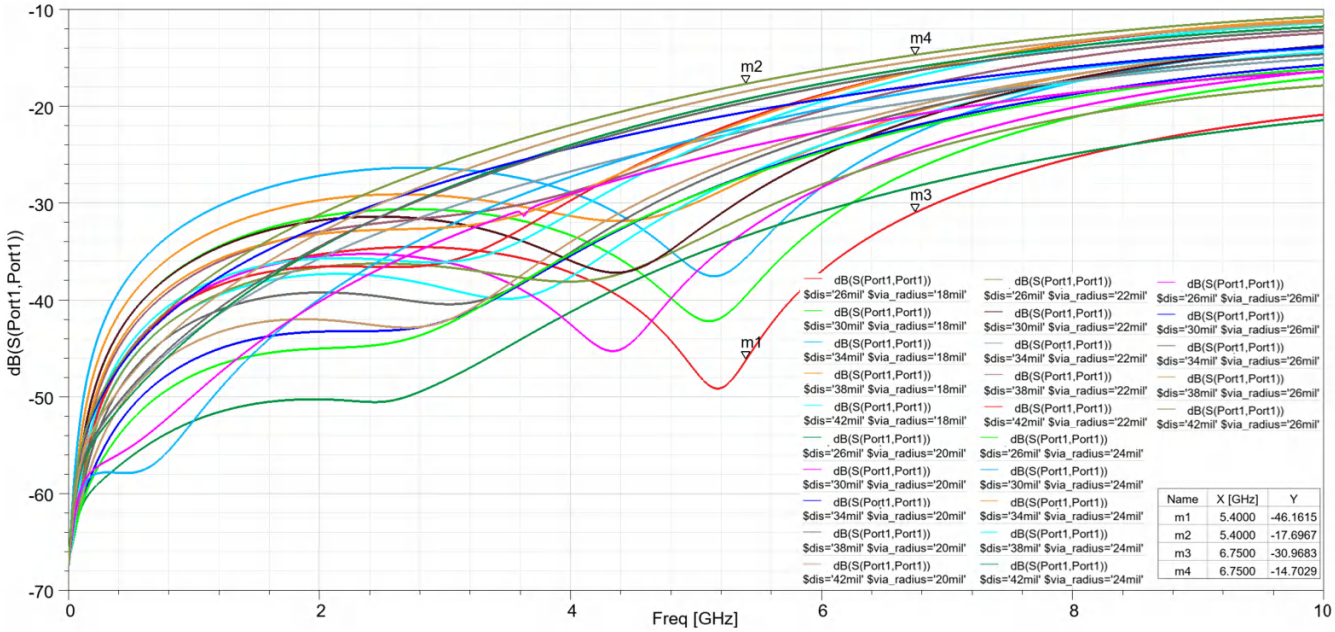


Figure 3-14. Return Loss (S11) With Different Via Anti-Pad Size and Ground Vias Spacing

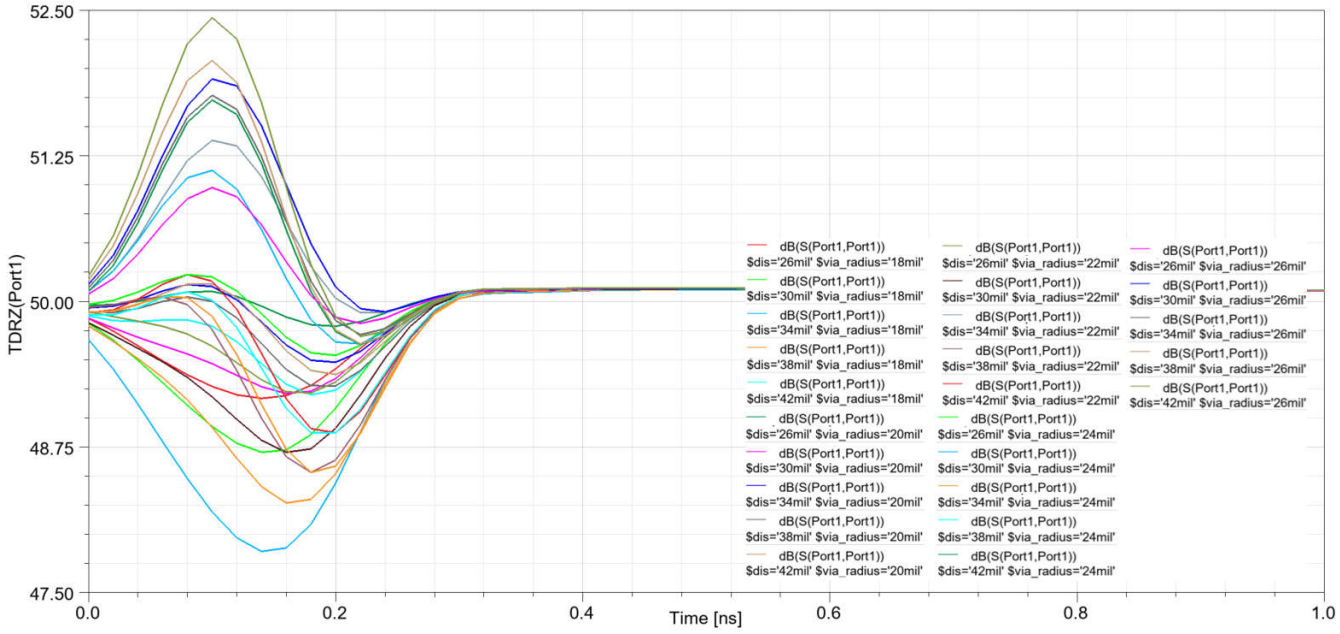


Figure 3-15. TDR Impedance With Different Anti-Pad Size and Ground Vias Spacing

3.5 ESD Diode Parasitic Capacitance Impact and Optimization

ESD diode inherent parasitic capacitance can significantly degrade signal integrity in high-speed applications. For instance, a 0.2pF parasitic capacitance impacts return loss (S11) at 6.75GHz as in the following:

1. Equation 3 details the capacitive reactance calculation.

$$Z_c = \frac{1}{jwC} = -j\frac{1}{2\pi fC} = -j\frac{1}{2\pi \times 6.75\text{GHz} \times 0.2\text{pF}} = -118j\Omega \quad (3)$$

2. Equation 4 shows the parallel impedance with 50Ω transmission line.

$$Z_{parallel} = \frac{50 \times (-118j)}{50 - 118j} \quad (4)$$

3. Equation 5 is the return loss degradation.

$$\text{Return loss (dB)} = 20\log_{10}\left|\frac{Z_{parallel} - 50}{Z_{parallel} + 50}\right| = -13.7\text{dB} \quad (5)$$

Assuming the original return loss is –30dB at 6.75GHz (typical for high-speed interfaces), the degradation caused by the 0.2pF capacitance is approximately 16.3dB.

As Figure 3-16 shows, the return loss (S11) across the entire PCB channel worsens progressively as ESD diode capacitance increases.

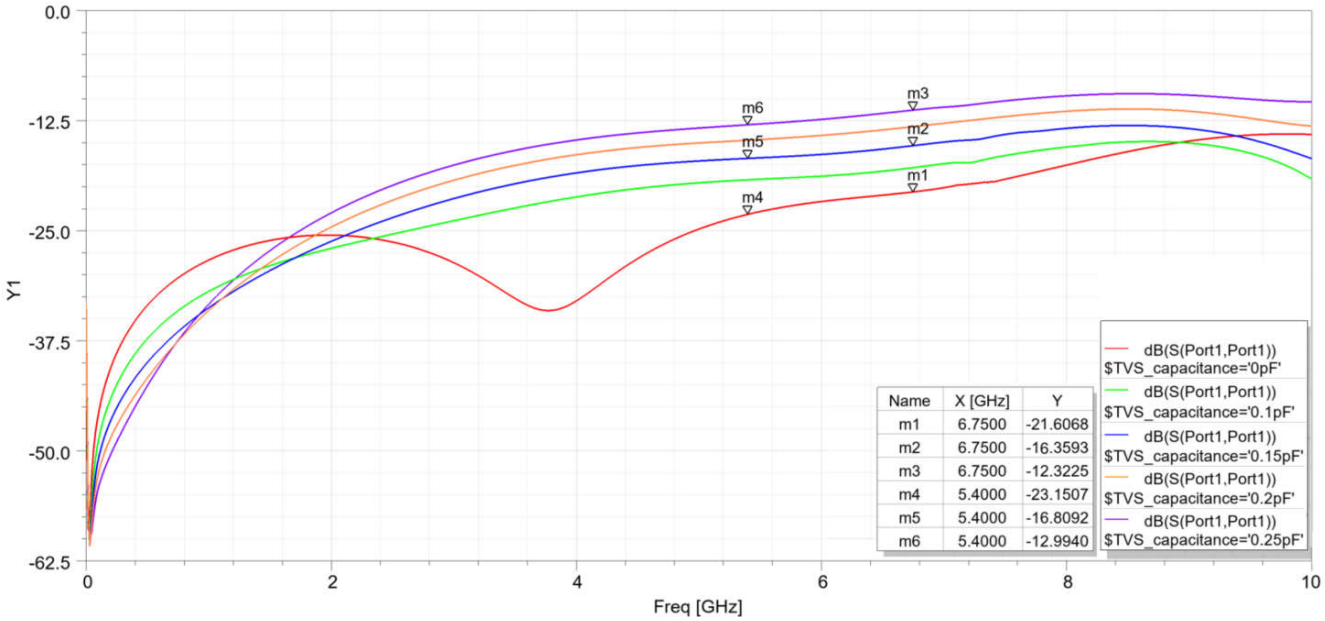


Figure 3-16. Return Loss (S11) With Different ESD Diode Capacitance

Parasitic capacitance from ESD diode inherent capacitance and ESD diode landing pad both severely impact impedance and return loss performance. Therefore, compensating for this capacitance effect is necessary.

- Using an anti-pad under the ESD diode can be a viable option to compensate for the parasitic capacitance.
- If anti-pad is not enough to compensate the capacitance:
  - Create anti-pad on more layers to make the signal trace refer to a deeper ground layer. For instance, create anti-pad on layer 2 and layer 3, and let the signal refer to layer 4. This increases dielectric thickness, raising more impedance to counteract capacitance effects.
  - Slightly narrow the trace near the ESD diode to compensate the capacitance. The narrowed trace introduces higher inductance, transforming the original parasitic capacitance into an inductor-capacitor-inductor (L-C-L) T-coil model, which can effectively compensate the capacitance-induced impedance drops.

Figure 3-17 is an example of slightly narrowing the trace near the ESD diode and enlarging the anti-pad to compensate parasitic capacitance effects.

Figure 3-18 compares the entire PCB channel return loss (S11) between the narrowed trace design and the original trace design (with ESD diode parasitic capacitance = 0.2pF). After optimization, the entire PCB channel (from the IC pin to the connecter via) return loss is improved by 3dB at 6.75GHz, and 4dB at 5.4GHz.

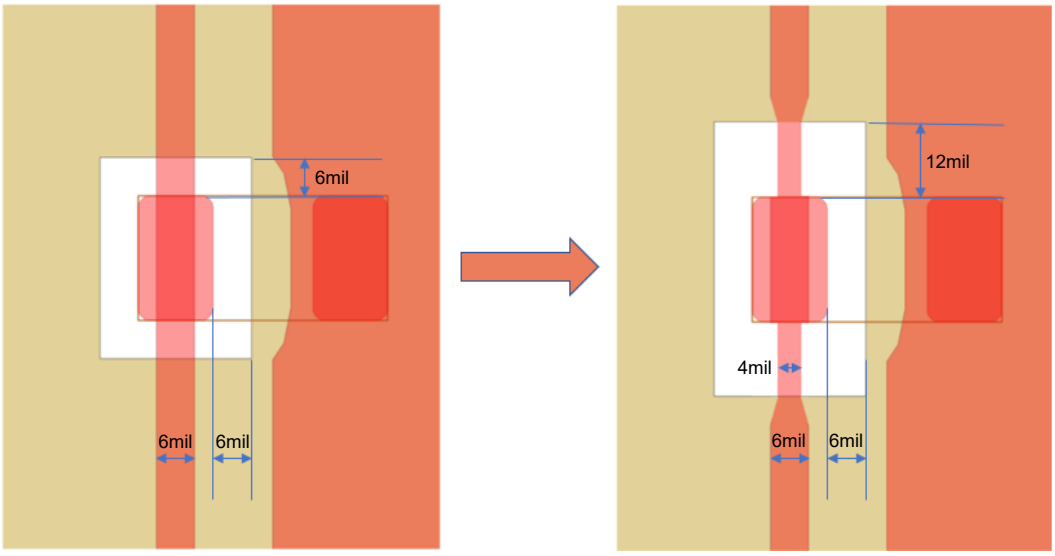


Figure 3-17. Simulation Model With and Without the Narrowed Trace Near ESD Diode

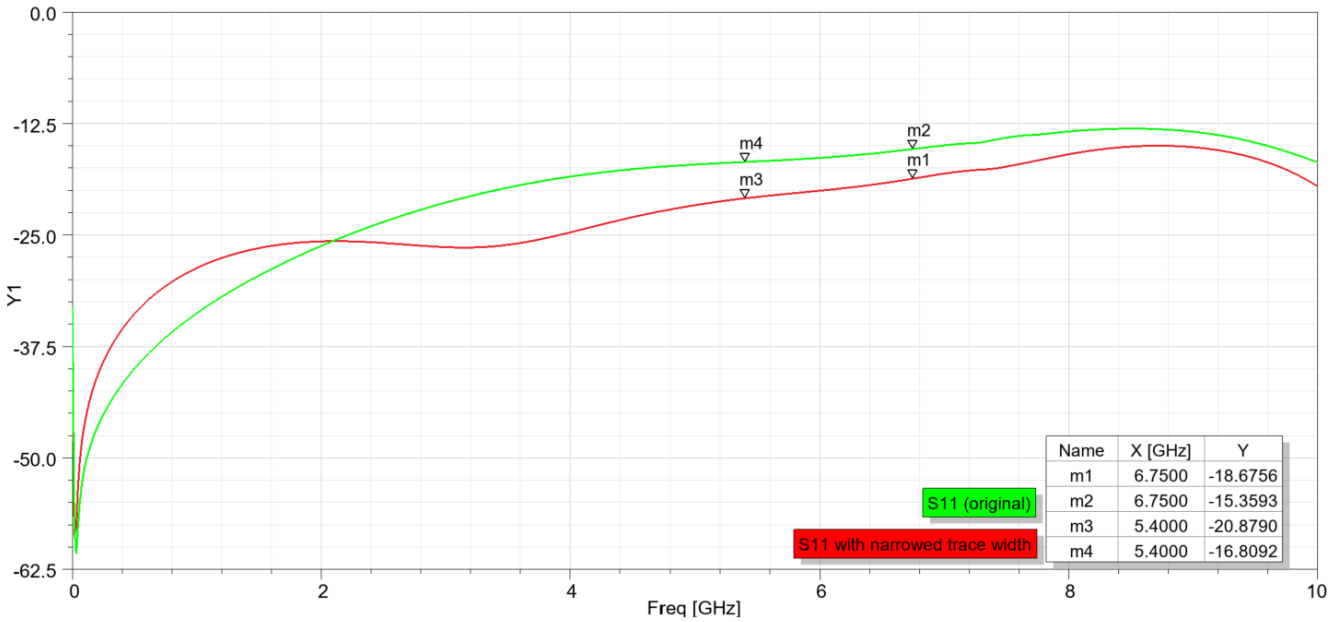


Figure 3-18. Return Loss (S11) With and Without the Narrowed Trace Near the ESD Diode

Key recommendations for the ESD diode:

- Reduce the ESD diode capacitance value to a lowest possible value (≤ 0.2pF). Increased parasitic capacitance degrades both return loss and insertion loss performance.
- Use compensation techniques in PCB layout design, such as adding single layer or multilayer ground cut-out (anti-pad) under the ESD diode, or narrowing the trace width near the ESD diode to compensate for the capacitance impact.
- Place the ESD diode directly onto the high-speed trace to avoid any stub.
- Place the ESD diode by use case. For systems requiring short-to-battery testing, the ESD diode can be placed on the chip-side of the AC coupling capacitor. For systems that are not requiring short-to-battery testing, the ESD diode can be placed as close as possible to the connector side for better ESD performance and signal integrity.
- Performing simulation to validate compensation strategies is highly recommended.

4 Summary

This application note analyzes the impact of critical factors such as transmission line impedance, AC coupling capacitor landing pad geometry, ESD diode parasitic capacitance, connector footprint and signal via structure on S-parameters performance. Optimization methodologies are proposed, including anti-pad design, ground via spacing optimization, removal of non-functional pads, and ESD diode capacitance compensation techniques.

Note

The simulation results and parameters selection presented in this article are only applicable to this specific design example. For the new designs, engineers must perform dedicated simulations tailored to the individual PCB stackup and layout to provide robustness and compliance with target channel specifications.

These design guidelines and optimization strategies are not confined to automotive SerDes applications, but can be extended to other high-speed domains.

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