Application Note

Efficiency Improvement With Y-Bridge in TAS2x20, TAS257x

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ABSTRACT

In the rapidly evolving landscape of portable electronics, the demand for richer features and enhanced performance is pushing designers to seek smarter ways to manage power consumption. Managing power efficiency without compromising performance is a growing challenge, especially in devices where audio quality is paramount. Texas Instruments (TI) has developed a remarkable design to this challenge with the enhanced Class-D audio amplifier architecture. This cutting-edge design optimizes power usage without sacrificing audio quality, offering a significant advantage for battery-powered devices like wireless speakers, earbuds, smart home gadgets, and mobile devices.

This article delves into real-world use cases, demonstrating how this technology extends battery life and enhances device performance. By adopting TI's optimized architecture, designers can push the boundaries of audio quality and efficiency, creating next-generation products that meet the demands of today's consumers.

Table of Contents

Trademarks

1 Introduction

Audio amplifiers traditionally use a low-voltage rail (VDD) for I/Os and internal biasing, alongside a high-voltage supply (PVDD) for power stage switching and amplification. At low voltage levels of the output signals, when the power demand is low, the efficiency often falls below 20% due to unnecessary headroom from the single high-voltage supply.

To address this inefficiency, TI developed the remarkable Y-Bridge architecture. This design enables the amplifier to seamlessly switch between two power supplies based on the required power level, reducing idle power consumption by 90% and boosting efficiency by 15–20% at low power levels, all without compromising audio performance. Combined with TI's industry-leading algorithms, this architecture helps original equipment manufacturers (OEM) to maximize efficiency and extend battery life of the OEM end products.

As shown in Figure 1-1, when Y-Bridge is being used, efficiency is significantly improved at low power (less than 100mW) over the traditional amplifiers with no Y-Bridge.

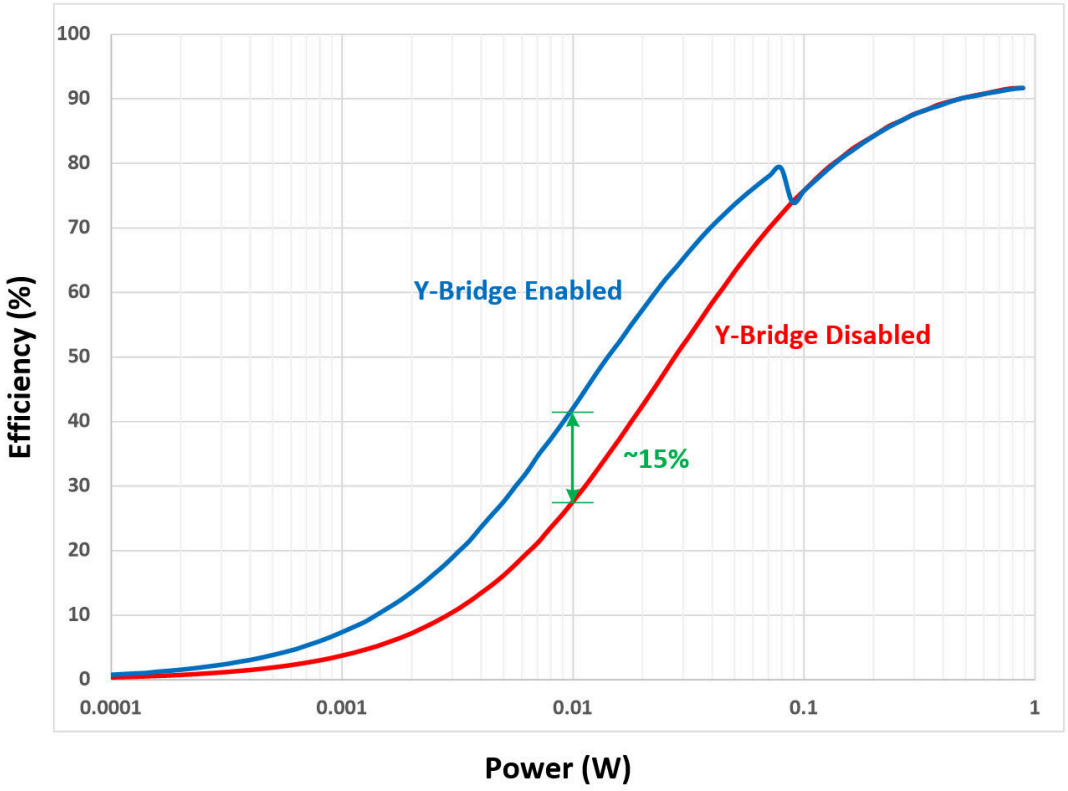

Figure 1-1. Efficiency Measured in EVM With and Without Y-Bridge

2 What is Y-Bridge

Y-Bridge is an amplifier architecture designed to switch between two power rails based on power demand with a programmable power threshold that optimizes efficiency at lower power levels and reduces consumption in standby or idle states. The architecture resembles a *Y* shape, distinguishing this from the traditional linear half-bridge design. Figure 2-1 shows the difference between a traditional Class-D amplifier vs the amplifier with Y-Bridge architecture.

For a classic half-bridge architecture, the output stage relies solely on a high-voltage supply (PVDD) for switching. In contrast, the Y-Bridge architecture utilizes both a high-voltage supply (PVDD) and a fixed low-voltage rail (VDD). At low output power levels, including idle states where minimal headroom is needed, the amplifier operates on the lower voltage rail (VDD) without causing clipping, significantly improving efficiency. When power demand rises and greater headroom is required, the amplifier seamlessly switches to the high-voltage supply (PVDD), matching the efficiency of a standard system without the Y-Bridge. This is why the benefits of the Y-Bridge can be realized the most at lower power levels, where traditional Class-D amplifiers are typically less efficient.

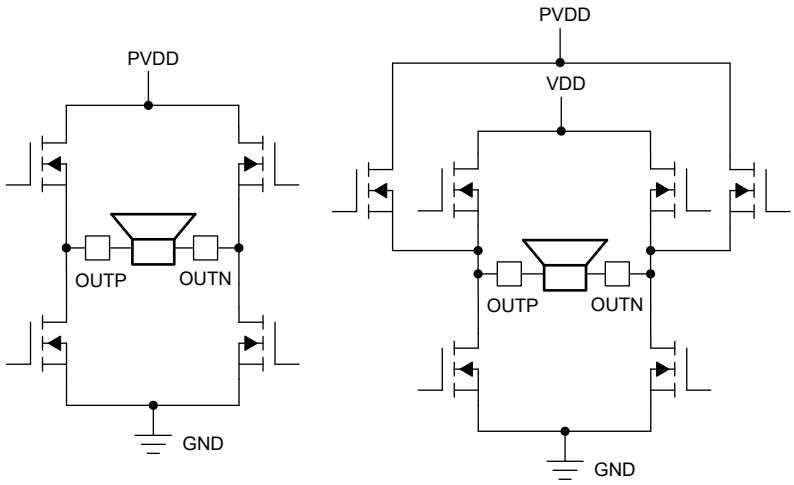

Figure 2-1. Traditional Class-D Amplifier vs Simplified Y-Bridge Architecture

TI's latest audio amplifiers — including the TAS2120, TAS2320, TAS2572, and TAS2574 — feature the Y-Bridge architecture. Users can configure the device to enable or disable this functionality, but when disabled, the amplifier relies solely on the PVDD supply. In this case, this is essential to make sure the PVDD voltage is high enough to prevent clipping.

3 Benefits of Y-Bridge

The Y-Bridge feature is particularly advantageous for systems requiring a high-voltage power stage supply, such as 2S–4S battery configurations (7V–14V). In Texas Instruments devices, this pin is typically referred to as PVDD. The PVDD supply can be sourced from an external power supply, an external boost circuit output, or generated internally from the VBAT using an integrated boost circuit, available in devices like the TAS2572, TAS2574, and TAS2120. The VDD rail, also represents the lower voltage supply already present in the system, typically 1.8V in the TAS2x20 and TAS257x device families. When the power stage supply (PVDD) is 5V or higher, switching between PVDD and the 1.8V rail offers greater benefits compared to scenarios where PVDD is less than 5V. Therefore, the Y-Bridge feature is most advantageous in systems that require a high-voltage output stage.

Additionally, the Y-Bridge feature dynamically selects between PVDD and VDD based on a predefined threshold. When the audio output signal exceeds a programmed threshold, the Class-D output switches to the high-voltage supply (PVDD). Below this threshold, the output continues using the 1.8V rail (VDD). This threshold is user-configurable, typically set around 100mW for most use cases. The efficiency plot illustrates the improved efficiency up to this threshold. Beyond this point, the efficiency typically aligns with that of a system without the Y-Bridge.

Figure 3-1 shows the functional block diagram of a smart amplifier with Y-Bridge feature

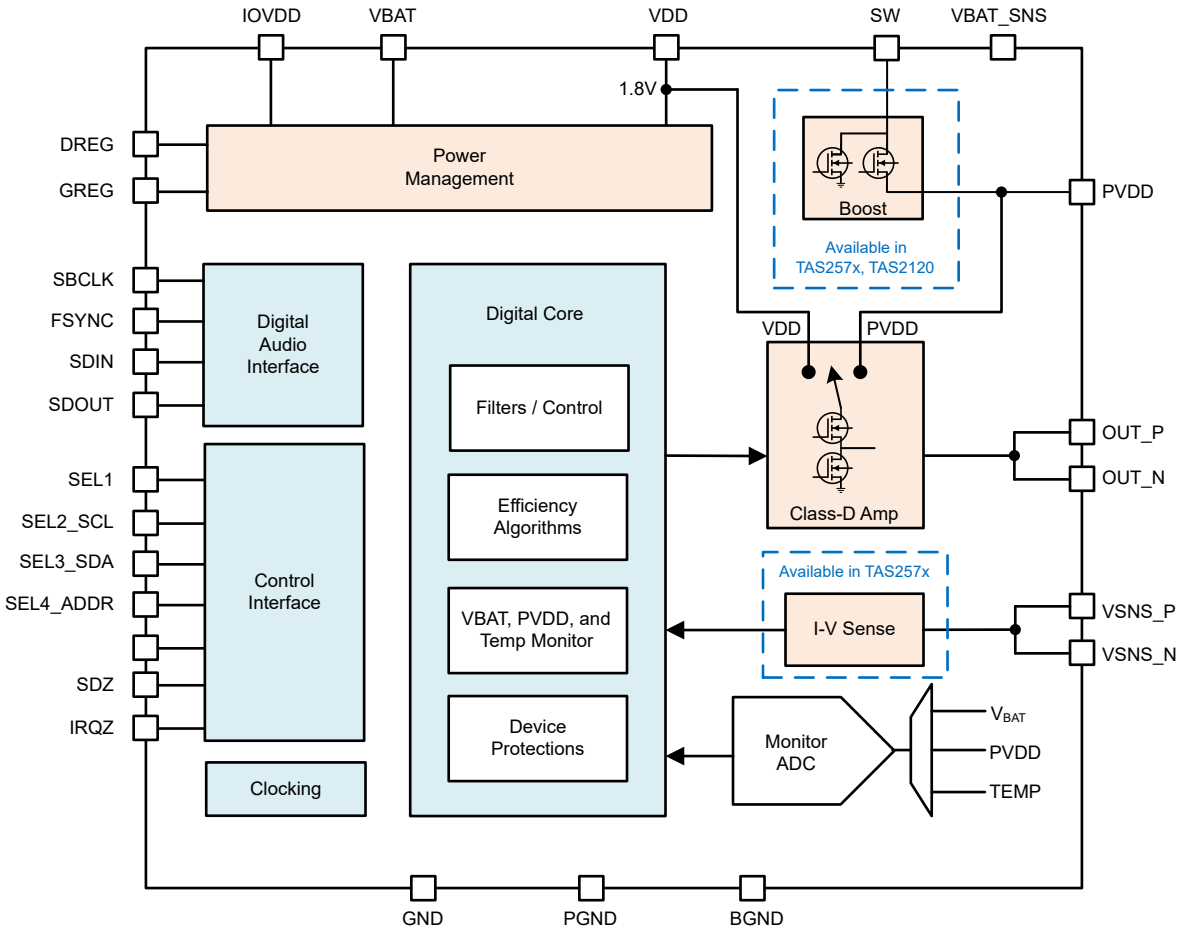

Figure 3-1. Functional Block Diagram of a Smart Amplifier With Y-Bridge Feature

4 Configuration of Y-Bridge

This application note details the process of configuring the Y-Bridge registers for the TAS2x20 and TAS257x device families. Both families utilize the Y-Bridge configuration to enhance efficiency during audio playback. When the feature is enabled using *EN_Y_BRIDGE_MODE* set to high, the device can automatically select the output voltage to switch the output PWM.

Table 4-1. VDD Y-Bridge Mode Configuration

EN_Y_BRIDGE_MODE	Configuration
0	Y-Bridge mode is disabled
1 (default)	Y-Bridge mode is enabled

When the audio signal level is low, the output can switch at 1.8V (VDD) to enable higher system-level efficiency by reducing the class-D output switching voltage. Conversely, when the audio signal level is high, the output switches at PVDD to make sure the required output power level is met.

5 Y-Bridge Thresholds and Hysteresis Registers

The device continuously monitors the input audio signal level against the Y-Bridge mode threshold configured in the *VDD_MODE_THR_LVL [23:0]* register. When the audio signal drops below this threshold, an internal hysteresis timer is activated. If the signal remains below the threshold for the duration specified by the *YBRIDGE_HYST_TIMER [1:0]* register, the device switches to a lower voltage (1.8V) VDD supply-based PWM switching mode. Once the signal level exceeds the threshold defined by the *VDD_MODE_THR_LVL [23:0]* register plus the *VDD_MODE_HYST [23:0]* register, the device starts switching the output PWM signal on PVDD supply without introducing any signal clipping.

Both the *VDD_MODE_THR_LVL [23:0]* and *VDD_MODE_HYST [23:0]* registers can be configured using the PPC3 software tool.

Table 5-1. VDD_MODE_THR_LVL Register

Bit	Field	Type	Reset	Description
23-0	VDD_MODE_THR_LVL[23:0]	R/W	50A3D7h	Addresses 0x8 to 0xA are combined. Can be configured using the PPC3 Software.

Table 5-2. VDD_MODE_HYST Register

Bit	Field	Type	Reset	Description
23-0	VDD_MODE_HYST[23:0]	R/W	DA74h	Addresses 0xC to 0xE are combined. Can be configured using the PPC3 Software.

Table 5-3. VDD Y-Bridge Hysteresis Timer

YBRIDGE_HYST_TIMER[1:0]	Configuration
00	100us
01 (default)	500us
10	5ms
11	50ms

Unlike the TAS257x family, TAS2x20 devices can be configured using either hardware pin control or I²C control. In hardware pin control mode, the user can select one of the three predefined configurations for the Y-Bridge threshold. In contrast, for I²C or software control mode, the Y-Bridge threshold is defined by the combination of the *VDD_MODE_THR_LVL* and *VDD_MODE_HYST* registers as described previously.

Table 5-4. SEL4 HW Mode Configuration

SEL4_ADDR Connection	Configuration
Direct Short to GND	Y-Bridge threshold of 80mW
Direct Short to Supply	Y-Bridge threshold of 40mW
24k to Supply	Y-Bridge threshold of 1mW

Additionally, in hardware pin control mode, the hysteresis timer is set to a default value of 500 microseconds. In contrast, for I²C or software control mode, the hysteresis timer value can be customized via the *YBRIDGE_HYST_TIMER* register as mentioned above.

6 1S, 2S and External PVDD Mode

The TAS2572, TAS2574, and TAS2120 devices feature an integrated Class-H boost circuit as well as supporting 1S, 2S, and External PVDD mode. As a result, the Y-Bridge PVDD voltage can vary depending on the specific use case and the application circuit. PVDD voltage can be same as the voltage on the VBAT pin when there is no power demand for the boost voltage (boost by-pass mode), or this can come from an external fixed supply (if a high voltage rail is already available in the system), or this can also come from an external boost circuitry. Therefore, depending on the 1S, 2S and external PVDD mode, the PVDD high voltage can vary.

In boost bypass mode, where the boost is not required, the PVDD voltage can be identical to the VBAT voltage (ranging from 2.5V to 5.5V). In this case, PVDD = VBAT.

In integrated boost mode, the PVDD voltage is determined by the internally generated boost output, which is derived from the VBAT supply. Here, PVDD = internal boost output voltage.

In external PVDD mode, the PVDD voltage is sourced either from a fixed external power supply or by an external boost output. This mode is particularly applicable to the TAS2320 device, which does not feature an integrated boost circuit.

7 Efficiency Improvement for Different Use Cases

Figure 7-1 demonstrated that enabling the Y-Bridge can lead to a power consumption reduction of up to 75% compared to the scenario when absent or not enabled. The degree of power savings can vary depending on the specific use case. For example, audio tracks with silent segments achieve higher power savings than continuous audio tracks, such as music. This substantial reduction in power consumption results in an efficiency improvement of 15-20% in lower power modes, when compared to traditional amplifiers that do not utilize the Y-Bridge architecture.

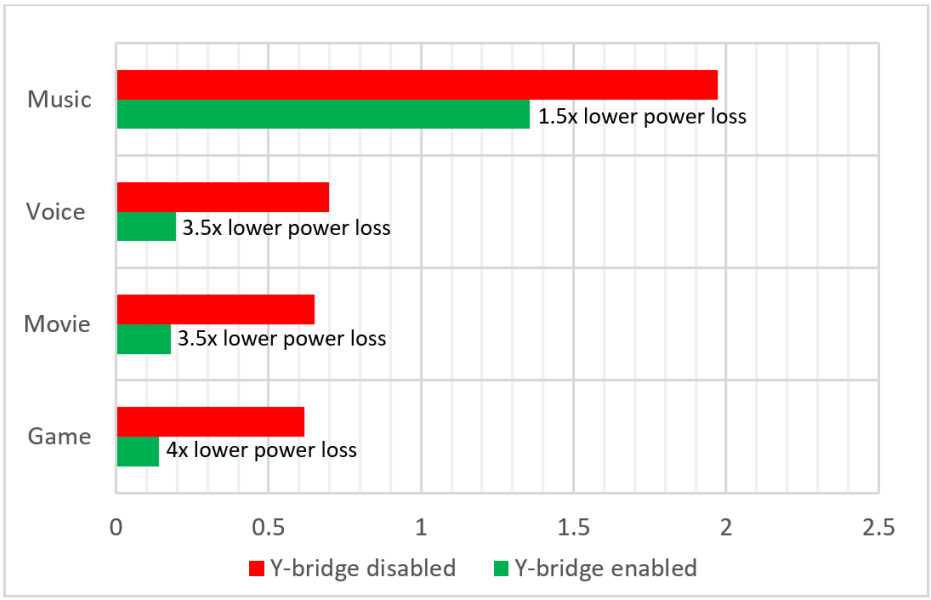

Figure 7-1. Power Consumption Measured in EVM Connected to Laptop Speakers (in W)

8 Summary

To achieve an efficient audio design with extended battery life, the recommendation is to use an audio amplifier with a Y-Bridge architecture. Texas Instruments latest audio amplifiers incorporate this architecture, combined with cutting-edge audio enhancement algorithms. By using the Y-Bridge configuration, designers can optimize system power consumption, enabling more efficient power management. This leads to significant reductions in power usage, ultimately providing longer battery life and enhanced user experience.

9 References

- Texas Instruments, *TAS2572: 6.6W Digital-In Smart Amplifier with I/V Sense and Integrated 13V Class-H Boost*
- Texas Instruments, *TAS2574: 8.5W Digital-In Smart Amplifier with I/V Sense and Integrated 15V Class-H Boost*
- Texas Instruments, *TAS2120: 8.2W Mono Digital-In Class-D Amplifier with Integrated 15V Class-H Boost*
- Texas Instruments, *TAS2320: 15W Mono Digital-In Class-D Amplifier with 14V External Boost Support*

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