Application Note

TAS2x20 Design and Layout Guidelines

Ivan Salazar

ABSTRACT

The TAS2x20 family of audio amplifiers is a class of digital input Class-D audio amplifiers optimized for efficiency and battery life in real music and voice applications. The amplifier is capable of delivering high output power using an integrated Class-H boost converter for TAS2120 and external boost for TAS2320.

This application note describes the recommended practices in the design and PCB layout for designs that use this family of devices to provide high quality and reliability of the device in the system, and enable higher efficiency and performance once integrated into the system.

Table of Contents

Trademarks

1 Introduction

TAS2x20 is a digital-input Class-D amplifier family. TAS2120 takes a voltage supply from a single or multi-cell battery source, and boosts the supply to a high voltage. TAS2320 takes a voltage supply directly from a higher voltage source such as multi-cell battery or AC/DC adapter. These features enable the user to play audio and deliver high power into a speaker load.

When using this device in audio designs, the PCB design is a critical factor. To verify that the device is reliable and meets the required performance and functionality criteria, while minimizing losses to maintain system efficiency, certain design and layout practices need to be accounted for while designing the application.

This application note provides a set of recommended guidelines that need to be followed, which enable the user to operate the device at designed for performance and efficiency. The TAS2120EVM is used as a reference to highlight these guidelines.

2 Application Schematics

The following figures show the various configurations that the TAS2x20 can be connected in. Figure 2-1 shows the TAS2120 in 1S configuration, where a single-cell battery is used as the voltage source to power up the device.

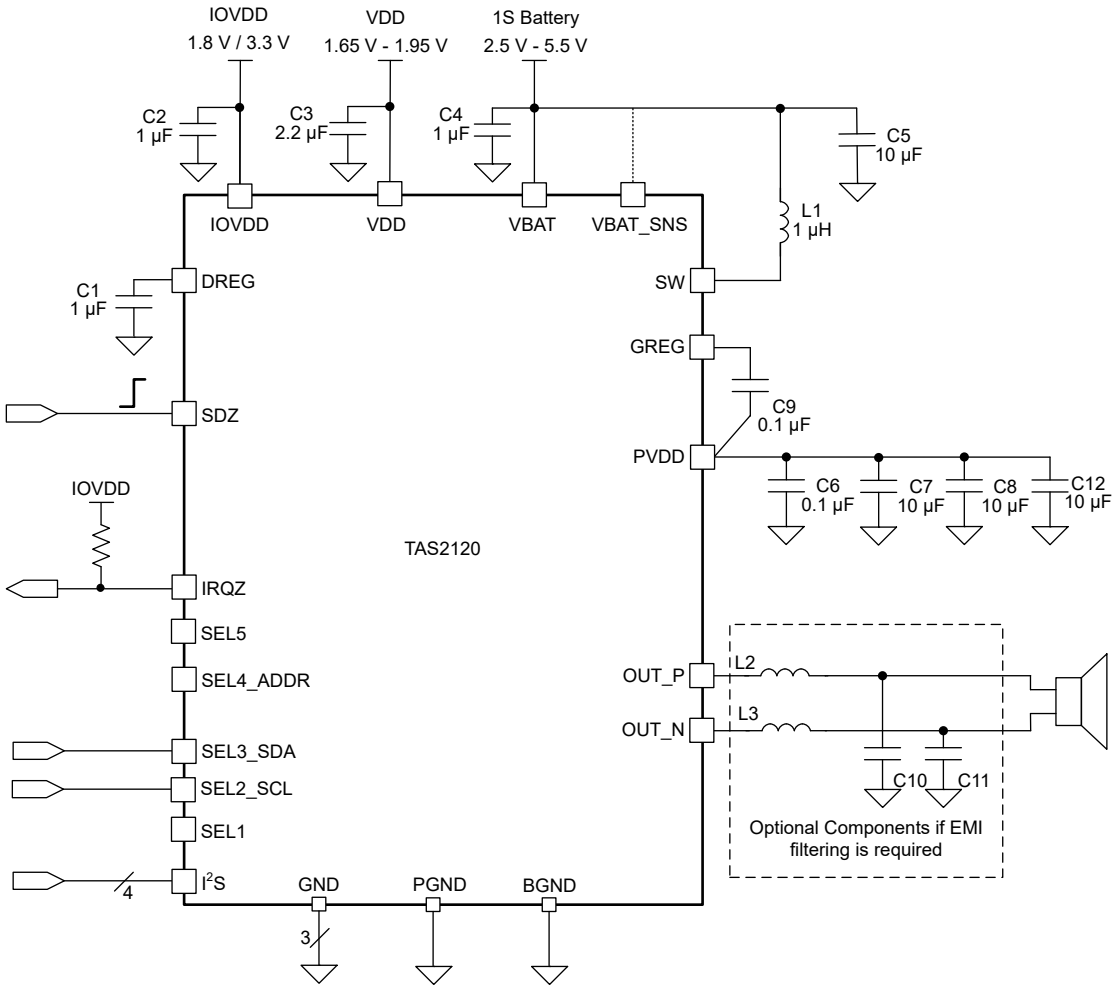

Figure 2-1. TAS2120 in 1S Configuration

Figure 2-2 shows the device being connected in 2S configuration, with a 2-cell battery acting as the power source for the device.

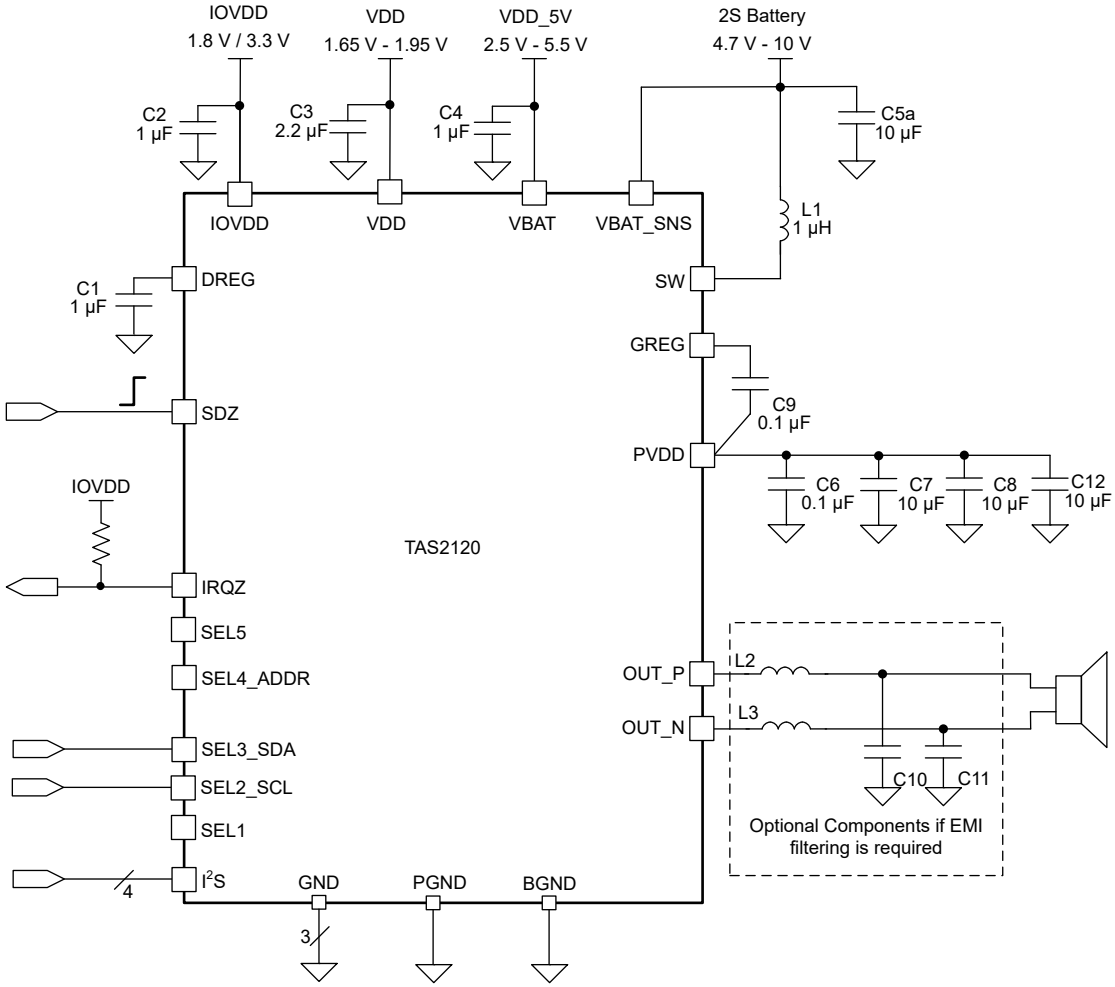

Figure 2-2. TAS2120 in 2S Configuration

Figure 2-3 shows an external PVDD configuration for the TAS2320 where the internal boost converter of the device is disabled, and the PVDD can be provided externally from a 3-cell battery.

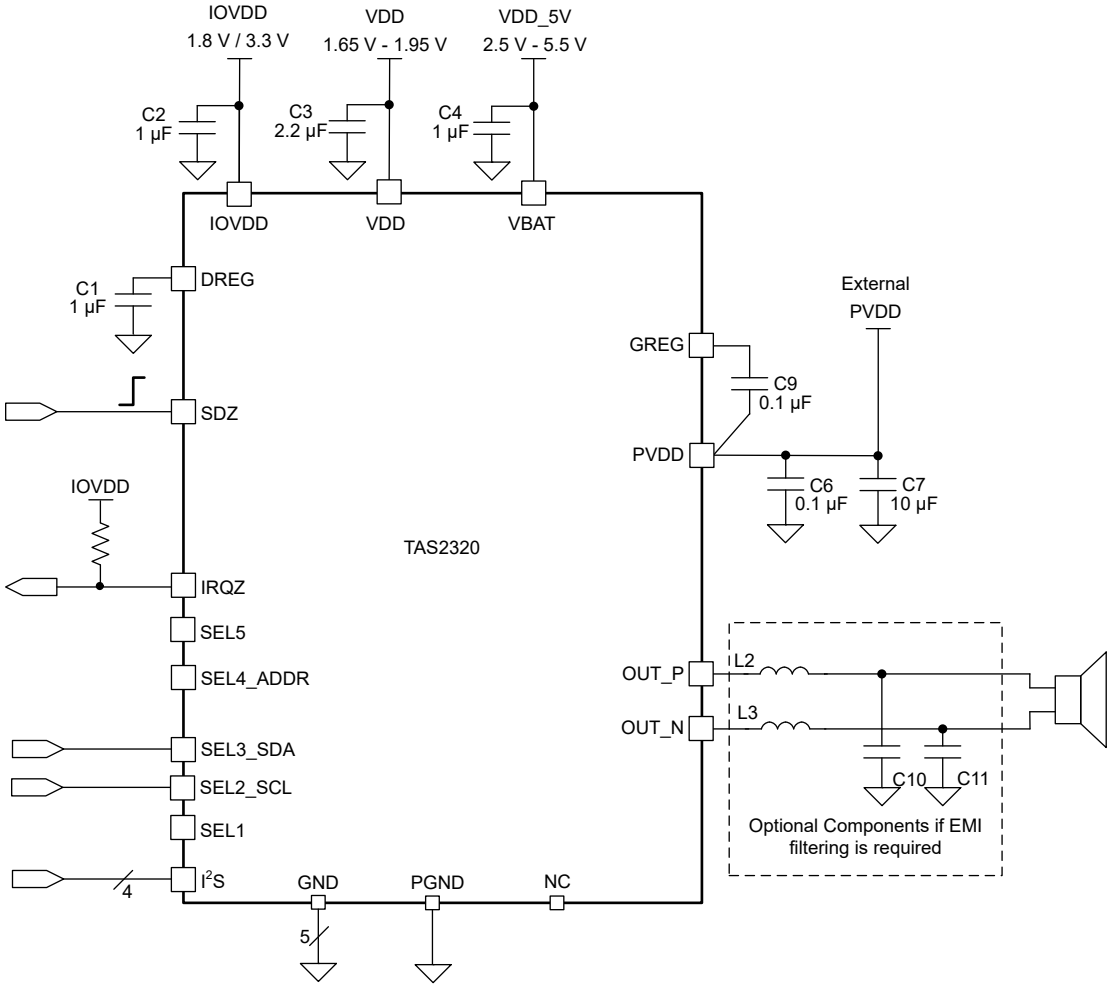

Figure 2-3. TAS2320 in External PVDD Configuration

2.1 Recommended Component Ratings

Table 2-1 shows the recommended component ratings for the components shown in Figure 2-1, Figure 2-2, and Figure 2-3.

Table 2-1. Component Ratings

Component	Description	Specification	Min	Typical	Max	Unit
L1	Boost Converter Inductor	Inductance	0.47	1	-	µH
		Saturation Current	-	5.3	-	A
L2, L3	Optional EMI Filter Inductors	DC Current	2	-	-	A
C1, C2	DREG, IOVDD decoupling capacitors	Capacitance 20% tolerance	-	1	-	µF
		Voltage Rating	2	6.3	-	V
C3	VDD decoupling capacitor	Capacitance 20% tolerance	-	2.2	-	µF
		Voltage Rating	4	6.3	-	V
C4	VBAT decoupling capacitor	Capacitance 20% tolerance	-	1	-	µF
		Voltage Rating	6.3	10	-	V
C5	VBAT power decoupling capacitor	Capacitance 20% tolerance	-	10	-	µF
		Voltage Rating	6.3	10	-	V

Table 2-1. Component Ratings (continued)

Component	Description	Specification	Min	Typical	Max	Unit
C5a	VBAT2S decoupling capacitor	Capacitance 20% tolerance	-	10	-	µF
		Voltage Rating	10	16	-	V
C6	PVDD Low-ESL decoupling capacitor	Capacitance 20% tolerance	-	0.1	-	µF
		Voltage Rating	16	25	-	V
C7, C8, *C12	PVDD Power decoupling capacitors. C12 required only for Boost output >13V	Capacitance 20% tolerance	-	10	-	µF
		Voltage Rating	16	25	-	V
		De-rated capacitance at 13V of the combined PVDD capacitor	3	-	-	µF
C9	GREG decoupling capacitor	Capacitance 20% tolerance	-	0.1	-	µF
		Voltage Rating	6.3	10	-	V
C10, C11	Optional EMI Filter capacitors (must use L2, L3 if C10, C11 are used)	Voltage Rating	2xPVDD		-	V

Function selection pins in hardware mode must be connected to IOVDD, VBAT or GND using specific resistor values for each of the options, follow the Table 2-2 table to select the correct component values.

Table 2-2. Hardware Select Pin Resistor Values

Hardware Select Pin	Resistor Value	Description
SEL1	0Ω to VBAT	21dBV and Volume Ramp Enabled
	24kΩ to VBAT	18dBV and Volume Ramp Enabled
	24kΩ to GND	12dBV and Volume Ramp Enabled
	5kΩ to VBAT	6dBV and Volume Ramp Enabled
	330Ω to VBAT	21dBV and Volume Ramp Disabled
	5kΩ to GND	18dBV and Volume Ramp Disabled
	1.2kΩ to VBAT	12dBV and Volume Ramp Disabled
	1.2kΩ to GND	6dBV and Volume Ramp Disabled
	0Ω to GND	I^2C Mode
SEL2	1.2kΩ to IOVDD	Left Justified Right Channel or TDM Slot 4
	5kΩ to GND	Left Justified Mix or TDM Slot 5
	5kΩ to IOVDD	TDM Slot 6
	24kΩ to GND	TDM Slot 7
	1.2kΩ to GND	Left Justified Left Channel or TDM Slot 3
	0Ω to IOVDD	I^2S Mix or TDM Slot 2
	330Ω to IOVDD	I^2S Right Channel or TDM Slot 1
	0Ω to GND	I^2S Left Channel or TDM Slot 0
SEL3	0Ω to IOVDD	Rising edge of SBCLK
	0Ω to GND	Falling edge of SBCLK
SEL4	24kΩ to IOVDD	Address 0x94 or Y-Bridge Threshold 1mW
	0Ω to IOVDD	Address 0x96 or Y-Bridge Threshold 40mW
	24kΩ to GND	Address 0x92
	0Ω to GND	Address 0x90 or Y-Bridge Threshold 80mW

Table 2-2. Hardware Select Pin Resistor Values (continued)

Hardware Select Pin	Resistor Value	Description
SEL5	0Ω to GND	TAS2120: VBAT 1S Mode TAS2320: N/A
	24kΩ to IOVDD	TAS2120: VBAT 2S Mode TAS2320: N/A
	0Ω to IOVDD	TAS2120: External PVDD mode (2.5V to 14V) TAS2320: External PVDD mode (2.5V to 14V)

2.2 Reference Schematic

Figure 2-4 and Figure 2-4 show the schematic used in TAS2120EVM and TAS2320EVM, which is used to design the PCB described in the following sections.

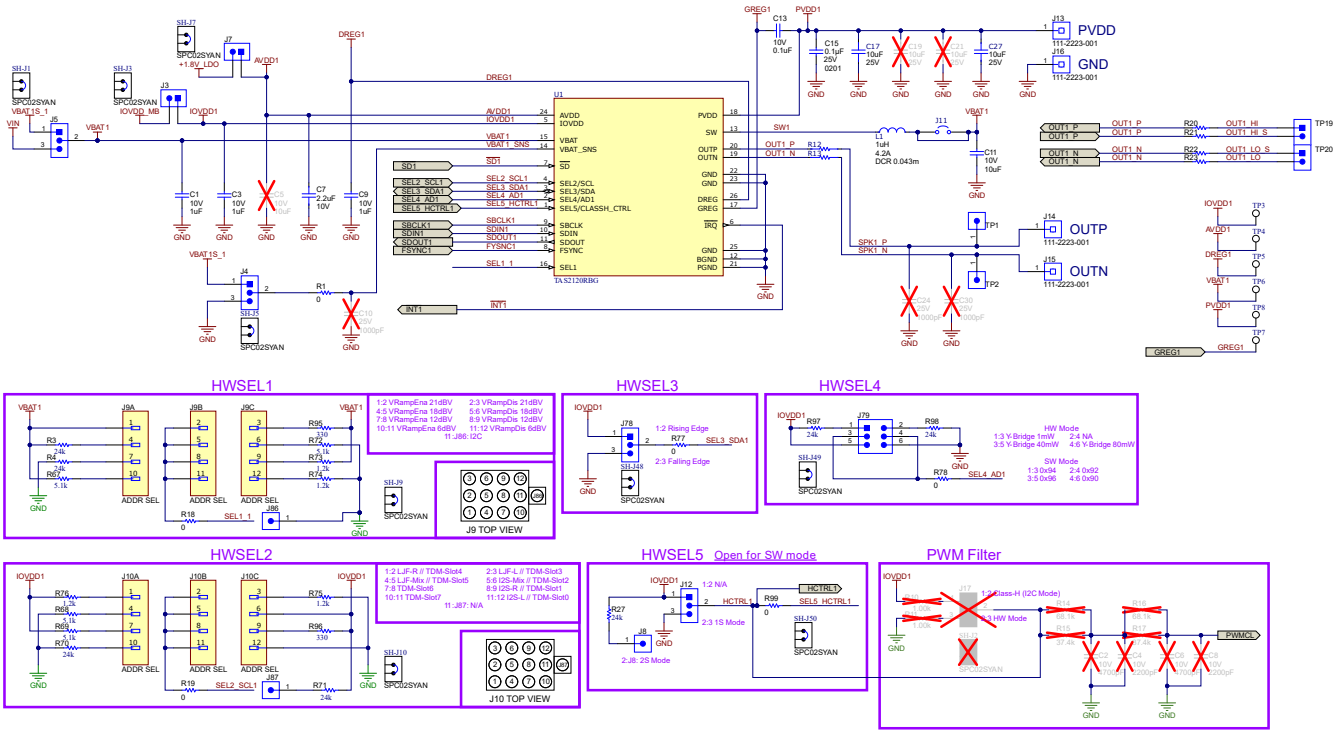

Figure 2-4. TAS2120EVM Reference Schematic

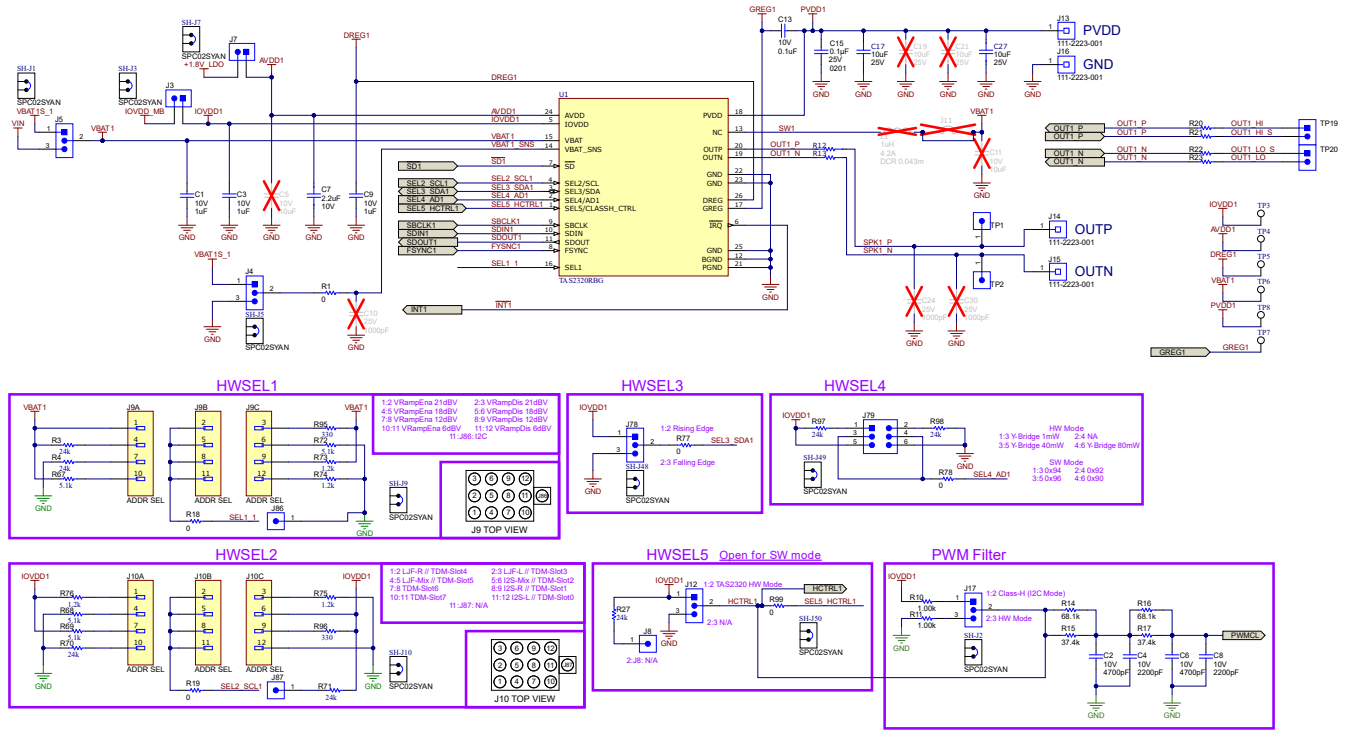

Figure 2-5. TAS2320EVM Reference Schematic

3 Design Guidelines

This section describes in detail the best layout practices to be followed for individual pin sections of the device.

3.1 VDD Pin

The VDD pin is used to power up various critical analog and digital blocks within the device. The VDD pin also acts as a power source for driving the Class-D output stage at lower power, if and when the device is operating in the Y-bridge mode.

The following guidelines need to be taken into account when routing the VDD pin to the corresponding power source on the PCB:

- When the Y-Bridge is enabled at power levels below the Y-Bridge threshold, the Class-D amplifier draws switching currents from the VDD pin. This current can be in the order of 200mA due to the fast edge rates.
- Any parasitic inductance in the path between the VDD pin and the corresponding power source results in significant voltage ripple on the pin, due to the L.dI/dT inductive kickback to the switching currents. This effect can potentially impact the performance and functionality of the device.
- Decoupling the VDD pin with a capacitor of value ≥ 2.2µF to the GND pin is recommended. This capacitor needs to be placed as close to the VDD pin as possible in the same layer.
- The decoupling capacitor must have the lowest possible parasitic inductance (ESL). Using a 0201 package capacitor is recommended.
- In case of space constraints in the PCB, place the capacitor such that the top plate connects directly to the VDD pin, and the bottom plate is connected to the PCB ground plane using multiple vias (a minimum of 3 vias is recommended).

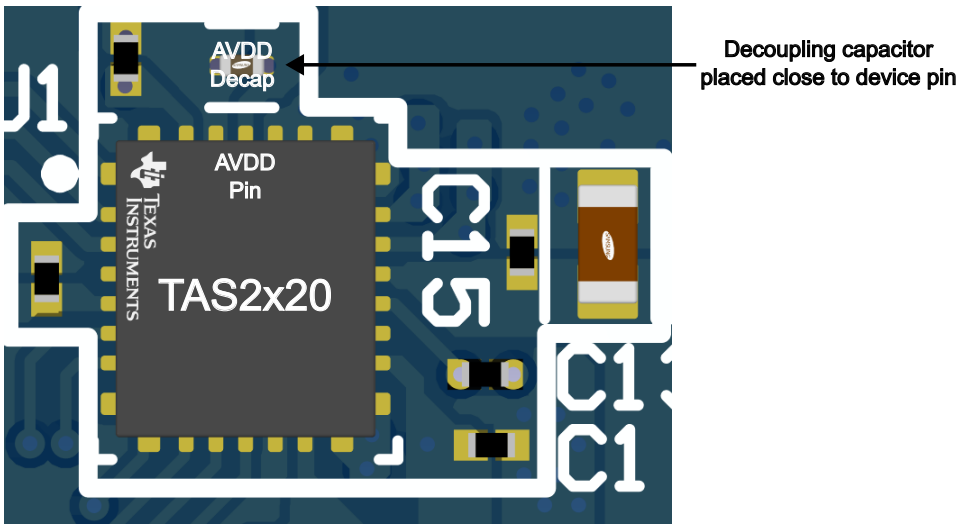

Figure 3-1. Placement of VDD Decoupling Capacitor

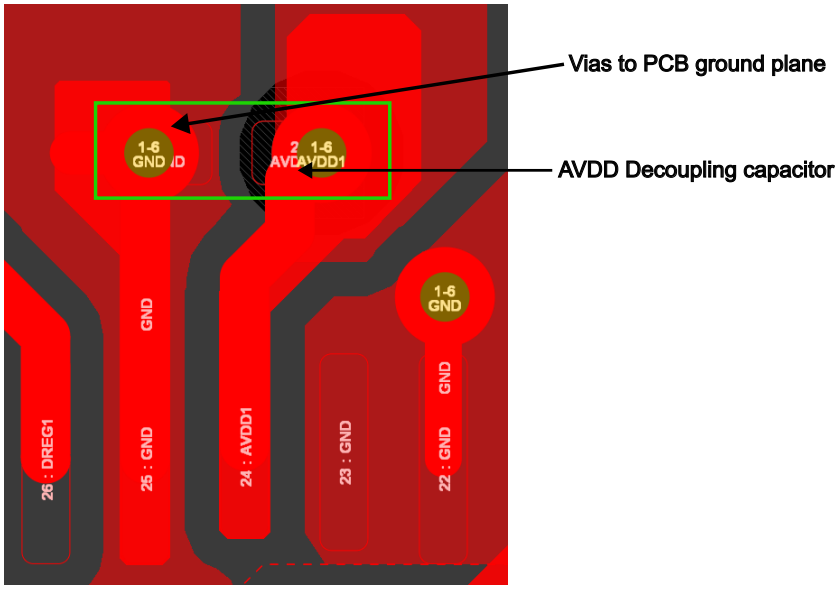

Figure 3-2. Routing from VDD

3.2 PVDD Pin

The PVDD pin correspond to the output of the internal boost converter. The PVDD pin also act as the power source for driving the Class-D output stage when the output power level is higher than the Y-Bridge threshold.

The following recommendations need to be taken into account when routing the PVDD pin on to the PCB:

- When the output power level is beyond the Y-Bridge threshold, the Class-D output stage draws high switching currents from the PVDD pin due to the fast edge rates.
- This pin must not be loaded through external circuitry when the device is operating with the boost converter.
- To minimize voltage ripple on the PVDD pin due to these transient currents, the PVDD pin must be bypassed with capacitors of value ≥ 2 x 22µF or ≥ 3 x 10µF.

  For PVDD<13V bypass capacitor can be reduced to 2 x 10µF or 1 x 22µF.
- This capacitance can see a level of derating due to:
  - Tolerance
  - Voltage coefficient near maximum PVDD voltage
- This derated capacitance must be at least 3µF at 13V.
- The PVDD pin also needs to be bypassed with a low-ESL capacitor (ESL must be ≤ 250pH) of 0.1µF, to minimize the loop inductance from PVDD to PGND. Use a 0201 package capacitor to achieve this bypass. The low-ESL capacitor must be placed as close to the device as possible.
- The decoupling capacitors need to be bypassed to the PGND pin. When bypassing through the PCB ground plane, use multiple vias (a minimum of three vias is recommended), to minimize parasitic inductance between the ground connection on the bypass capacitor and the PGND pin of the device.
- When operating in external PVDD mode, the PVDD pin needs to be connected to the power source using wide traces that are capable of carrying high current, and have low parasitic resistances, to minimize I^2R losses.

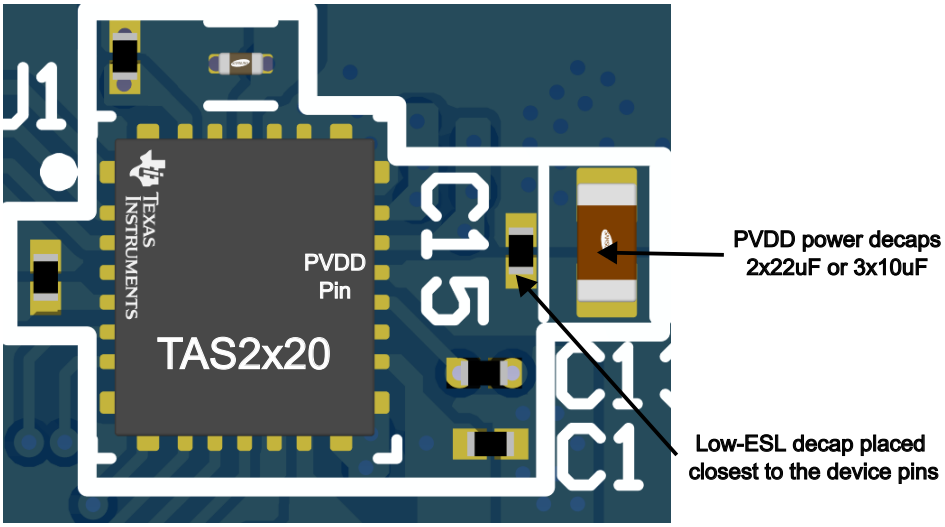

Figure 3-3. Placement of PVDD Decoupling Capacitors

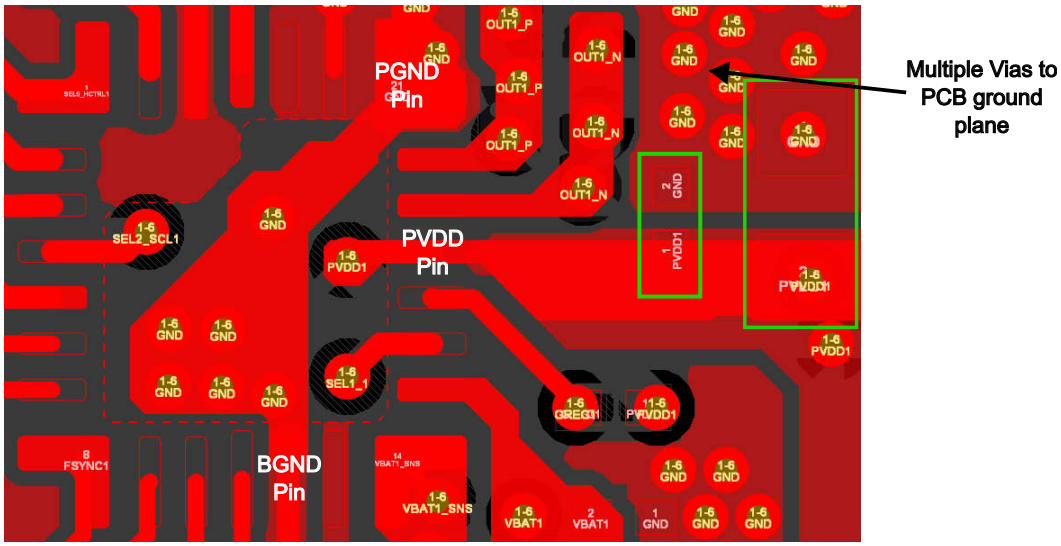

Figure 3-4. Routing From PVDD

3.3 GREG Pin

The GREG pin acts as the supply pin for the high-side gate drivers in the boost converter and the Class-D output stages. The GREG pin is powered using the voltage on the VBAT pin.

The following recommendations need to be taken into account when routing the GREG pin on to the PCB:

- The GREG pin needs to be decoupled to the PVDD pin using a capacitor of value 0.1µF (recommendation is to use a 0201 package to minimize ESL and ESR).
- The top plate needs to be connected to the GREG pin, and the bottom plate needs to use a star-connection directly to the PVDD pins, and not to the PVDD PCB plane or the top plate of the PVDD decoupling capacitor, to avoid common inductance to the PVDD pins.
- The voltage rating of the decoupling capacitor must be ≥ 6.3V.
- If the connection is made in inner PCB layers, use multiple vias to reduce parasitic inductance in the path.

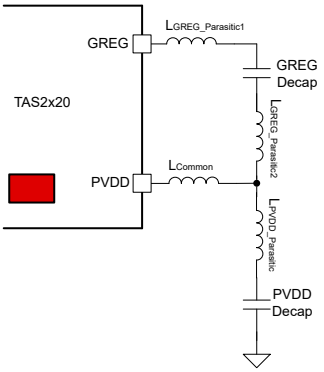

Figure 3-5. Incorrect Routing of GREG Decoupling Capacitor

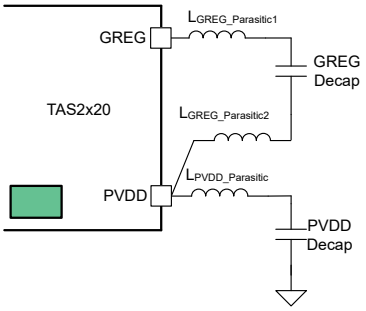

Figure 3-6. Correct Routing of GREG Decoupling Capacitor

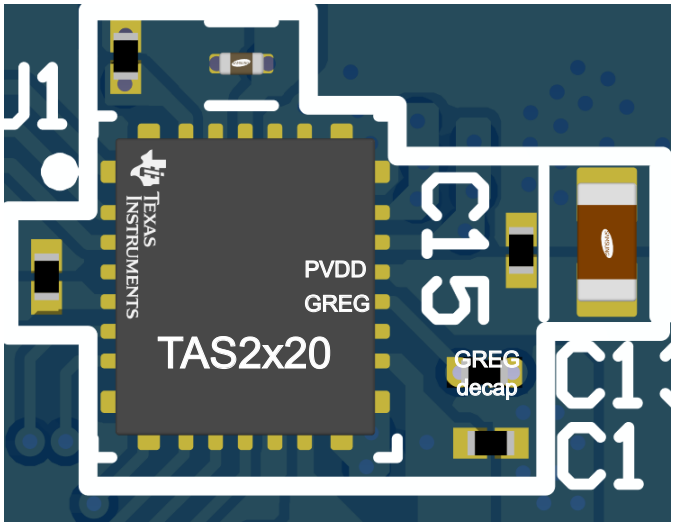

Figure 3-7. Placement of GREG Decoupling Capacitor on EVM

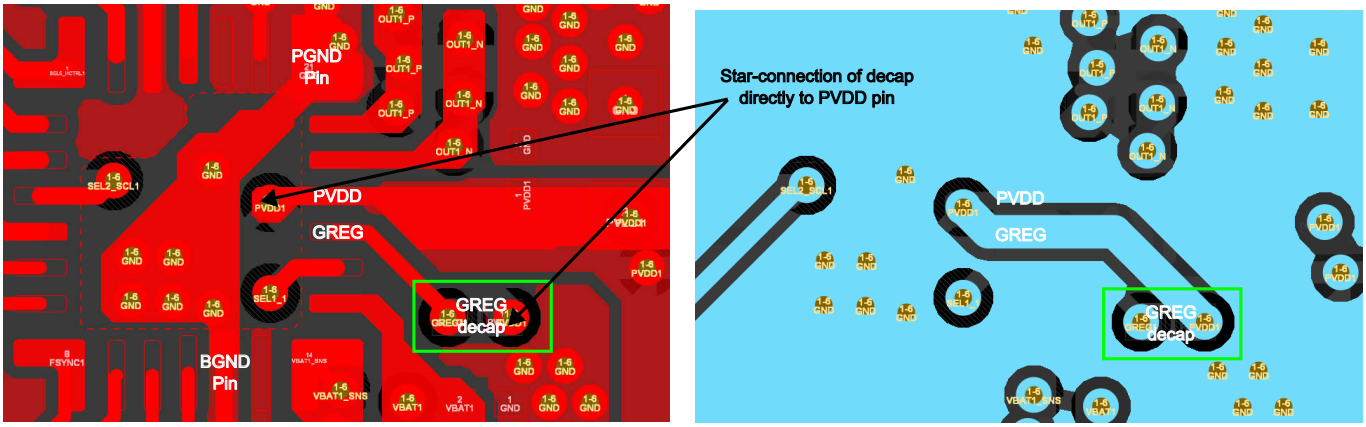

Figure 3-8. Connection of GREG Decoupling Capacitor to Inner Layer Using Vias

3.4 SW Pin

The SW pin correspond to the switching input to the internal boost converter of the device. The following recommendations need to be taken into account while routing the power source to the SW pin on the PCB:

- This node is expected to carry high transient current. The node needs to be routed with wide traces with high current carrying capability and minimal parasitic resistance and inductance.

- This node can switch at high voltages. Avoiding routing any low-voltage traces is recommended, including BCLK, FSYNC, SDIN SDOUT and more across this node to avoid coupling.
- Place the inductor that connects to the SW pin close to the device. Using inductors with lower ESR helps to achieve higher efficiency.
- The routing from the power source to the SW inductor must have minimal parasitic resistance to minimize efficiency impact from I^2R losses.
- Decouple the SW inductor with a capacitor of value ≥ 10µF, placed as close to the inductor as possible. This placement is meant to reduce ripple on the node stemming from transient currents. This capacitor must be placed between the power source and the inductor, and not between the inductor and the SW pin of the device.
- Minimize parasitic capacitance on the SW node path, to reduce switching losses, which impacts efficiency.
- When the device is operating in external PVDD mode, the SW pin must be left unconnected.

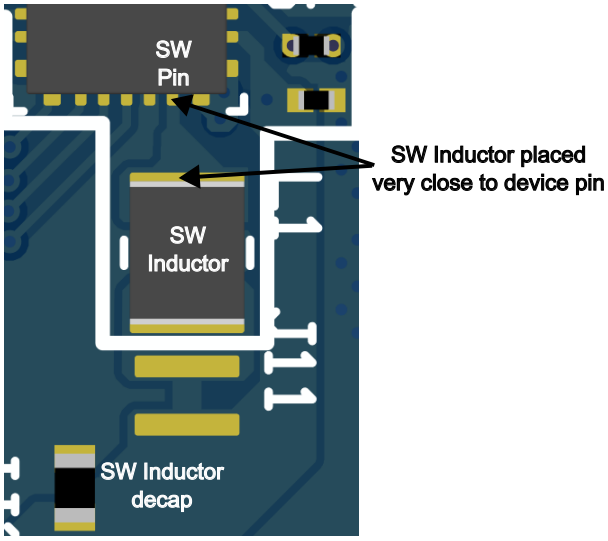

Figure 3-9. Placement of Boost Inductor and Decoupling Capacitor Near SW Pin

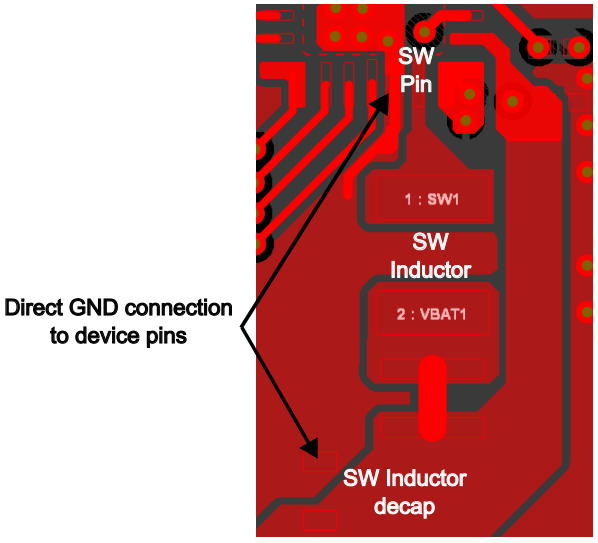

Figure 3-10. Routing of Power Source to SW Inductor

3.5 VBAT Pin

The VBAT pin acts as a device power supply pin, used to power up some of the internal analog blocks within the device. This pin also acts as a voltage sense pin when the device is configured to sense the supply voltage on

the VBAT pin. This pin is used for various battery monitoring decisions like voltage limiting, brown-out detection, boost turn-on, and more, especially in VBAT1S mode.

The following guidelines need to be taken into account while routing the VBAT pin on to the PCB:

- The VBAT pin carries a current up to 10mA. The trace routed to this pin can be narrower compared to the previously mentioned pins.
- The VBAT pin needs to be routed to the power source through a trace that is independent of the high current path used to route to the SW inductor.
- The VBAT pin needs to be decoupled to GND with a capacitor of value ≥ 1µF, that is placed as close to the device as possible. Using a 0201 package capacitor for lower ESL and ESR is recommended.
- The bottom plate of the capacitor, if connected to GND through the ground plane of the PCB, needs to be connected using multiple vias to minimize parasitic inductance to the GND pin.

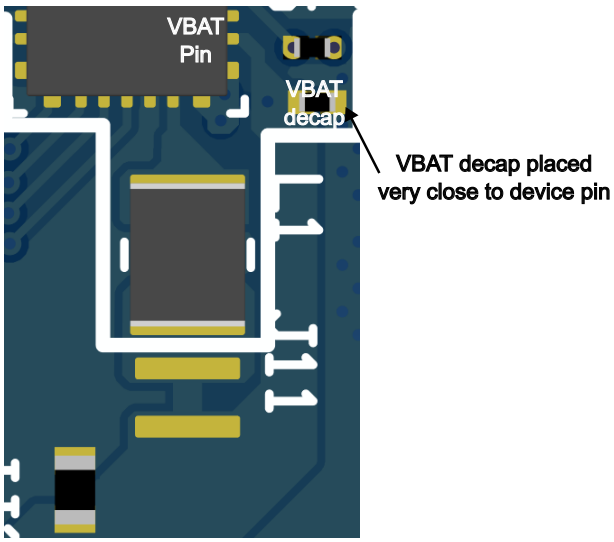

Figure 3-11. Placement of Decoupling Capacitor Near the VBAT Pin

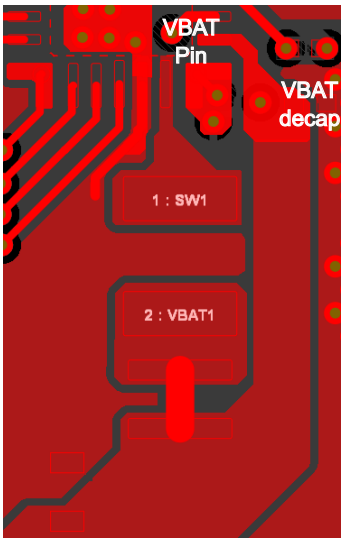

Figure 3-12. Routing of Power Source to VBAT Pin

3.6 OUT_P and OUT_N Pins

The OUT_P and OUT_N pins correspond to the differential output of the Class-D amplifier. The following guidelines need to be taken into account for routing these pins on the PCB:

- These pins switch from 0 - AVDD in Y-bridge mode, and 0 - PVDD when Y-bridge threshold is exceeded.

- This switching happens at fast edge rates, and results in high switching current at these nodes. Therefore these pins need to be routed to the speaker with wide traces capable of carrying high current.
- When the routing switches into inner layers of the PCB, multiple vias need to be used to provide current carrying capacity, and reduced parasitic inductance.
- The parasitic capacitance on these pins need to be kept to a minimum, since these parasitic capacitance results in increased switching losses, impacting efficiency. If the capacitance is high enough, the switching can also potentially trigger over-current interrupts.
- Since these nodes are high-voltage switching nodes, avoid routing any low-voltage nodes across this path, like BCLK, FSYNC, SDIN, SDOUT, and more, to avoid coupling.

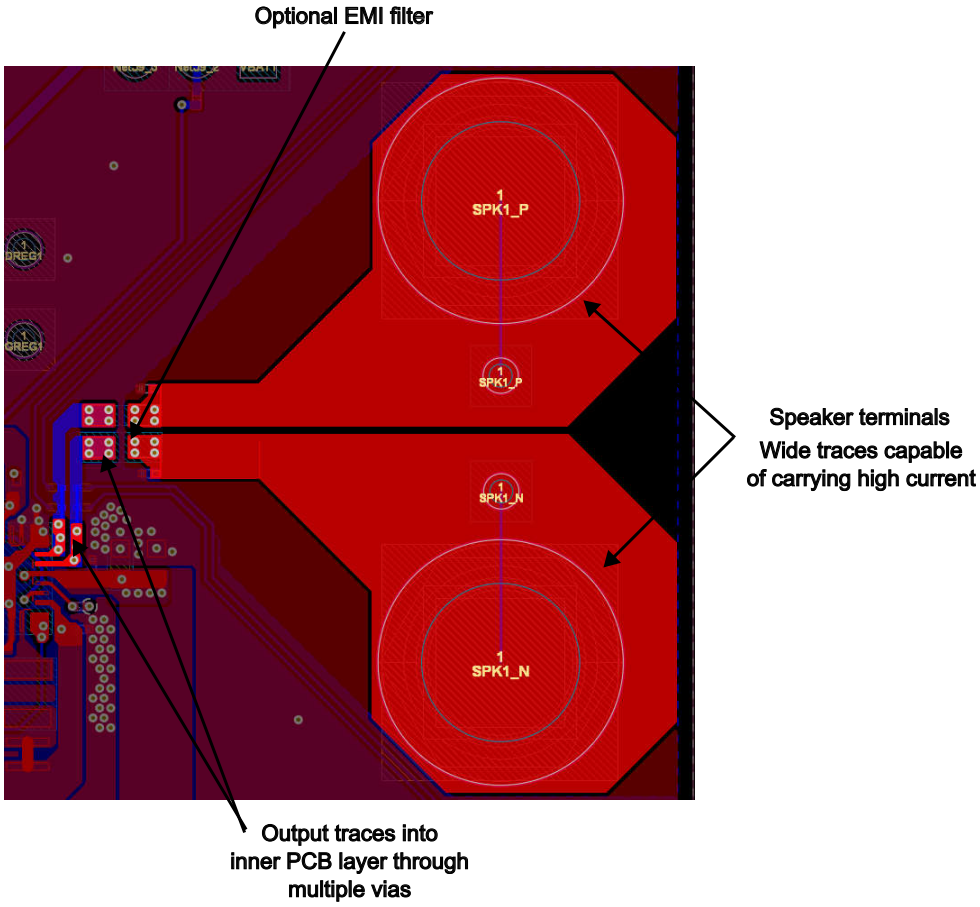

Figure 3-13. Routing of OUT_P/N to Speaker Terminals

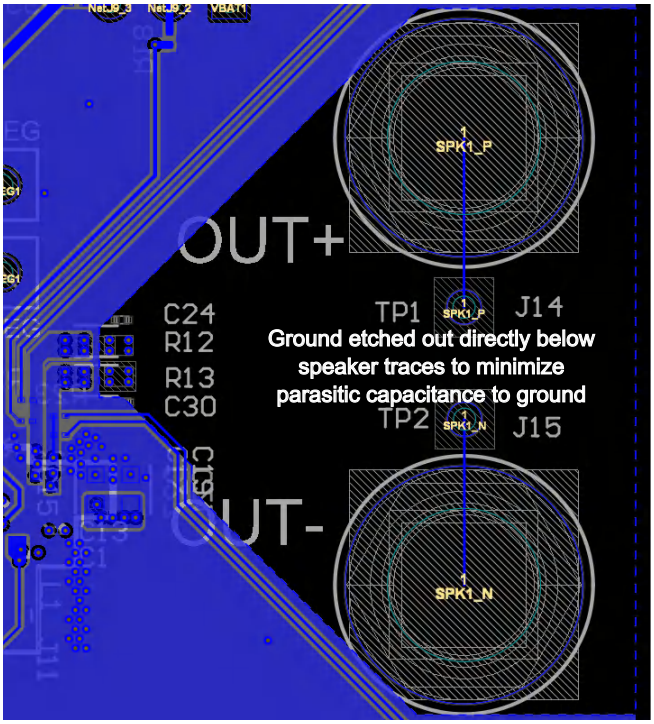

Figure 3-14. Routing Below OUT_P/N Paths in Inner PCB Layers

3.6.1 Optional EMI Filter on Output

The TAS2120 supports edge-rate control to minimize EMI, however the system designer can include passive EMI filter on the Class-D outputs if desired.

When using an EMI filter on the OUT_P or OUT_N pins, the following must be accounted for:

- The L - C cutoff frequency of the filter must be > 3MHz to avoid resonance with the Class-D switching frequency.
- The value of the capacitor, C, used in the filter must be selected, such that the (C / L) ratio is ≤ 1.5. This measure avoids false over-current interrupts during peak output power delivery.

3.7 IOVDD Pin

The IOVDD pin is the power supply pin for the digital I/Os of the device. The following recommendations need to be taken into account while routing the IOVDD pin on to the PCB:

- Decouple the IOVDD pin to GND using a capacitor of value ≥ 1µF, placed as close to the device as possible.

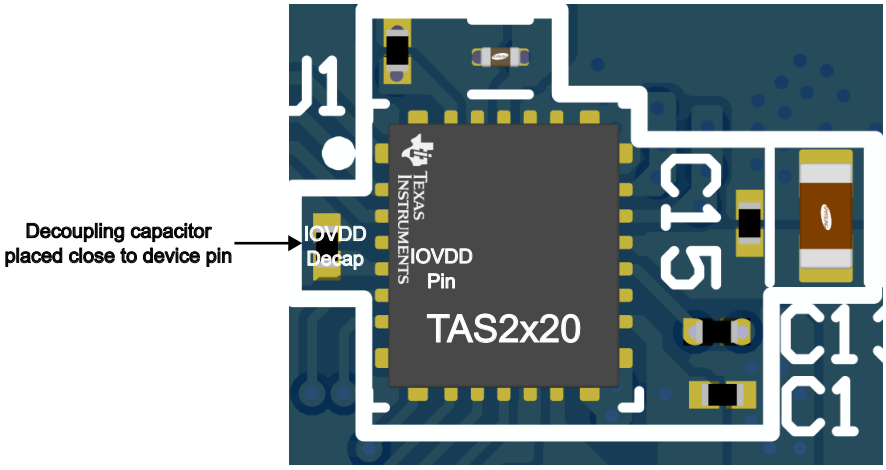

Figure 3-15. Placement of IOVDD Decoupling Capacitor

3.8 DREG Pin

The DREG pin corresponds to an internally generated LDO voltage. The DREG pin acts as a power supply for the internal digital blocks of the device. The following guidelines need to be taken into consideration while routing the DREG pin on to the PCB:

- The DREG pin must be decoupled to the GND pin with a capacitor of value ≥ 1µF. This capacitor needs to be placed as close to the device as possible. Use a 0201 capacitor to minimize ESR and ESL.
- The DREG pin must not be loaded by any external circuit.
- If decoupling through the ground plane of the PCB, use multiple vias to minimize parasitic inductance between the ground connection of the capacitor and the GND pin of the device.

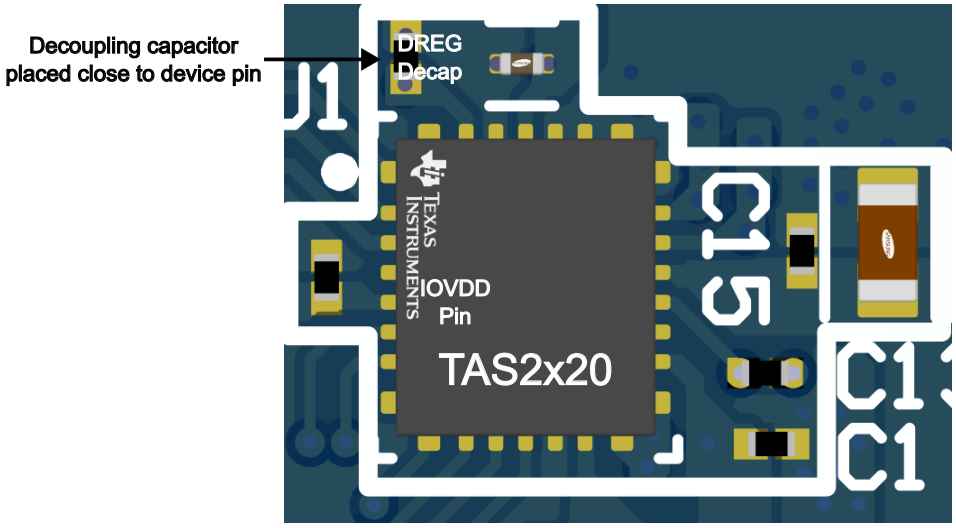

Figure 3-16. Placement of DREG Decoupling Capacitor

3.9 Digital I/O Pins

The device contains the following digital I/O pins, all referenced with respect to the IOVDD supply voltage:

- SEL1 for Hardware Mode selections
- SEL2_SCL, SEL3_SDA for I^2C communication to the device and Hardware Mode selections.
- SEL4_AD to set the I^2C device address and Hardware Mode selections.
- SEL5_CLASSH for Boost PWM control and Hardware Mode selections.
- SBCLK, FSYNC, SDIN, SDOUT for the TDM/I^2S audio serial interface.
- IRQz for the device interrupt.
- SDz for hardware shutdown of the device.

These digital pins need to be routed away from the high-voltage switching nodes (SW, OUT_P, OUT_N), to avoid any coupling, which can corrupt the integrity of the digital signals.

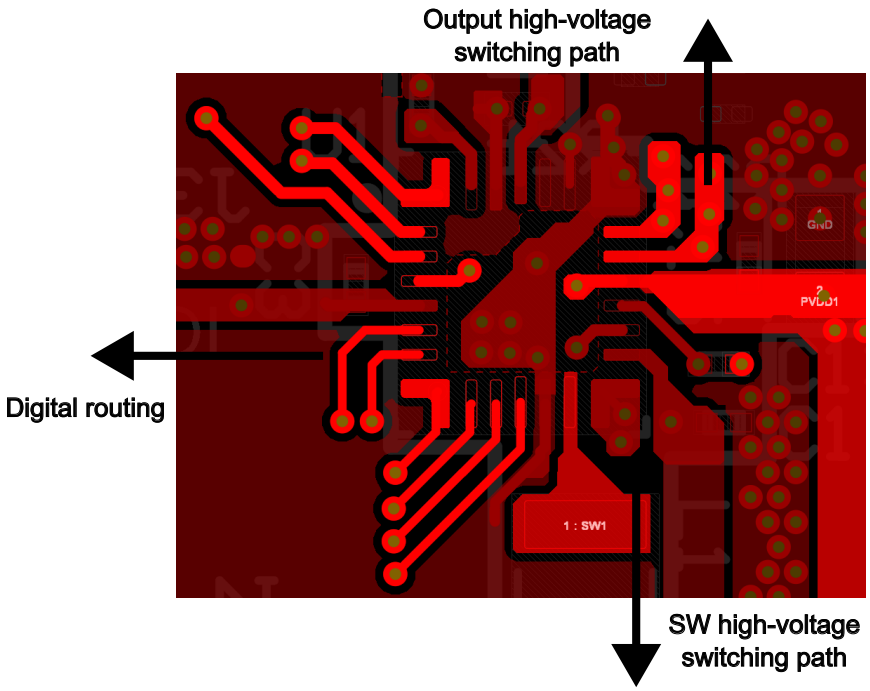

Figure 3-17. Routing of Digital Lines Away From the High-voltage Switching Lines

3.10 Ground Pins

The device contains multiple ground pins, which need to be connected to the ground planes in the PCB. While connecting the pins, the following guidelines must be taken into consideration:

- GND pin is used for the analog and digital grounds. This pin must to be connected independently to the PCB ground plane using vias. Avoid shorting this pin to other GND pins at the top layer, to avoid common inductance to PCB ground.
- BGND pin refers to the boost converter, and PGND pin refers to the Class-D power stage. These pins need to be shorted together on the top layer of the PCB, and then routed to the PCB ground plane using individual vias.
- Avoid shorting the BGND or PGND pins to the other GND pins of the device in the top layer, to avoid common inductance to the PCB ground.

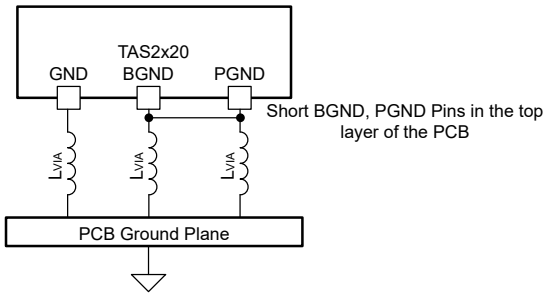

Figure 3-18. Connection of Ground Pins to PCB GND Plane

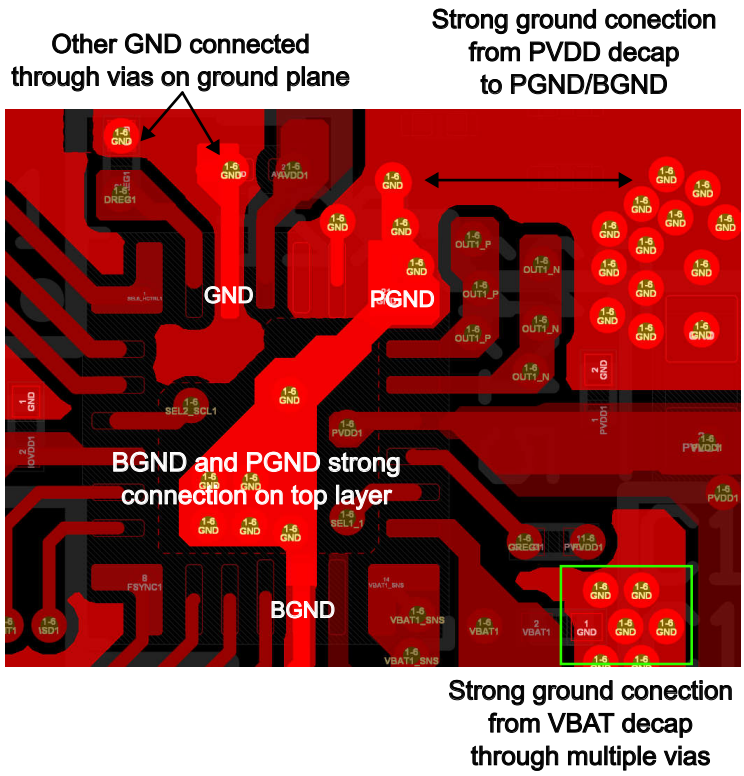

Figure 3-19. Connection of Device GND Pins

3.11 HW Selection Pins

TAS2X20 supports hardware control mode, which is controlled by a series of resistors connected to IOVDD, VBAT or GND depending on the required function as described in Table 2-2. These resistors must be placed as close to the IC as possible to reduce the parasitic capacitance between the IC pin and the resistor connection point. Follow the table below for specific tolerances for each of the resistor value cases.

Table 3-1. Component Ratings

BOM Resistors	Tolerance	Temp-co of R	Pin Capacitance
0Ω (direct short)	<10Ω short	N/A	<7.5pF (recommended) 15pF (max)
330Ω	±5% (recommended) ±10% (max)	<±400ppm/C	
1.2kΩ			
5kΩ			
24kΩ			

4 EMI Specific Guidelines

PCB layout design can considerably improve EMI performance. This section covers some recommendations to consider for EMI constrained applications.

The main source of radiated emissions produced from audio amplifiers is the output Class-D switching. Specifically for TAS2120 and TAS2320, the emissions can be lower at lower power as the Class-D switches from 0V up to the VDD voltage rail. As output power increases the emissions can do as well as the voltage rail swaps to PVDD. During PCB layout design consider the following recommendations to improve the radiated emissions performance.

- Output traces need to be routed using inner layers. GND shielding is recommended on top and bottom of the layer used for output traces.
- Use top or bottom layer only if using output filter components like ferrites or inductors and capacitors. Use multiple vias on pad, reduce the copper area on top or bottom layer as much as possible.
- TAS2120 and TAS2320 feature edge rate control for the Class-D output. For best EMI performance configure the edge rate to the slowest setting (0.5V/ns).
- If LC filter is needed for more EMI constrained systems, refer to the following documentation with further information on how to select the filter components:
  - LC Filter Design, application note.
  - LCFILTER-CALC-TOOL Class-D LC Filter Designer

5 Summary

Table 5-1 summarizes the recommended design and layout practices for the different pins of the device.

Table 5-1. Summarized Design and Layout Guidelines

Section	Pin or Section	Maximum Parasitic Trace Inductance (pH)	Recommended Guidelines
1	VDD	650	Decouple with a capacitor ≥ 2.2µF, placed as close to device as possible
2	PVDD	600	Decouple with capacitor 3 x 10µF or 2 x 22µF, placed as close as possible to device
			Needs small package 0.1µF capacitor (0201) placed closest to the device, with minimal ESL
			Account for derating due to PVDD voltage
			Wide traces with high current carrying capability
3	GREG	4000	Decouple with 0.1µF capacitor to PVDD pin
			Connect directly to PVDD pin with star connection
4	SW		Place inductor as close as possible to device
			Wide traces to carry high current and minimize parasitic resistance critical for efficiency (reduced I^2R losses)
			Decouple with ≥ 10µF capacitor near inductor
			Minimize parasitic capacitance to ground to reduce switching losses
			Leave pin unconnected in external PVDD mode
5	VBAT	950	Connect directly to power source using star connection
			Decouple with ≥ 1µF capacitor, placed as close as possible to device
5	VBAT_SNS		Connect directly to power source using star connection
			Optional connection in VBAT1S mode, connect to ground if unused
6	OUT_P / OUT_N		Decouple with ≥ 1µF capacitor, placed as close as possible to device
			Wide traces capable of carrying high current
			Minimize parasitic capacitance to ground to reduce switching losses
7	IOVDD		Can be shorted to VDD near the device pin if 1.8V is the required I/O supply. Recommended to use both C2 and C3 capacitors even when shorted, with the capacitors placed close to the VDD pin
8	DREG		Decouple with ≥ 1µF capacitor as close as possible to device
9	Digital		Avoid routing near high-voltage switching nodes like SW, OUT_P, OUT_N to avoid coupling
10	Ground		Short BGND or PGND pins on top layer
			Avoid common inductance to ground plane between PGND or BGND and GND pins
			Total parasitic inductance to PCB ground critical for device performance. Use multiple vias to minimize inductance
11	HW Selection Pins		Place HW setting resistors as close as possible to the IC. Parasitic capacitance after the resistor doesn't matter.

6 References

- Texas Instruments, *LC Filter Design*, application note.
- Texas Instruments, *LCFILTER-CALC-TOOL Class-D LC Filter Designer*, product page.
- Texas Instruments, *TAS2120 Evaluation Module*.
- Texas Instruments, *TAS2320 Evaluation Module*.

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