Application Note

Dynamic Voltage and Temperature Tracking Based Limiter in TAX5XXX-Q1

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ABSTRACT

The TAx5xxx-Q1 family of audio converters are used in automotive applications that can experience exposure to high temperature conditions and sudden fluctuations in battery supply voltage (VBAT). The TAx5xxx-Q1 generation of Texas Instruments' audio converters introduces a *Distortion Limiter*, *Brown-out Protector*, and *Thermal Foldback* feature that monitors battery voltage and die temperature levels. This monitor function helps protect the device from these adverse factors by automatically attenuating the output signal.

The *Distortion Limiter* reduces the peak of the output signal and the *Brown-out Protector* applies a constant gain reduction to the output signal as a function of supply voltage. In addition,*Thermal Foldback* automatically attenuates the output signal, by reducing the gain, if the temperature of the die exceeds a programmable limit while audio is still present at the output.

The *Distortion Limiter*, *Brown-out*, and *Thermal Foldback* features are algorithms within the limiter bank of the DAC signal chain present in TAx5xxx-Q1 devices. This application note describes how to configure these features for the following devices:

- TAC5411-Q1
- TAC5412-Q1
- TAC5311-Q1
- TAC5312-Q1
- TAC5212-Q1
- TAC5211-Q1
- TAC5111-Q1
- TAD5212-Q1

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1 Introduction

Maximizing efficiency in battery-powered applications is paramount for extending battery life and maintaining high-quality audio. Audio signals that approach the limits of the dynamic range of the DAC can create distortion in the output signal and audio clipping. TAx5xxx-Q1 devices mitigate the risk of distortion and improve power consumption by allowing the user to map VBAT to the output peak because the device is continuously monitoring the output signal level with the limiter bank algorithm.

A droop in VBAT reduces the supply headroom needed to prevent audio clipping and the ability of the device to supply current is limited when the battery voltage continues to decrease. If an audio converter continues to drive significant current into a speaker, or speaker amplifier, the system battery voltage can dip below normal system operating levels. This continuous dip in voltage can potentially cause electrical damage to devices sharing the same supply, or result in the system shutting down. This type of event is commonly known as *Brown Out*. Texas Instruments' audio option for this problem is to incorporate a *Brown-out Protector* and *Distortion Limiter* to reduce the peak or gain of the output signal. These features grant the user control over attenuation levels based on supply voltage, which effectively manages device power consumption.

Automotive audio applications require that devices are fully-operational in high ambient temperature conditions. This device family has an overtemperature detection circuit that can enable the shutdown of input channels, MICBIAS, and on-chip boost in the DAC_FLT_CFG (P1_R80) and INT_CFG register (P0_R66) upon fault detection. The *Thermal Foldback* feature attenuates the audio signal based on a programmed temperature limit with audio playing to further prevent damage to the device.

2 Signal Processing Chain

The *Limiter Bank* algorithm is a digital signal design present in the DAC signal path of the TAx5xxx-Q1 devices. This algorithm governs the *Distortion Limiter*, *Brown-out Protector*, and *Thermal Foldback* feature (Figure 2-1).

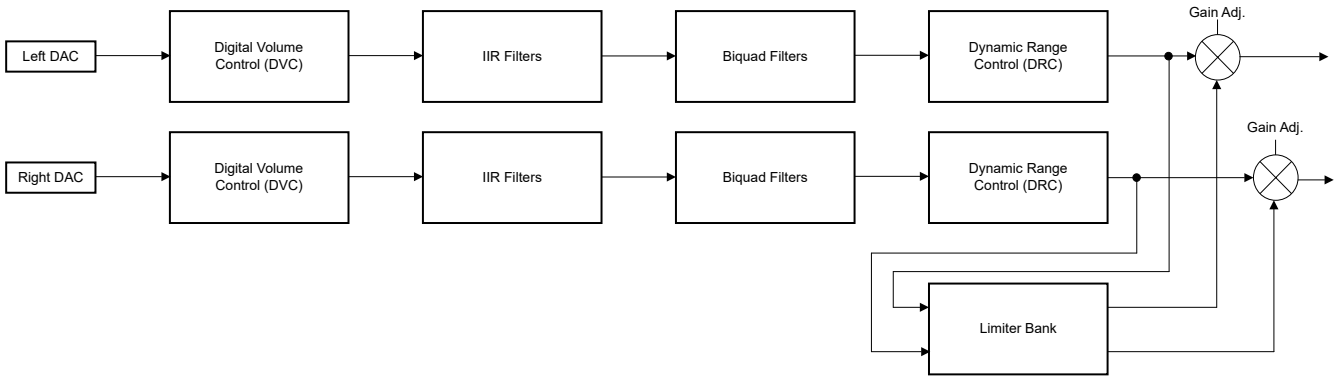

Figure 2-1. DAC Signal Chain

The left and right DAC channel signal levels are the inputs to the limiter bank. The user can select which signal is altered by the *Distortion Limiter* in the LIMITER_CFG (P1_R35_D6:7) register. The input MUX to the limiter bank can be configured to receive the max signal present, the left signal of the DAC channel, the right signal of the DAC channel, or the average signal level of both channels.

The limiter bank algorithm monitors the VBAT pin level and internal temperature of the die to apply changes to the left and right DAC channel output signal level. The user can activate or deactivate the *Distortion Limiter*, *Brown-out Protector* (BOP), and *Thermal Foldback* feature individually within the MISC_CFG0 register (P1_45).

The *Distortion Limiter* and BOP apply an attenuation to the output signal if VBAT is below the target level. These algorithms engage within the limiter bank as a function of VBAT, the default configuration, or AVDD by configuring the MISC_CFG0 (P1_R45_D1) and DIAG_CFG13 (P1_R83_D2) registers. *Thermal Foldback* attenuates the output signal if the temperature of the die exceeds the threshold governed by the coefficients on page 26 of the register map. Moreover, the limiter bank uses a small step-size during attack and release of the algorithm to reduce distortions in the input and output signal.

The limiter bank then applies the minimum of all gain adjustments made to the output signal of the DAC. The gain adjustments can be applied to both output channels, either channel individually, or none at all in the LIMITER_CFG (P1_R35_D4:5) register.

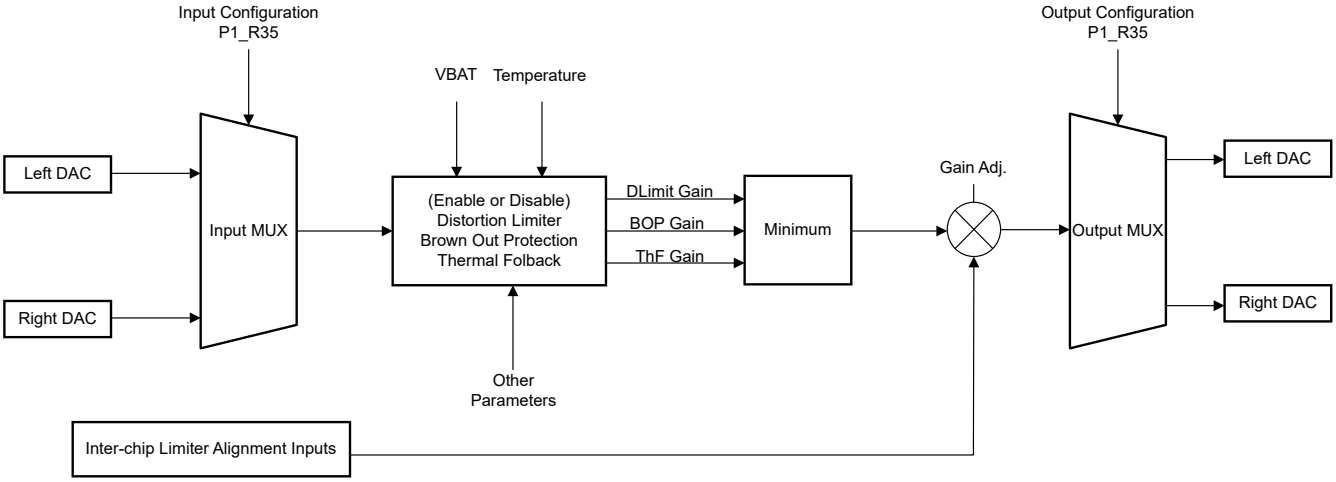

Figure 2-2. Limiter Bank Signal Chain

3 Distortion Limiter

The *Distortion Limiter* works by scaling down the output signal as a function of the battery voltage and input signal level. When VBAT or AVDD drops below the *inflection point*, the peak of the output signal is reduced from the *threshold maximum* to the *threshold minimum*. This feature is valuable when the battery level starts to drop during prolonged use and prevents more supply voltage than necessary being drained to achieve the desired peak output voltage. The gain is restored to the programmed operating condition once the supply recovers. This design prevents the output from exceeding the *threshold maximum* when the input signal increases to a level that exceeds the full-scale input signal range to prevent audio clipping.

The output signal for the TAx5xxx-Q1 family is up to 10Vrms differential and 5Vrms single-ended. The *Distortion Limiter* allows the user to configure the *threshold maximum* and *threshold minimum* values in dbFS and the *inflection point* of the supply voltage. Figure 3-1 displays how the configuration of the limiter block maps the battery voltage to the output peak.

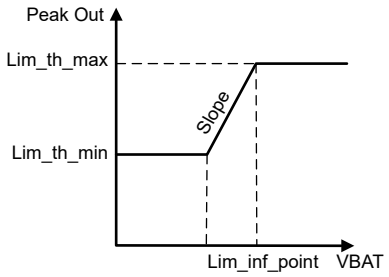

Figure 3-1. Distortion Limiter Output Configuration

Figure 3-2 highlights the response of the peak output signal as VBAT fluctuates. By default, the input:output signal ratio is 1:1 relative to full scale.

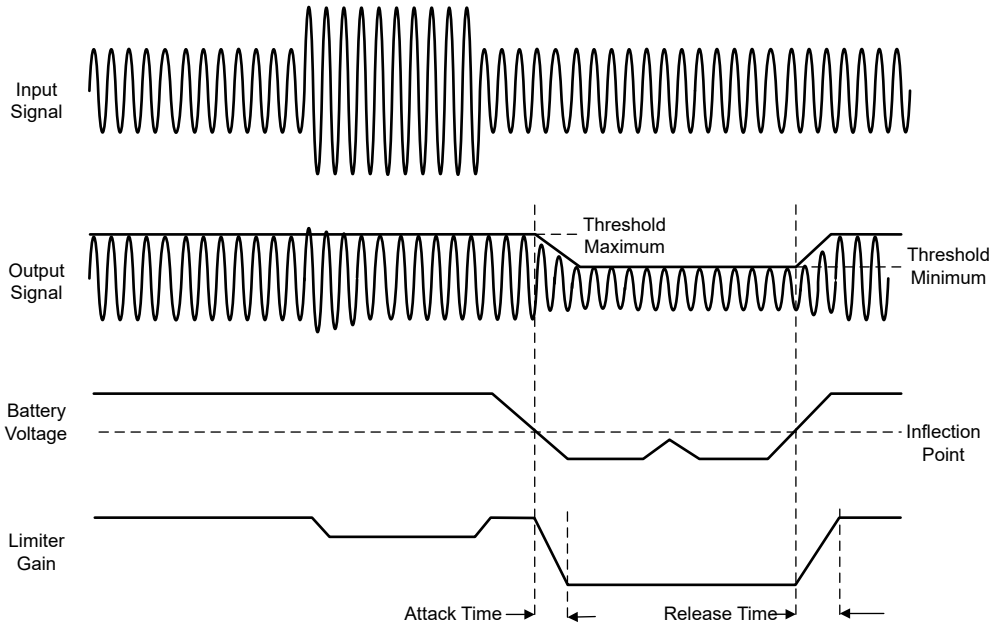

Figure 3-2. Distortion Limiter Example

The *Distortion Limiter* can be customized to end application power specifications without impacting the listening experience. Users can configure the parameters of the limiter to prioritize an extended battery life by restricting the output peak and reducing the gain gradually as VBAT decreases. Conversely, users can create a steeper slope when setting a lower VBAT inflection point threshold. A steeper slope emphasizes an audio signal range in low-battery voltage conditions.

3.1 Distortion Limiter Parameters

Table 3-1 shows the parameters of the *Distortion Limiter* algorithm. The parameters reside in the 32-bit-wide coefficient memory (page 25 registers) of the device.

Table 3-1. List of Distortion Limiter Parameters

Distortion Limiter Parameter	Function and Description
Threshold Maximum (dB)	The maximum peak output signal level, relative to full scale output voltage
Threshold Minimum (dB)	The minimum peak output signal the *Distortion Limiter* attenuates to
Inflection Point (V)	The battery level where the output peak begins to reduce below the *threshold maximum*
Slope (V/V)	The rate of output peak decrease from the *threshold maximum*
Attack Rate (dB/step)	The step rate response when the *Distortion Limiter* triggers a gain decrease
Release Rate (dB/step)	The step rate response when the *Distortion Limiter* triggers a gain increase
Hold Counter (ms)	The amount of time taken, following a change in VBAT, before the *Distortion Limiter* adjusts the output signal level

3.1.1 Threshold Maximum

The *threshold maximum* is the maximum peak output signal. The target level is expressed relative to full scale (dBFS) of the DAC output. This threshold is controlled by the coefficient YRAM_LIM_TH_MAX. Equation 1 shows how to compute the parameters from the desired dB value. The maximum peak range is from -50dB to 24dB and can be programmed in steps of 1x10^-6dB, where PO is the *peak output* level in dB.

$$\text{YRAM\_LIM\_THR\_MAX} = \text{round}\left(10^{((\text{PO}+3)/20)} \times 2^{24}\right) \quad (1)$$

Table 3-2 lists the registers corresponding to YRAM_LIM_TH_MAX. The default value (0x1699C0F) corresponds to 3dB.

Table 3-2. Programmable Coefficient Registers for Threshold Maximum

Coefficient	Page	Register	Reset Value	Description
yram_lim_th_max	0x19	0x6C	0x00	RDAC_SF1_BYT1[31:24]
yram_lim_th_max	0x19	0x6D	0x00	RDAC_SF1_BYT2[23:16]
yram_lim_th_max	0x19	0x6E	0x00	RDAC_SF1_BYT3[15:8]
yram_lim_th_max	0x19	0x6F	0x00	RDAC_SF1_BYT4[7:0]

3.1.2 Threshold Minimum

The *threshold minimum* is the minimum peak output signal the *Distortion Limiter* attenuates to. The target level is expressed relative to full scale (dBFS) of the DAC output. This threshold is controlled by the coefficient YRAM_LIM_TH_MIN. Equation 2 shows how to compute the parameters from the desired dB value. The maximum peak range is from -50dB to 24dB and can be programmed in steps of 1x10^-6dB, where MP is the *minimum peak* level of the signal in dB.

$$\text{YRAM\_LIM\_THR\_MIN} = \text{round}\left(10^{((\text{MP}+3)/20)} \times 2^{24}\right) \quad (2)$$

Table 3-3 lists the registers corresponding to YRAM_LIM_TH_MIN. The default value (0x007259DB) corresponds to -7dB.

Table 3-3. Programmable Coefficient Registers for Threshold Minimum

Coefficient	Page	Register	Reset Value	Description
YRAM_LIM_TH_MIN	0x19	0x70	0x00	LDAC_SF1_BYT1[31:24]
YRAM_LIM_TH_MIN	0x19	0x71	0x00	LDAC_SF1_BYT2[23:16]
YRAM_LIM_TH_MIN	0x19	0x72	0x00	LDAC_SF1_BYT3[15:8]
YRAM_LIM_TH_MIN	0x19	0x73	0x00	LDAC_SF1_BYT4[7:0]

3.1.3 Inflection Point

The *inflection point* sets the VBAT level where the *Distortion Limiter* begins to reduce the gain below the *threshold maximum*. The monitored level of VBAT must decrease below the *inflection point* for a period longer than the *hold counter*. This threshold is controlled by the coefficient YRAM_LIM_INF_PT. Equation 3 shows how to compute the parameters from the desired voltage value. The threshold range is from 0.01V to 15V and can be programmed in steps of 1x10^-6V, where V is the *voltage* level maximum in volts.

$$\text{YRAM\_LIM\_INF\_PT} = \text{round}\left(\text{V} \times 2^{11}\right) \quad (3)$$

Table 3-4 lists the registers corresponding to YRAM_LIM_INF_PT. The default value (0x0000199A) corresponds to 3.2V.

Table 3-4. Programmable Coefficient Registers for Inflection Point

Coefficient	Page	Register	Reset Value	Description
YRAM_LIM_INF_PT	0x19	0x74	0x00	RDAC2_SF1_BYT1[31:24]
YRAM_LIM_INF_PT	0x19	0x75	0x00	RDAC2_SF1_BYT2[23:16]
YRAM_LIM_INF_PT	0x19	0x76	0x00	RDAC2_SF1_BYT3[15:8]

3.1.4 Slope

The *slope* is the rate the output peak decreases from the *threshold maximum* as a function of the drop in battery voltage. The programmable slope decreases the peak output power level in V/V as the battery voltage decreases. This threshold is controlled by the coefficient YRAM_LIM_SLOPE. Equation 4 shows how to compute the parameters from the desired slope in volts/volt. The threshold range is from 1V/V to 7.99V/V and can be programmed in steps of 1x10^-6V, where S is the slope in V/V.

$$\text{YRAM\_LIM\_SLOPE} = \text{round}\left(S \times 2^{28}\right) \quad (4)$$

Table 3-5 lists the registers corresponding to YRAM_LIM_SLOPE. The default value (0x10000000) corresponds to 1V/V.

Table 3-5. Programmable Coefficient Registers for Slope

Coefficient	Page	Register	Reset Value	Description
YRAM_LIM_SLOPE	0x19	0x78	0x00	ASIOUT_BUF_VARS_BYT1[31:24]
YRAM_LIM_SLOPE	0x19	0x79	0x00	ASIOUT_BUF_VARS_BYT2[23:16]
YRAM_LIM_SLOPE	0x19	0x7A	0x00	ASIOUT_BUF_VARS_BYT3[15:8]
YRAM_LIM_SLOPE	0x19	0x7B	0x00	ASIOUT_BUF_VARS_BYT4[7:0]

3.1.5 Attack Rate

The *attack rate* is the step rate response when the *Distortion Limiter* triggers a gain decrease. The settling time of the signal is faster as this rate increases. This threshold is controlled by the coefficient YRAM_ATTACK_COEFFI_LIM. Equation 5 shows how to compute the parameters from the desired attenuation rate in dB/step. The threshold range is from -6dB/step to 0dB/step and can be programmed in steps of 1x10^-6dB, where AR is the *attenuation rate* of the output signal in dB/step.

$$\text{YRAM\_ATTACK\_COEFFI\_LIM} = \text{round}\left(10^{(\text{AR}/20)} \times 2^{31}\right) \quad (5)$$

Table 3-6 lists the registers corresponding to YRAM_ATTACK_COEFFI_LIM. The default value (0x78D6FC9F) corresponds to -0.5dB/step.

Table 3-6. Programmable Coefficient Registers for Attack Rate

Coefficient	Page	Register	Reset Value	Description
YRAM_ATTACK_COEFFI_LIM	0x19	0x60	0x00	ADC_CH3_SF1_BYT1[31:24]
YRAM_ATTACK_COEFFI_LIM	0x19	0x61	0x00	ADC_CH3_SF1_BYT2[23:16]
YRAM_ATTACK_COEFFI_LIM	0x19	0x62	0x00	ADC_CH3_SF1_BYT3[15:8]
YRAM_ATTACK_COEFFI_LIM	0x19	0x63	0x00	ADC_CH3_SF1_BYT4[7:0]

3.1.6 Release Rate

The *release rate* is the step rate response when the *Distortion Limiter* triggers a gain increase. The settling time of the signal is faster as this user-defined rate increases. This threshold is controlled by the coefficient YRAM_REL_COEFFI_LIM. Equation 6 shows how to compute the parameters from the desired attenuation rate in dB/step. The threshold range is from -1x10^6dB/step to 6dB/step and can be programmed in steps of 1x10^-6dB, where RR is the *Release Rate* of the output signal in dB/step.

$$\text{YRAM\_REL\_COEFFI\_LIM} = \text{round}\left(10^{(\text{RR}/20)} \times 2^{30}\right) \quad (6)$$

Table 3-7 lists the registers corresponding to YRAM_REL_COEFFI_LIM. The default value (0x40BDB7C0) corresponds to 0.1dB/step.

Table 3-7. Programmable Coefficient Registers for Release Rate

Coefficient	Page	Register	Reset Value	Description
YRAM_REL_COEFFI_LIM	0x19	0x64	0x00	ADC_CH4_SF1_BYT1[31:24]
YRAM_REL_COEFFI_LIM	0x19	0x65	0x00	ADC_CH4_SF1_BYT2[23:16]
YRAM_REL_COEFFI_LIM	0x19	0x66	0x00	ADC_CH4_SF1_BYT3[15:8]
YRAM_REL_COEFFI_LIM	0x19	0x67	0x00	ADC_CH4_SF1_BYT4[7:0]

3.1.7 Hold Counter

The *hold counter* is the amount of time taken following a change in VBAT before the *Distortion Limiter* adjusts the output signal level and engages the *Distortion Limiter*. This threshold is controlled by the coefficient YRAM_RESET_COUNTER_LIM. Equation 7 shows how to compute the parameters from the desired attenuation rate in milliseconds. The threshold range is from 1ms to 1000ms and can be programmed in 1ms steps, where T is the *Time* in milliseconds before the *Distortion Limiter* is active.

$$\text{YRAM\_RESET\_COUNTER\_LIM} = \text{round}\left(\text{T} \times 2^{0}\right) \tag{7}$$

Table 3-8 lists the registers corresponding to YRAM_RESET_COUNTER_LIM. The default value (0x00000060) corresponds to 2 milliseconds.

Table 3-8. Programmable Coefficient Registers for Hold Counter

Coefficient	Page	Register	Reset Value	Description
YRAM_RESET_COUNTER_LIM	0x19	0x7C	0x00	ASIOUT_BUF_VARS_BYT1[31:24]
YRAM_RESET_COUNTER_LIM	0x19	0x7D	0x00	ASIOUT_BUF_VARS_BYT2[23:16]
YRAM_RESET_COUNTER_LIM	0x19	0x7E	0x00	ASIOUT_BUF_VARS_BYT3[15:8]
YRAM_RESET_COUNTER_LIM	0x19	0x7F	0x00	ASIOUT_BUF_VARS_BYT4[7:0]

3.2 Limiter Response

The settings for the *Distortion Limiter* validation, shown in Figure 3-3, can be programmed through direct I²C communication and are configurable in the PurePath™ Console 3 software.

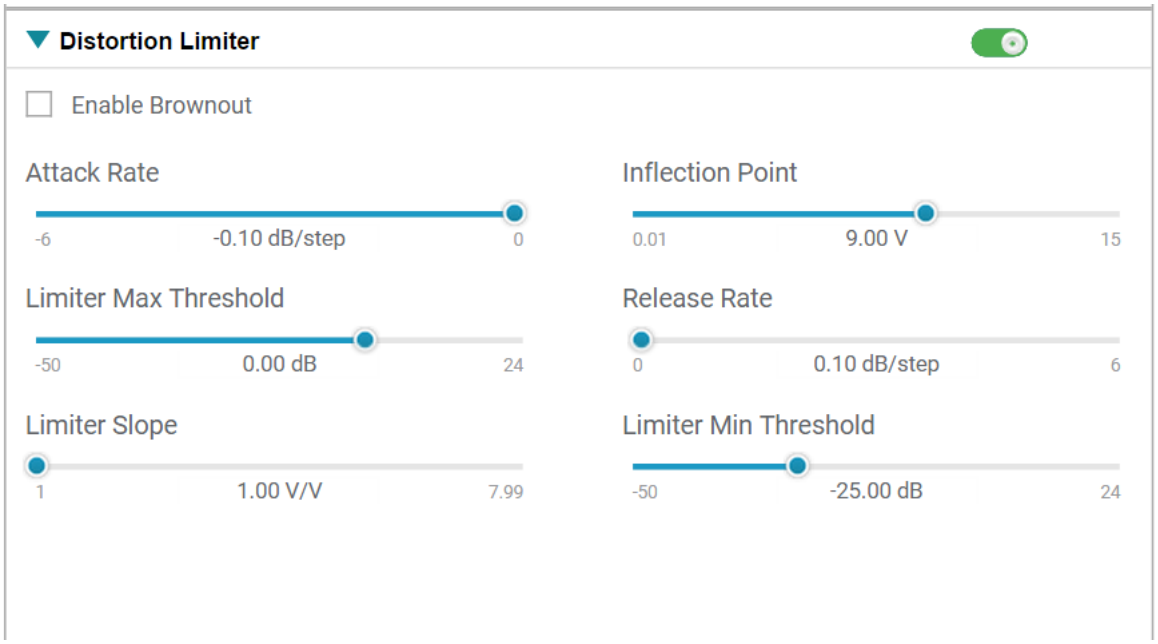

Figure 3-3. Distortion Limiter PPC3 Configuration

An example of the limiter actively adjusting the gain is represented in the scope capture of Figure 3-4. In this example, VBAT, provided by a bench top supply and represented on Channel two is ramped down over time causing the limiter to engage. Prior to the inflection point, the output signal on Channel one is a full-scale 2Vrms signal attenuated to approximately 120mVrms as VBAT drops.

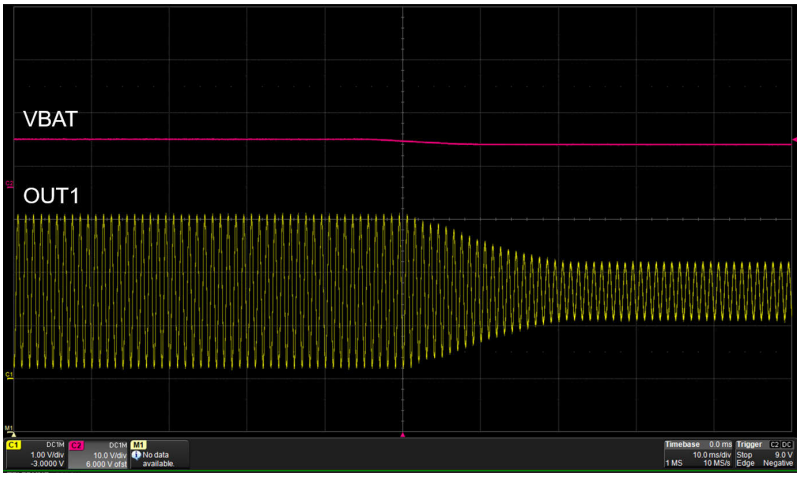

Figure 3-4. Distortion Limiter Attack Profile

Figure 3-5 is an example of the attack and release rate of the limiter engaging as VBAT drops and suddenly ramps back to a level above the inflection point.

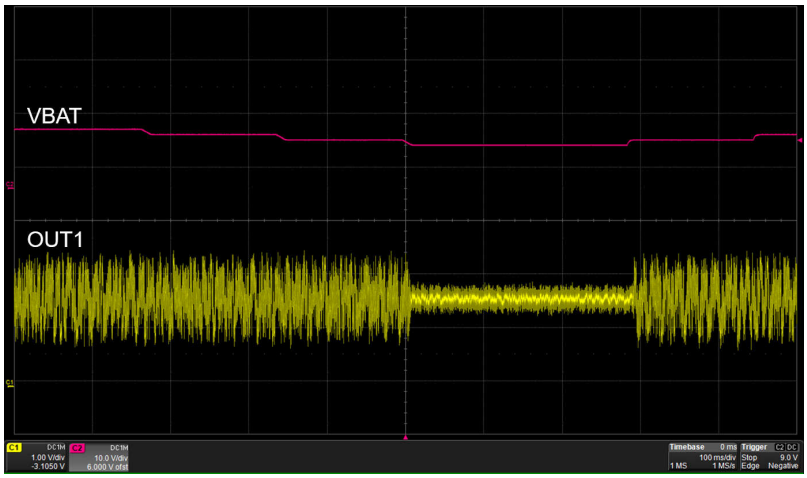

Figure 3-5. Distortion Limiter Two-Stage Response

4 Brown-Out Protection

The *Brown-out* protection technique works by applying a constant attenuation to the output signal based on user-defined critical VBAT levels. The degree of attenuation and critical VBAT levels are programmed and applied to the signal path irrespective of the audio input signal. This feature is valuable when the user wants the output signal to reduce to a defined signal level in the event there is a sudden drop in battery voltage. The output signal can increase back to the original state as the battery voltage recovers and is greater than the critical level parameters. Figure 4-1 displays how the configuration of this block attenuates the output signal as a function of battery voltage level.

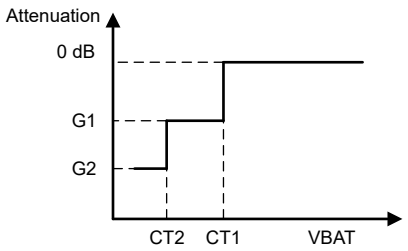

Figure 4-1. BOP Output Configuration

Figure 4-2 shows the response of the *Brown-out* protection block as VBAT surpasses or regresses VBAT critical levels.

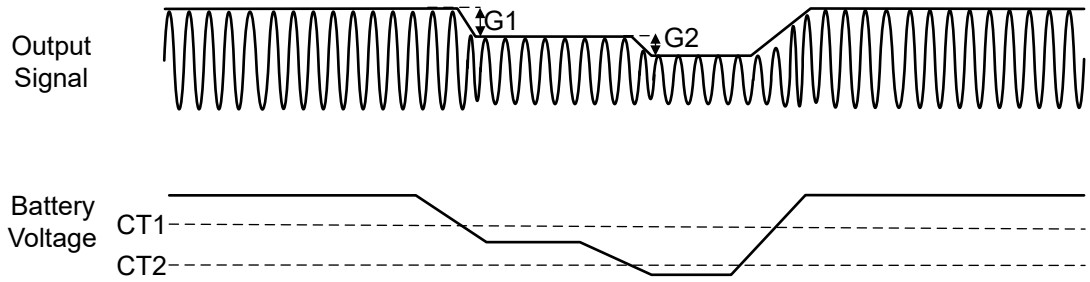

Figure 4-2. Brown-Out Protection Example

An attenuation of Gain Level 1 (G1) is applied to the output signal if VBAT is less than Critical Level 1 (CT1) and greater than Critical Level 2 (CT2). The output signal is reduced to the level of G2 if VBAT is less than CT1 and CT2. The *Brown-out* protection block gains up the output signal to the defined peak output as VBAT recovers.

4.1 Brown-Out Protection Parameters

Table 4-1 shows the parameters of the *Brown-out* protection algorithm. The parameters reside in the 32-bit-wide coefficient memory (Book 0, page 26) of the device.

Table 4-1. List of Brown-Out Protection Parameters

Brown-Out Parameter	Function and Description
Critical Level (V)	A user-defined VBAT level parameter to initiate a gain increase or decrease to the output signal
Gain Level (dB)	The amount of gain applied to the output signal level when a critical VBAT level is triggered
Attack Rate (dB/step)	The step rate response when the BOP triggers a gain decrease
Release Rate (dB/step)	The step rate response when the BOP triggers a gain increase
Hold Counter (ms)	The amount of time taken following a change in VBAT before the brown-out protector attenuates the output signal level

4.1.1 Critical Level

The *critical level* is a user-defined VBAT level parameter to initiate a gain increase or decrease to the output signal. This upper and lower threshold is controlled by the coefficients YRAM_VSUP_TH1 and YRAM_VSUP_TH2 respectively. Equation 8 shows how to compute the parameters from the desired voltage value. The threshold range is from 0.01V to 15V and can be programmed in steps of 1x10^-6V, where VS is the battery *voltage supply* critical level.

$$\text{YRAM\_VSUP\_TH}(1/2) = \text{round}(\text{VS} \times 2^{11}) \tag{8}$$

Table 4-2 lists the registers corresponding to YRAM_VSUP_TH(1/2). The default value for threshold 1 (0x0000199A) corresponds to 3.2V and the default value for threshold 2 (0x00001666) corresponds to 2.8V.

Table 4-2. Programmable Coefficient Registers for Critical Levels

Coefficient	Page	Register	Reset Value	Description
YRAM_VSUP_TH1	0x1A	0x20	0x00	ASIOUT_BUF_VARS_BYT1[31:24]
	0x1A	0x21	0x00	ASIOUT_BUF_VARS_BYT2[23:16]
	0x1A	0x22	0x00	ASIOUT_BUF_VARS_BYT3[15:8]
	0x1A	0x23	0x00	ASIOUT_BUF_VARS_BYT4[7:0]
YRAM_VSUP_TH2	0x1A	0x28	0x00	ASIOUT_BUF_VARS_BYT1[31:24]
	0x1A	0x29	0x00	ASIOUT_BUF_VARS_BYT2[23:16]
	0x1A	0x2A	0x00	ASIOUT_BUF_VARS_BYT3[15:8]
	0x1A	0x2B	0x00	ASIOUT_BUF_VARS_BYT4[7:0]

4.1.2 Gain Level

The *gain level* is the amount of gain applied to the output signal level when a *critical level* is triggered. The value of gain decrease is constant and dependent on where the monitored VBAT level falls relative to the critical level thresholds. This upper and lower threshold is controlled by the coefficients YRAM_BOP_TH1 and YRAM_BOP_TH2 respectively. Equation 9 shows how to compute the parameters for the desired constant gain adjustment value. The threshold range is from -1x10^-6dB to 0dB and can be programmed in steps of 1x10^-6dB, where GL is the *gain* level decrease in dB applied to the output signal.

$$\text{YRAM\_BOP\_TH}\left(1/2\right) = \text{round}\left(10^{\text{GL}/20} \times 2^{30}\right) \tag{9}$$

Table 4-3 lists the registers corresponding to YRAM_BOP_TH(1/2). The default value for threshold 1 (0x2D4EFBD6) corresponds to -3dB and the default value for threshold 2 (0x143D1362) corresponds to -10dB.

Table 4-3. Programmable Coefficient Registers for Gain Levels

Coefficient	Page	Register	Reset Value	Description
YRAM_BOP_TH1	0x1A	0x24	0x00	ASIOUT_BUF_VARS_BYT1[31:24]
	0x1A	0x25	0x00	ASIOUT_BUF_VARS_BYT2[23:16]
	0x1A	0x26	0x00	ASIOUT_BUF_VARS_BYT3[15:8]
	0x1A	0x27	0x00	ASIOUT_BUF_VARS_BYT4[7:0]
YRAM_BOP_TH2	0x1A	0x2C	0x00	ASIOUT_BUF_VARS_BYT1[31:24]
	0x1A	0x2D	0x00	ASIOUT_BUF_VARS_BYT2[23:16]
	0x1A	0x2E	0x00	ASIOUT_BUF_VARS_BYT3[15:8]
	0x1A	0x2F	0x00	ASIOUT_BUF_VARS_BYT4[7:0]

4.1.3 Attack Rate

The *attack rate* is the step rate response when the *Brown-out Protector* triggers a gain decrease. The settling time of the signal is faster as this user-defined rate increases. This threshold is controlled by the coefficient YRAM_ATTACK_COEFFI_BOP. Equation 10 shows how to compute the parameters from the desired attenuation rate in dB/step. The threshold range is from -6dB/step to 0dB/step and can be programmed in steps of 1x10^-6dB, where AR is the *attack rate* on the output signal in dB/step.

$$\text{YRAM\_ATTACK\_COEFFI\_BOP} = \text{round}\left(10^{\text{AR}/20} \times 2^{31}\right) \tag{10}$$

Table 4-4 lists the registers corresponding to YRAM_ATTACK_COEFFI_BOP. The default value (0x78D6FC9F) corresponds to -0.5dB/step.

Table 4-4. Programmable Coefficient Registers for Attack Rate

Coefficient	Page	Register	Reset Value	Description
YRAM_ATTACK_COEFFI_BOP	0x1A	0x14	0x00	ASIOUT_BUF_VARS_BYT1[31:24]
YRAM_ATTACK_COEFFI_BOP	0x1A	0x15	0x00	ASIOUT_BUF_VARS_BYT2[23:16]
YRAM_ATTACK_COEFFI_BOP	0x1A	0x16	0x00	ASIOUT_BUF_VARS_BYT3[15:8]
YRAM_ATTACK_COEFFI_BOP	0x1A	0x17	0x00	ASIOUT_BUF_VARS_BYT4[7:0]

4.1.4 Release Rate

The *release rate* is thestep rate response when the *Brown-out Protector* triggers a gain increase. The settling time of the signal is faster as this user-defined rate increases. This threshold is controlled by the coefficient YRAM_REL_COEFFI_BOP. Equation 11 shows how to compute the parameters from the desired attenuation rate in dB/step. The threshold range is from -1x10^6dB/step to 6dB/step and can be programmed in steps of 1x10^-6dB, where RR is the *release rate* on the output signal in dB/step.

$$\text{YRAM\_REL\_COEFFI\_BOP} = \text{round}\left(10^{\text{RR}/20} \times 2^{30}\right) \tag{11}$$

Table 4-5 lists the registers corresponding to YRAM_REL_COEFFI_LIM. The default value (0x40BDB7C0) corresponds to 0.1dB/step.

Table 4-5. Programmable Coefficient Registers for Release Rate

Coefficient	Page	Register	Reset Value	Description
YRAM_REL_COEFFI_BOP	0x1A	0x18	0x00	ASIOUT_BUF_VARS_BYT1[31:24]
YRAM_REL_COEFFI_BOP	0x1A	0x19	0x00	ASIOUT_BUF_VARS_BYT2[23:16]
YRAM_REL_COEFFI_BOP	0x1A	0x1A	0x00	ASIOUT_BUF_VARS_BYT3[15:8]
YRAM_REL_COEFFI_BOP	0x1A	0x1B	0x00	ASIOUT_BUF_VARS_BYT4[7:0]

4.1.5 Hold Counter

The *hold counter* is the amount of time taken following a change in VBAT before the *Brown-out Protector* attenuates the output signal level. This threshold is controlled by the coefficient YRAM_RESET_COUNTER_BOP. Equation 12 shows how to compute the parameters from the desired hold rate in milliseconds. The threshold range is from 1ms to 1000ms and can be programmed in 1ms steps, where T is the *time* in milliseconds before the *Brown-out* protection block is active.

$$\text{YRAM\_RESET\_COUNTER\_BOP} = \text{round}\left(\text{T} \times 2^{0}\right) \tag{12}$$

Table 4-6 lists the registers corresponding to YRAM_RESET_COUNTER_LIM. The default value (0x00000060) corresponds to 2 milliseconds.

Table 4-6. Programmable Coefficient Registers for Hold Counter

Coefficient	Page	Register	Reset Value	Description
YRAM_RESET_COUNTER_BOP	0x1A	0x1C	0x00	ASIOUT_BUF_VARS_BYT1[31:24]
YRAM_RESET_COUNTER_BOP	0x1A	0x1D	0x00	ASIOUT_BUF_VARS_BYT2[23:16]
YRAM_RESET_COUNTER_BOP	0x1A	0x1E	0x00	ASIOUT_BUF_VARS_BYT3[15:8]
YRAM_RESET_COUNTER_BOP	0x1A	0x1F	0x00	ASIOUT_BUF_VARS_BYT4[7:0]

4.2 Brown-Out Protection Response

Figure 4-3 is an example of the BOP algorithm engaging with the following parameters:

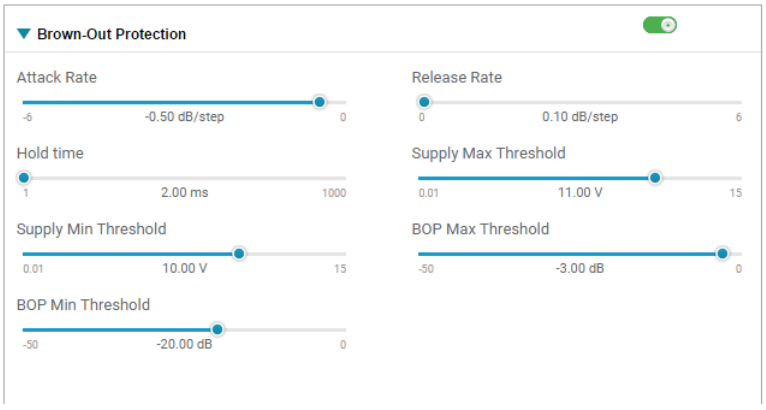

Figure 4-3. BOP PPC3 Configuration

Figure 4-4 features an incoming audio signal subject to the parameters of the BOP algorithm. VBAT is dropping from 11V to 10V at the first negative edge of channel two and subsequently the analog output is attenuated to a -3dB signal. As VBAT continues to drop below 10V the output further attenuates to the BOP minimum threshold, a -20dB signal.

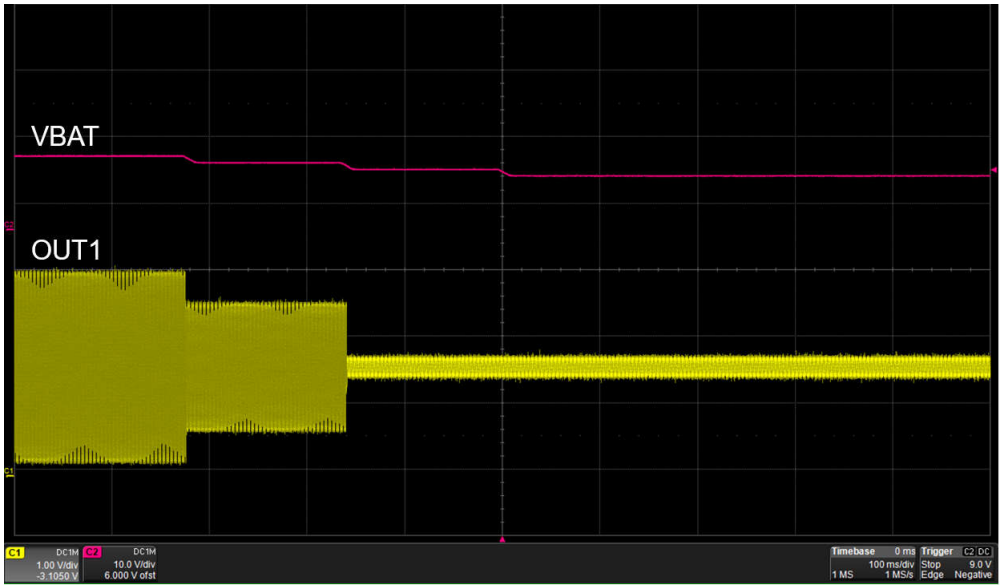

Figure 4-4. Two Stage BOP Response

5 Thermal Foldback

An attenuation is applied to the output signal when the temperature of the die exceeds the user-defined threshold. The user defines the slope, max attenuation, and temperature threshold for this block, as shown in Figure 5-1. After enabling *Thermal Foldback*, the temperature can be monitored in DIAG_MON_MSB_TEMP (P0_R106) and DIAG_MON_LSB_TEMP registers (P0_R107_D7:4). The 12-bit hexadecimal must be converted to a decimal and then used in Equation 13 to compute the temperature in degrees Celsius.

$$Temperature(°C) = 408.815605 - 0.1225435506 \times (Read\_data) \quad (13)$$

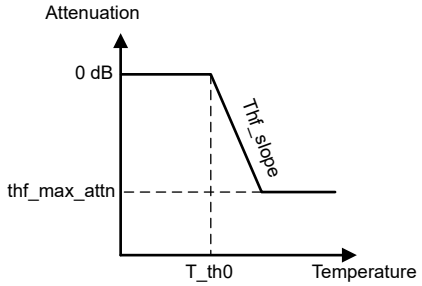

Figure 5-1. Thermal Foldback Output Configuration

Figure 5-2 demonstrates that the user-defined max attenuation is applied to the signal and slope and the signal decreases as a function of temperature.

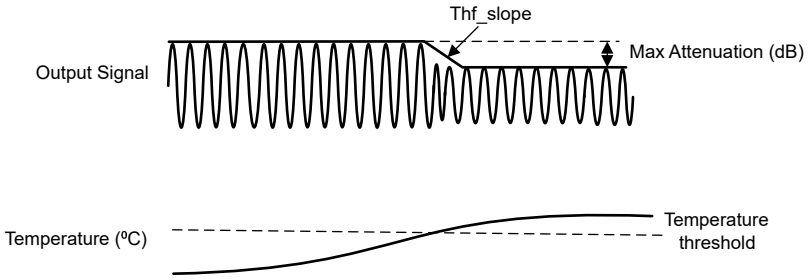

Figure 5-2. Thermal Foldback Example

5.1 Thermal Foldback Parameters

Table 5-1 shows the parameters of the *Thermal Foldback* algorithm. The parameters reside in the 32-bit-wide coefficient memory (Book 0, page 26) of the device.

Table 5-1. Thermal Foldback Parameters

Thermal Foldback Parameter	Function and Description
Temperature Threshold (deg)	A user-defined temperature level parameter, that if exceeded, applies a gain decrease to the output signal
Maximum Attenuation Threshold (dB)	The maximum amount of attenuation applied to the output signal if the temperature threshold is triggered
Slope (dB/deg)	The rate in dB, per degree attenuation, applied to the output signal until max attenuation level is reached
Attack Coefficient (dB/step)	The step rate response when *Thermal Foldback* triggers a gain decrease
Release Coefficient (dB/step)	The step rate response when *Thermal Foldback* triggers a gain increase
Hold Counter (ms)	The amount of time taken following a change in VBAT before the *Thermal Foldback* block attenuates the output signal level

5.1.1 Temperature Threshold

The *temperature threshold* is a user-defined temperature level parameter that applies a gain decrease to the output signal if the temperature threshold is exceeded. This threshold is controlled by the coefficient YRAM_TEMP_TH. Equation 14 shows how to compute the parameters from the desired temperature in degrees Celsius. The threshold range is from 0°C to 255°C and can be programmed in one-degree steps, where T is the *temperature threshold* in degrees Celsius.

$$\text{YRAM\_TEMP\_TH} = \text{round}\left(\text{T} \times 2^{7}\right) \tag{14}$$

Table 5-2 lists the registers corresponding to YRAM_TEMP_TH. The default value (0x00002380) corresponds to 71°C.

Table 5-2. Programmable Coefficient Registers for Temperature Threshold

Coefficient	Page	Register	Reset Value	Description
YRAM_TEMP_TH	0x1A	0x3C	0x00	ASIOUT_BUF_VARS_BYT1[31:24]
YRAM_TEMP_TH	0x1A	0x3D	0x00	ASIOUT_BUF_VARS_BYT2[23:16]
YRAM_TEMP_TH	0x1A	0x3E	0x00	ASIOUT_BUF_VARS_BYT3[15:8]
YRAM_TEMP_TH	0x1A	0x3F	0x00	ASIOUT_BUF_VARS_BYT4[7:0]

5.1.2 Maximum Attenuation Threshold

The *maximum attenuation threshold* is the maximum amount of attenuation applied to the output signal if the *temperature threshold* is triggered. This threshold is controlled by the coefficient YRAM_GAIN_MAX_ATTN_THF. Equation 15 shows how to compute the parameters from the desired maximum attenuation applied in dB. The threshold range is from 0dB to -70dB and can be programmed in 1dB steps, where MA is the *maximum attenuation* level in dB.

$$\text{YRAM\_GAIN\_MAX\_ATTN\_THF} = \text{round}\left(10^{\text{MA}/20} \times 2^{31}\right) \quad (15)$$

Table 5-3 lists the registers corresponding to YRAM_GAIN_MAX_ATTN_THF. The default value (0x2D6A866F) corresponds to -9dB.

Table 5-3. Programmable Coefficient Registers for Maximum Attenuation

Coefficient	Page	Register	Reset Value	Description
YRAM_GAIN_MAX_ATTN_THF	0x1A	0x40	0x00	ASIOUT_BUF_VARS_BYT1[31:24]
YRAM_GAIN_MAX_ATTN_THF	0x1A	0x41	0x00	ASIOUT_BUF_VARS_BYT2[23:16]
YRAM_GAIN_MAX_ATTN_THF	0x1A	0x42	0x00	ASIOUT_BUF_VARS_BYT3[15:8]
YRAM_GAIN_MAX_ATTN_THF	0x1A	0x43	0x00	ASIOUT_BUF_VARS_BYT4[7:0]

5.1.3 Slope

The *slope* is the rate in dB per degree attenuation applied to the output signal until *max attenuation* level is reached. This threshold is controlled by the coefficient YRAM_THF_SLOPE. Equation 16 shows how to compute the parameters from the desired slope in dB/degree. The threshold range is from -0.01dB/°C to -8dB/°C and can be programmed in steps of 1x10^-4V, where S is the *slope* in V/V.

$$\text{YRAM\_LIM\_SLOPE} = \text{round}\left(\text{S} \times 2^{28}\right) \quad (16)$$

Table 5-4 lists the registers corresponding to YRAM_THF_SLOPE. The default value (0xE0000000) corresponds to -2dB/deg.

Table 5-4. Programmable Coefficient Registers for Slope

Coefficient	Page	Register	Reset Value	Description
YRAM_THF_SLOPE	0x1A	0x44	0x00	ASIOUT_BUF_VARS_BYT1[31:24]
YRAM_THF_SLOPE	0x1A	0x45	0x00	ASIOUT_BUF_VARS_BYT2[23:16]
YRAM_THF_SLOPE	0x1A	0x46	0x00	ASIOUT_BUF_VARS_BYT3[15:8]
YRAM_THF_SLOPE	0x1A	0x47	0x00	ASIOUT_BUF_VARS_BYT4[7:0]

5.1.4 Attack Coefficient

The *attack coefficient* is the step rate response when *Thermal Foldback* triggers a gain decrease. The settling time of the signal is faster as this user-defined rate increases. This threshold is controlled by the coefficient YRAM_ATTACK_COEFFI_THF. Equation 17 shows how to compute the parameters from the desired attenuation rate in dB/step. The threshold range is from -6dB/step to 0dB/step and can be programmed in steps of 1x10^-6, where AR is the *attack rate* on the output signal in dB/step.

$$\text{YRAM\_ATTACK\_COEFFI\_THF} = \text{round}\left(10^{\text{AR}/20} \times 2^{31}\right) \quad (17)$$

Table 5-5 lists the registers corresponding to YRAM_ATTACK_COEFFI_THF. The default value (0x78D6FC9F) corresponds to -0.5dB/step.

Table 5-5. Programmable Coefficient Registers for Attack Rate

Coefficient	Page	Register	Reset Value	Description
YRAM_ATTACK_COEFFI_THF	0x1A	0x30	0x00	ASIOUT_BUF_VARS_BYT1[31:24]
YRAM_ATTACK_COEFFI_THF	0x1A	0x31	0x00	ASIOUT_BUF_VARS_BYT2[23:16]
YRAM_ATTACK_COEFFI_THF	0x1A	0x32	0x00	ASIOUT_BUF_VARS_BYT3[15:8]
YRAM_ATTACK_COEFFI_THF	0x1A	0x33	0x00	ASIOUT_BUF_VARS_BYT4[7:0]

5.1.5 Release Coefficient

The *release coefficient* is the step rate response when *Thermal Foldback* triggers a gain increase. The settling time of the signal is faster as this user-defined rate increases. This threshold is controlled by the coefficient YRAM_REL_COEFFI_THF. Equation 18 shows how to compute the parameters from the desired attenuation rate in dB/step. The threshold range is from -1x10^6dB/step to 6dB/step and can be programmed in steps of 1x10^-6, where RR is the *attack rate* on the output signal in dB/step.

$$\text{YRAM\_REL\_COEFFI\_THF} = \text{round}\left(10^{\text{RR}/20} \times 2^{30}\right) \tag{18}$$

Table 5-6 lists the registers corresponding to YRAM_REL_COEFFI_THF. The default value (0x40BDB7C0) corresponds to 0.1dB/step.

Table 5-6. Programmable Coefficient Registers for Release Rate

Coefficient	Page	Register	Reset Value	Description
YRAM_REL_COEFFI_THF	0x1A	0x34	0x00	ASIOUT_BUF_VARS_BYT1[31:24]
YRAM_REL_COEFFI_THF	0x1A	0x35	0x00	ASIOUT_BUF_VARS_BYT2[23:16]
YRAM_REL_COEFFI_THF	0x1A	0x36	0x00	ASIOUT_BUF_VARS_BYT3[15:8]
YRAM_REL_COEFFI_THF	0x1A	0x37	0x00	ASIOUT_BUF_VARS_BYT4[7:0]

5.1.6 Hold Counter

The *hold counter* is the amount of time taken following a change in temperature before the *Thermal Foldback* block attenuates the output signal level. This threshold is controlled by the coefficient YRAM_RESET_COUNTER_THF. Equation 19 shows how to compute the parameters from the desired hold rate in milliseconds. The threshold range is from 1ms to 1000ms and can be programmed in 1ms steps, where T is the *time* in milliseconds before the *Brown-out* protection block is active.

$$\text{YRAM\_RESET\_COUNTER\_THF} = \text{round}\left(\text{T} \times 2^{0}\right) \tag{19}$$

Table 5-7 lists the registers corresponding to YRAM_RESET_COUNTER_THF. The default value (0x00000060) corresponds to 2 milliseconds.

Table 5-7. Programmable Coefficient Registers for Hold Counter

Coefficient	Page	Register	Reset Value	Description
YRAM_RESET_COUNTER_THF	0x1A	0x38	0x00	ASIOUT_BUF_VARS_BYT1[31:24]
YRAM_RESET_COUNTER_THF	0x1A	0x39	0x00	ASIOUT_BUF_VARS_BYT2[23:16]
YRAM_RESET_COUNTER_THF	0x1A	0x3A	0x00	ASIOUT_BUF_VARS_BYT3[15:8]
YRAM_RESET_COUNTER_THF	0x1A	0x3B	0x00	ASIOUT_BUF_VARS_BYT4[7:0]

5.1.6.1 Thermal Foldback Response

For this test, the *Thermal Foldback* is enabled with a temperature threshold of 50°C and an initial die temperature of 28°C is observed using the temperature monitoring registers. A hot air stream is used to heat up the device. As the hot air is applied to the device, the temperature rises above the temperature threshold, thus triggering the *Thermal Foldback* algorithm to apply an output attenuation. Figure 5-3 shows the PPC3 parameters for the following example.

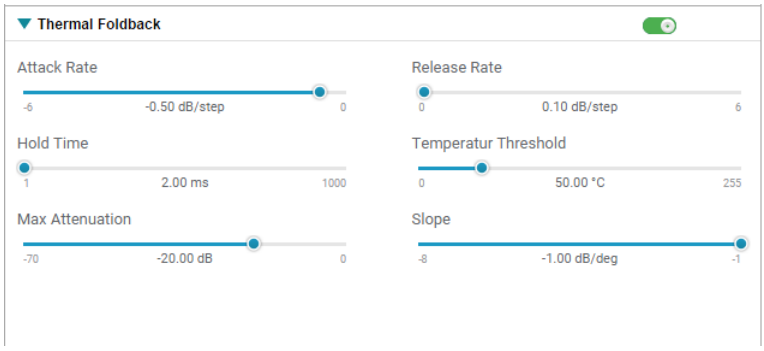

Figure 5-3. Thermal Foldback PPC3 Configuration

At this initial temperature, a full-scale input signal is played. Figure 5-4 shows the output of the codec at full-scale. This plot shows the positive output of a differential signal and the amplitude of this signal is later compared to the output signal when *Thermal Foldback* is triggered.

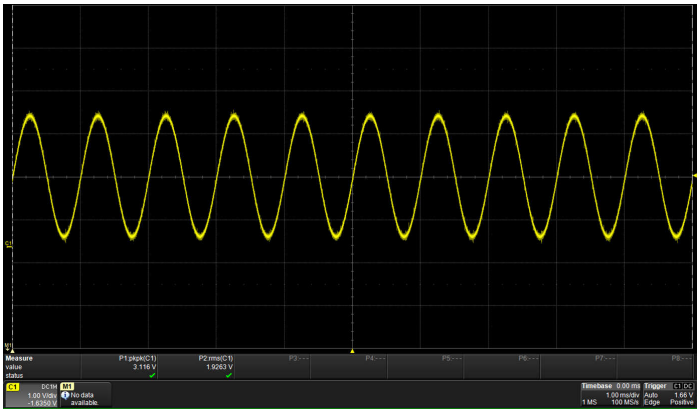

Figure 5-4. Thermal Foldback - Ambient Temperature

Hot air is applied to the device and soaked to a final temperature of 81°C. The temperature monitoring registers read A38h.

Figure 5-5 shows the comparison of the output at the initial temperature and at the final temperature. The initial temperature shows an amplitude of 3.12Vpp while the final temperature shows an amplitude of 640mVpp. This plot shows an attenuation of around -19dB, close to the expected attenuation based on the *Thermal Foldback* settings.

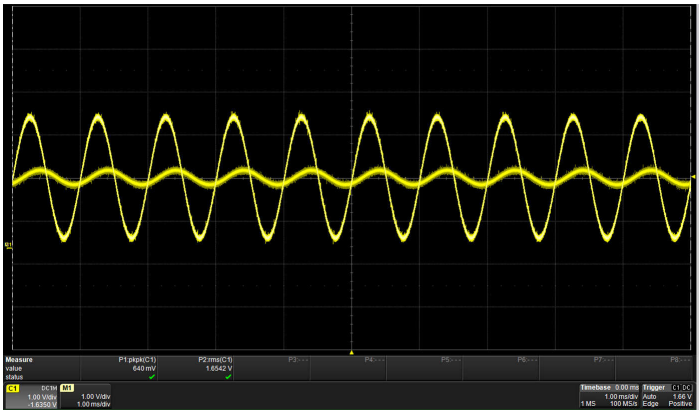

Figure 5-5. Thermal Foldback - Final Temperature Data Appended

6 Example

Table 6-1 provides an example script compatible with TAx5xxx-Q1 devices with the following parameters.

Table 6-1. Example Script With Parameters

Distortion Limiter	Brown-Out Protector	Thermal Foldback
• Attack Coefficient: -0.2dB/step • Release Coefficient: 0.5dB/step • Hold Counter: 1ms • Inflection Point: 11V • Threshold Max: -2dB • Threshold Min: -40dB • Slope: 1V/V	• Attack Coefficient: -0.5dB/step • Release Coefficient: 0.1dB/step • Hold Counter: 2ms • Critical Level 1: 11V • Critical Level 2: 3V • Gain Level 1: -3dB • Gain Level 2: -20dB	• Attack Coefficient: -0.5dB/step • Release Coefficient: 0.1dB/step • Hold Counter: 2ms • Temperature Threshold: 20°C • Max Attenuation: -30dB • Slope: -1V/V

```
# Key: w a0 XX YY ==> write to I2C address 0xa0, to register 0xXX, data 0xYY
# # ==> comment delimiter
#
# The following list gives an example sequence of items that must be executed in the time
# between powering the device up and reading data from the device. Note that there are
# other valid sequences depending on which features are used.
#
# See the corresponding EVM user guide for jumper settings and audio connections.
#
# Line-Out Fully-Differential 2-channel : INP1/INM1 - Ch1, INP2/INM2 - Ch2
# FSYNC = 48kHz (Output Data Sample Rate), BCLK = 12.288MHz (BCLK/FSYNC = 256)
####################################################################
#
#
# Power up IOVDD and AVDD power supplies keeping SHDNZ pin voltage LOW
# Wait for IOVDD and AVDD power supplies to settle to steady state operating voltage range.
# Release SHDNZ to HIGH.
# Wait for 1ms
#

w a0 00 00 # Go to Page 0
w a0 02 81 # Exit Sleep mode, Enable VREG and DREG
d 10       # Wait for 16ms

w a0 00 01 # Go to Page 1
w a0 ED 80 # Enable Distortion Limiter, BOP, and Thermal Foldback
w a0 5E 90 # Enable VBAT and Temperature channel for diagnostics

w a0 00 19        # Go to page 0x19
w a0 60 7d 16 1b f8    # Limiter Attack Rate
w a0 64 43 ca d0 23    # Limiter Release Rate
w a0 7c 00 00 00 30    # Limiter Hold Counter
w a0 74 00 00 58 00    # Inflection Point
w a0 6c 01 1f 3c 9a    # Limiter Threshold Maximum
w a0 70 00 03 9d b8    # Limiter Threshold Minimum
w a0 78 10 00 00 00     # Limiter Slope

w a0 00 01        # Go to page 0x1a
w a0 14 78 d6 fc 9f    # BOP Attack Rate
w a0 18 40 bd b7 c0    # BOP Release Rate
w a0 1c 00 00 00 60    # BOP Hold Counter
w a0 20 00 00 58 00    # BOP Voltage Threshold 1 (CT1)
w a0 28 00 00 18 00     # BOP Voltage Threshold 2 (CT2)
w a0 24 2d 4e fb d6    # BOP Threshold 1 (G1)
w a0 2c 06 66 66 66     # BOP Threshold 2 (G2)

w a0 30 78 d6 fc 9f    # Thermal Attack Rate
w a0 34 40 bd b7 c0    # Thermal Release Rate
w a0 38 00 00 00 60    # Thermal Hold Counter
w a0 3c 00 00 a0 00    # Temperature Threshold
w a0 40 04 0c 37 14     # Max Attenuation Threshold
w a0 44 f0 00 00 00     # Thermal Slope

w a0 00 00 # Go to Page 0
w a0 76 0c # Enable DAC Channels
w a0 78 40 # DAC Power Up
```

7 Summary

Texas Instruments has integrated three features into the TAx5xxx family of devices for audio processing in battery powered applications—*Distortion Limiter*, *Brown-out* protection, and *Thermal Foldback*. The *Distortion Limiter* dynamically adjusts audio levels based on battery voltage, providing distortion-free sound under fluctuating power conditions.*Brown-out* protection complements the *Distortion Limiter* by offering programmable, constant gain attenuation, which allows for customization of the audio quality preservation during low battery states. Finally, *Thermal Foldback* offers additional protection by adjusting the audio performance based on temperature, preventing overheating and potential damage to the system. Together, these features exemplify a comprehensive approach to balancing audio excellence and power efficiency in battery powered applications.

8 References

- Texas Instruments, *Battery Voltage Tracking Limiter and Brown-Out Protection* , application note
- Texas Instruments, *Advantages of Thermal Foldback on SmartAmps* , application note

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