Application Note

TAC5x1x and TAC5x1x-Q1 Programmable Biquad Filters - Configuration and Applications

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ABSTRACT

Audio systems make use of many signal processing function like Equalizers, Voice or Bass Boost, Mixers, and so on. The TAC5x1x and TAC5x1x-Q1 family of stereo audio codecs include different signal processing blocks based on the end application. This application note describes the operation of one of these signal processing blocks, the programmable per-channel infinite-impulse response (IIR) biquad filters. The application note also shows how these filters can be configured using the PurePath™ Console based on the desired frequency response.

The programmable biquad filters described in this application note are available in the following ADC, DAC, and Codec families:

- TAC5212, TAC5112, TAC5211, TAC5111
- TAC5212-Q1, TAC5112-Q1, TAC5111-Q1
- TAA5212
- TAD5212, TAD5112
- TAD5212-Q1, TAD5112-Q1
- TAC5412-Q1, TAC5312-Q1, TAC5411-Q1, TAC5311-Q1
- TAA5412-Q1

The TAC devices have the biquad filters on both recording and playback paths, whereas the TAA devices have the biquad filters only on the recording path, and TAD devices have the biquad filter only on the playback path.

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1 Introduction

The TAC5x1x and TAC5x1x-Q1 family of audio codecs have separate signal chains for recording (though analog and or digital microphones) and for playback (through DAC) of audio signals.

Each channel of the recording path follows the signal chain shown in Figure 1-1. This signal chain supports an analog differential or single-ended signal or a digital pulse density modulation (PDM) digital microphone. In TAC5x1x and TAC5x1x-Q1 device families, the analog input signal is converted by a high-performance ADC into a digital signal. The digital signal has a programmable phase calibration to adjust the phase delay of each channel in steps of one modulator clock cycle. This allows the system to match the phase across different channels. The phase-calibrated digital signal is then decimated through a set of linear phase filters or low-latency decimation filters. DC offset is removed from the decimated signal through a Digital High-Pass Filter (HPF) with three pre-set cutoff frequencies or a fully programmable cutoff frequency. The output of the HPF is gain calibrated with 0.1dB steps and summed with other channels. The gain calibration matches the gain across different channels, particularly if the channels have microphones with varying gain values. The output is then filtered by the Digital Biquad Filters and, in the case of secondary ASI, is parsed through a sample rate converter, before being gained by the volume control.

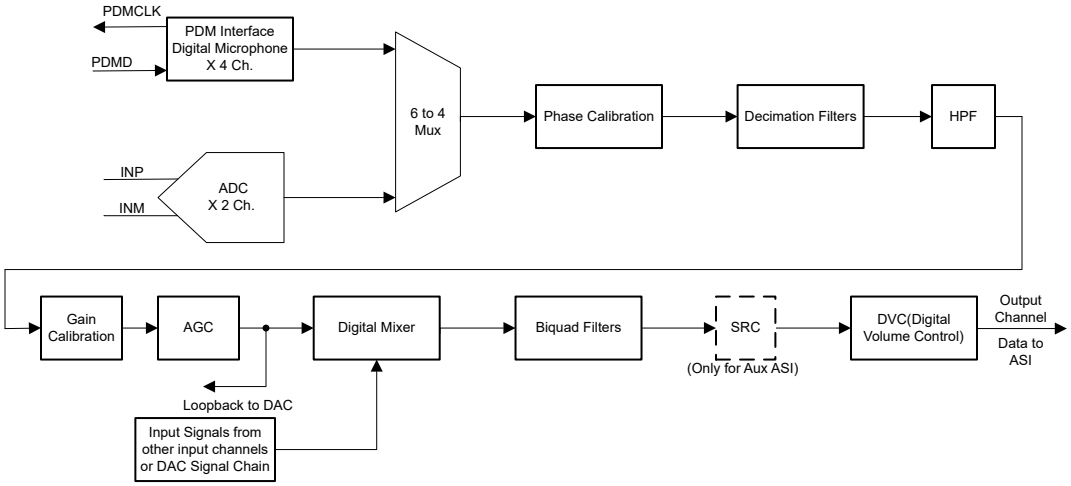

Figure 1-1. Recording (ADC) Path Signal Chain

Similarly each channel of the playback path follows the signal chain shown in Figure 1-2. the signal chain contains a programmable 8x4 Mixer for the main ASI inputs, and a 2x4 programmable mixer for the axillary ASI inputs. The mixed signal is then gained up through digital volume control, and a high-pass filter similar to that on the recording channel removes any DC component present in the signal. this signal is processed through a series of biquad filters, followed by additional signal processing blocks. The processed signal is then interpolated through interpolation filters, and is converted to analog output through a digital-to-analog converter (DAC).

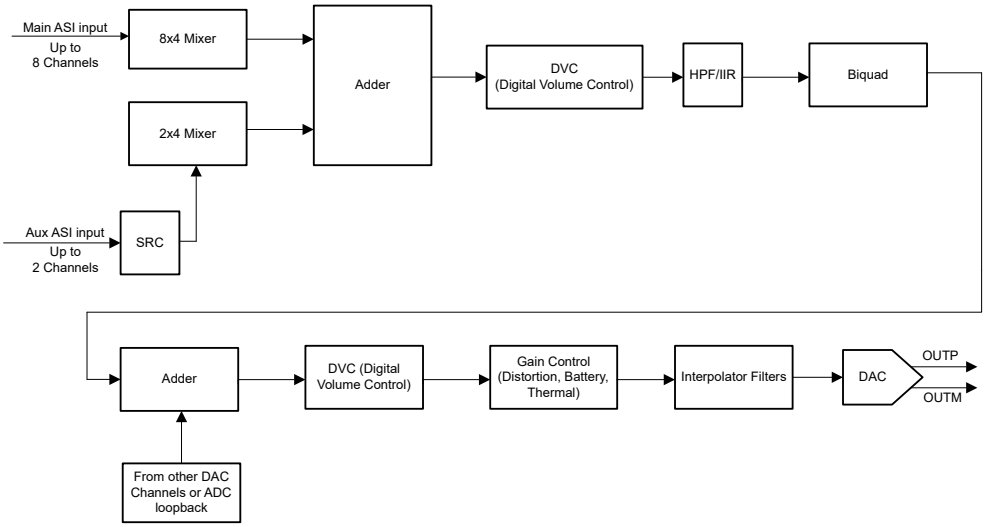

Figure 1-2. Playback (DAC) Path Signal Chain

This application note concentrates on how to configure the Digital Biquad Filters. The Digital Biquad Filters are digitally implemented as a set of IIR filters.

2 Infinite Impulse Response Filters

Equation 1 specifies the transfer function of an infinite impulse (IIR) digital filter.

$$H\left(z\right) = \frac{b_0 + b_1z^{-1} + b_2z^{-2} + \ldots + b_Mz^{-M}}{1 + a_1z^{-1} + a_2z^{-2} + \ldots + a_Nz^{-N}} \quad (1)$$

When the coefficients of this transfer function are quantized for fixed point implementations, the resulting errors due to quantization and the recursive nature of the filter can significantly alter the desired filter characteristics and lead to instability. Partitioning this transfer function into a set of cascaded lower-order filters reduces the sensitivity to coefficient quantization. Cascaded Biquad IIR filter implementations have been proven to be effective in minimizing these effects.

2.1 Digital Biquad Filter

A digital biquad filter is a second-order IIR digital filter. The filter is represented is a ratio of two quadratic equations, hence called *biquad* (or *bi-quadratic*). The transfer function of a biquad filter is specified in Equation 2, and Figure 2-1 shows the Direct Form II block diagram implementation for the same. In this equation, the coefficients are normalized so that a_0 = 1 through the division of all the coefficients by a_0.

$$H\left(z\right) = \frac{b_0 + b_1z^{-1} + b_2z^{-2}}{1 + a_1z^{-1} + a_2z^{-2}} \quad (2)$$

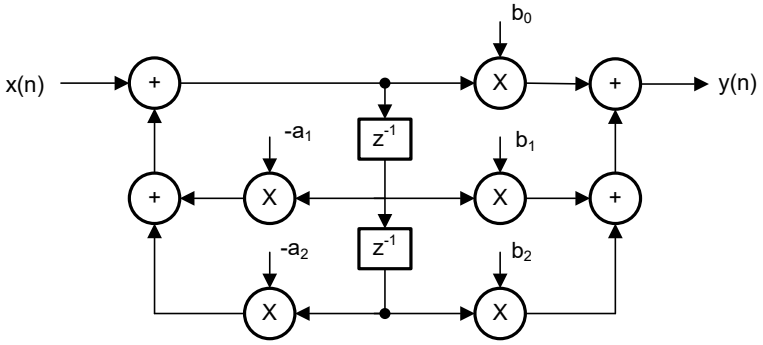

Figure 2-1. Direct Form II Biquad Filter

Different values of the filter coefficients a_1, a_2, b_0, b_1 and b_2 result in different filter frequency responses.

3 TAC5x1x and TAC5x1x-Q1 Digital Biquad Filters

The TAC5x1x and TAC5x1x-Q1 devices support up to three programmable digital biquad filters in the signal chain of each recording and playback channel, shown in Figure 1-1 and Figure 1-2 respectively. By default, each biquad filter acts as an all-pass filter, with a flat gain of 0dB across frequency. By changing the programmable coefficients of these biquad filters, the frequency response can be changed.

Equation 3 shows the quantized 32-bit transfer function of each biquad filter. The coefficients of the filter [N_0,N_1,N_2,D_1 and D_2] are programmable 32-bit twos-complement values, each occupying four consecutive registers in the register space of the device. With the Q-point located in the 31st bit location (Q31), the filter coefficients are in 1.31 format with a range from –1 (0x80000000) to 0.9999999995 (0x7FFFFFFF). In this notation, the decimal point is assumed to be between bit 30 and bit 31. Bit 31 contains the sign bit, while bits 30-0 contain the fractional bits as shown in Figure 3-1. With this notation, all coefficients are normalized to less than 1. To convert a floating point number less than one to Q31 format, multiply the floating point number by 2^{31} and truncate to the nearest integer. With this notation, the number 1, corresponding to a_0 in the denominator, becomes 2^{31} (0x7FFFFFF). Note that the coefficients N_1 and D_1 are multiplied by two. Thus, when using a digital filter design package to calculate these coefficients, divide by 2 the N_1 and D_1 before writing these coefficient registers. Also, note that coefficients D_1 and D_2 have a negative sign. So, multiply by –1 before writing D_1 and D_2 to the coefficient registers when using a digital filter design package.

$$H(z) = \frac{N_0 + 2N_1 z^{-1} + N_2 z^{-2}}{2^{31} - 2D_1 z^{-1} + D_2 z^{-2}} \quad (3)$$

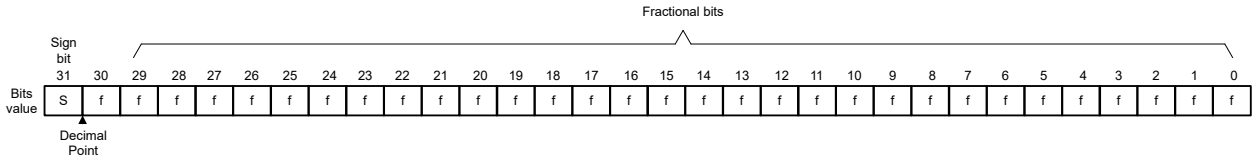

Figure 3-1. Q-31 Format Representation

3.1 Filter Design using PurePath™ Console

To facilitate the use of the biquad filters, the PurePath™ Console includes a graphical filter design section that plots the magnitude, phase, and group delay versus frequency. This filter design also generates the coefficients through several different filter design techniques filters.

Table 3-1 lists the different types of filters supported in the PurePath™ Console. Through bi-linear transformation (BLT), the analog filter equations shown in the table can be converted from the S-domain to the digital Z-domain. In these filters, each pole of the filter provides a –6dB per octave or –10dB per decade slope in the frequency response. Each zero of the filter provides a +6dB per octave or +10dB per decade slope in the frequency response.

In the transfer functions shown in the Table 3-1, ω_c corresponds to the center/corner frequency of the filter, and Q refers to the quality factor of the filter.

Table 3-1. PurePath™ Console Digital Biquad Filter Options

Filter Type	Filter Transfer FunctioN (S-domain)	Filter Description
Band Pass	$H(s) = \frac{\frac{\omega_c}{Q}s}{s^2 + \frac{\omega_c}{Q}s + \omega_c^2}$	Band-Pass filter at the specified center frequency and passband width (filter bandwidth)
Bass Shelf	$H(s) = \frac{\omega_c^2}{s^2 + \omega_c s + \omega_c^2}$	Specified gain applied at the low frequency up to the specified cutoff frequency

Table 3-1. PurePath™ Console Digital Biquad Filter Options (continued)

Filter Type	Filter Transfer FunctioN (S-domain)	Filter Description
Equalizer (Bandwidth)	$H(s) = \frac{\frac{\omega_c}{Q}s}{s^2 + \frac{\omega_c}{Q}s + \omega_c^2}$	Band-pass filters at the specified center frequency and passband width, with the specified gain
Equalizer (Q Factor)		Band-pass filter at the specified center frequency and quality factor, with the specified gain. The quality factor is the center frequency divided by the passband width.
Gain	$H(s) = \frac{s^2 - \frac{\omega_c}{Q}s + \omega_c^2}{s^2 + \frac{\omega_c}{Q}s + \omega_c^2}$	All pass filter at the specified gain
High-Pass Butterworth 1	$H(s) = \frac{s^2}{s^2 + \sqrt{2}\omega_c s + \omega_c^2}$	First-order high-pass filter with specified gain, specified cutoff frequency, maximally flat passband and stopband response. Stopband frequency response has a –10dB / decade slope.
High-Pass Butterworth 2		Second-order high-pass filter with specified gain, specified cutoff frequency, maximally flat passband and stopband response. Stopband frequency response has a –20dB / decade.
High-Pass Bessel 2	$H(s) = \frac{s^2}{s^2 + \sqrt{3}\omega_c s + \omega_c^2}$	Second-order high-pass filter with specified gain, specified cutoff frequency, maximally flat phase and constant group delay across passband.
High-Pass Linkwitz Riley 2	$H(s) = \left(\frac{\omega_c s}{1 + \omega_c s}\right)^2$	Second-order high-pass filter composed of a Butterworth filter with –3dB at the cutoff frequency. When cascading a low-pass and high-pass Linkwitz Riley filters, the overall gain at the crossover frequency is 0dB.
High-Pass Variable Q 2	$H(s) = \frac{s^2}{s^2 + \frac{\omega_c}{Q}s + \omega_c^2}$	Second-order high-pass filter at the specified center frequency, gain, and quality factor. The quality factor is the center frequency divided by the passband width.
High-Pass Chebyshev	$H(s) = \frac{s^2}{\sqrt{2}s^2 + 0.911\omega_c s + \omega_c^2}$	High-pass filter with equiripple in the passband with maximally flat response in stopband
Low-Pass Butterworth 1	$H(s) = \frac{\omega_c^2}{s^2 + \sqrt{2}\omega_c s + \omega_c^2}$	First-order low-pass filter with specified gain, specified cutoff frequency, maximally flat passband and stopband response. Stopband frequency response has a –10dB / decade slope.
Low-Pass Butterworth 2		Second-order low-pass filter with specified gain, specified cutoff frequency, maximally flat passband and stopband response. Stopband frequency response has a –20dB / decade.
Low-Pass Bessel 2	$H(s) = \frac{\omega_c^2}{s^2 + \sqrt{3}\omega_c s + \omega_c^2}$	Second-order low-pass filter with specified gain, specified cutoff frequency, maximally flat group delay across passband
Low-Pass Linkwitz Riley 2	$H(s) = \left(\frac{1}{1 + \omega_c s}\right)^2$	Second-order low-pass filter composed of a Butterworth filter with –3dB at the cutoff frequency. When cascading a low-pass and high-pass Linkwitz Riley filters, the overall gain at the crossover frequency is 0dB.
Low-Pass Variable Q 2	$H(s) = \frac{{\omega_c}^2}{s^2 + \frac{\omega_c}{Q}s + \omega_c^2}$	Second-order low-pass filter at the specified center frequency, gain and quality factor. The quality factor is the center frequency divided by the passband width.
Low-Pass Chebyshev	$H(s) = \frac{{\omega_c}^2}{\sqrt{2}s^2 + 0.911\omega_c s + \omega_c^2}$	Low-pass filter with equiripple in the passband with maximally flat response in stopband
Notch	$H(s) = \frac{s^2 + \omega_c^2}{s^2 + \frac{\omega_c}{Q}s + \omega_c^2}$	Band stop filter at the specified center frequency and stopband width (filter bandwidth)

Table 3-1. PurePath™ Console Digital Biquad Filter Options (continued)

Filter Type	Filter Transfer FunctioN (S-domain)	Filter Description
Phase Shift	$H(s) = \frac{1 - \frac{s}{\omega_c}}{1 + \frac{s}{\omega_c}}$	All pass filter with 180 degree phase shift at the specified center frequency through the width given by the bandwidth
Treble Shelf	$H(s) = \frac{s^2}{s^2 + \omega_c s + \omega_c^2}$	Specified gain applied at the high frequencies past the specified cutoff frequency

In PurePath™ Console, the programmable biquad filter configuration is available in the "Advanced" tab of of user interface. Figure 3-2 shows the option to enable this feature.

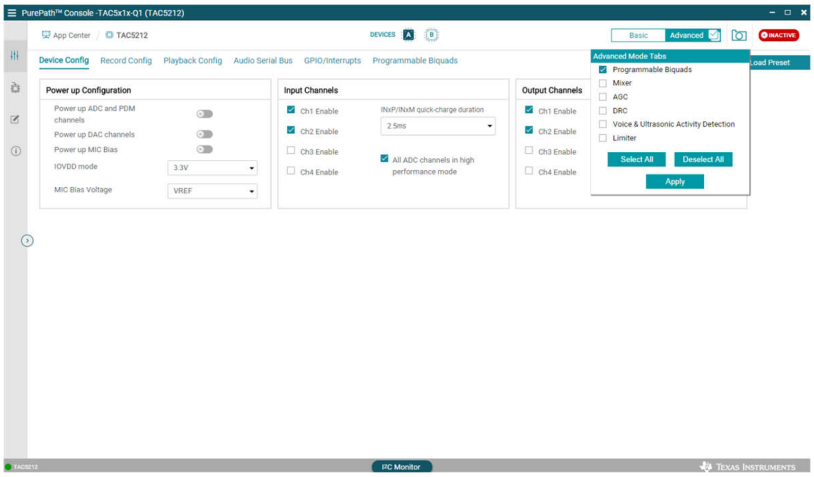

Figure 3-2. Enabling Biquad Filter Programmability in PurePath™ Console

3.1.1 Example of Programming Biquad Filters Using PurePath™ Console

Figure 3-3 shows how to create a set of filters for 5dB boost at 500Hz with bandwidth of 400Hz, cut –5dB at 4kHz with 5kHz bandwidth, and a Notch filter at 60Hz with 50Hz bandwidth for channel 1. The overall response of all three filters is plotted in red. The graphical plots allows users to zoom in and out of the frequency response plot and choose logarithmic or linear frequency axis, plot gain, phase, group delay, or impulse response.

Figure 3-3. PurePath™ Console Programmable Biquad Filter Example

Clicking on the swivel arrow at each biquad shows the normalized floating point coefficients for N_0, N_1, N_2, D_1, and D_2 of Equation 3 as shown in Figure 3-4. Note the PurePath™ Console has computed the floating point coefficients b0, b1, b2, a1, and a2 of Equation 2 and converted into the necessary values for N0, N1, N2, D1, and D2. Clicking the Apply button transmits the coefficients through I^2C to the TAC5x1x/TAC5x1x-Q1 devices on the EVM.

Figure 3-4. PurePath™ Console Programmable Biquad Filter Example Showing the Computed Coefficients in Normalized Floating Point Format

3.2 Generating Coefficients N_0, N_1, N_2, D_1, D_2 using a Digital Filter Design Package

By default (reset state), the biquad filters are configured as all-pass filters. In this condition, the filter coefficients (as mentioned in Equation 3) have the following values:

1. $N_0 = 2^{31}$ (b_0= 1)
2. N_1, N_2, D_1, D_2 = 0 (b_1, b_2, a_1, a_2 = 0)

When using a Digital Filter Design Package, such as MATLAB®, to generate an IIR biquad coefficients follow these steps:

1. Compute the coefficients [b0, b1, b2, a0, a1, a2] with a filter design function, such as the MATLAB butter function to design a Butterworth filter with cutoff at 1kHz of a system running at 48kHz. Note that MATLAB coefficients are normalized with a0 = 1.

```
[b, a] = butter( 2, 1000 / (48000/2) )
```

2. Convert these coefficients to [N_0, N_1, N_2, D_1, D_2] as shown in the following:
   - $N_0 = b_0$
   - $N_1 = b_1 / 2$
   - $N_2 = b_2$
   - $D_1 = -a_1 / 2$
   - $D_2 = -a_2$
3. Convert the coefficients to Q31 by multiplying by 2^{31} .
4. Round to nearest integer and convert to a 32-bit two's complement hexadecimal format:
   - For positive integers, convert to hexadecimal format
   - For negative integers, take the absolute value of the coefficient, convert it to binary, negate it, add one, and convert to hex. For example, to represent -135 in 32-bit two's complement hexadecimal format:
     – Absolute value of -135 is 0000 0000 0000 0000 0000 0000 1000 0111 in binary (or 0x00000087 in hex).
     – Negating the binary results in 1111 1111 1111 1111 1111 1111 0111 1000 in binary (or 0xFFFFFF78 in hex).

– Adding one to the same gives 1111 1111 1111 1111 1111 1111 0111 1001 in binary (or 0xFFFFFF79 in hex). Hence, the 32-bit, 32-bit two's complement hexadecimal representation of -135 is 0xFFFFFF79.

3.3 Avoiding Overflow Conditions

When cascading several biquad filters that add gain to the signal, make sure the overall response of the system does not cause the system to overflow. The biquad are computed in 32-bit fixed point arithmetic. If the overall response of the system in conjunction with the input signal is too large, undesired results can result due to arithmetic saturation. If saturation or overflow occurs, scale the input signal or scale down the coefficients of one or more biquad to keep the overall response of the system from saturating or overflowing.

Note that the overall response of the system is dependent on all the enabled components of the signal chain. The Digital High-Pass filter changes the frequency response at the low frequencies in conjunction with the Digital Biquad Filter response since both of these filters are cascaded together.

3.4 Biquad Filter Allocation on Recording Channel

Table 3-2 shows the assignment of these biquad filters to a specific channel on the ADC recording path based on the ADC_DSP_BQ_CFG[1:0] register setting of DSP_CFG0 (P0_R114) register. When no additional filtering is needed for the system application, setting ADC_DSP_BQ_CFG[1:0] to 2'b00 disables the Digital Biquad Filters for all channels. Table 3-2 also shows the mapping of the biquad filter coefficients in the TAC5x1x register space.

Table 3-2. Biquad Filter Allocation to the Record Channel

Programmable Biquad Filter	Record Channel Allocation Using P0_R114_D[3:2] Register Setting		
	ADC_DSP_BQ_CFG[1:0] = 2'b01 (1 Biquad per Channel)	ADC_DSP_BQ_CFG[1:0] = 2'b10 (Default) (2 Biquads per Channel)	ADC_DSP_BQ_CFG[1:0] = 2'b11 (3 Biquads per Channel)
Biquad Filter 1	Allocated to output channel 1	Allocated to output channel 1	Allocated to output channel 1
Biquad Filter 2	Allocated to output channel 2	Allocated to output channel 2	Allocated to output channel 2
Biquad Filter 3	Allocated to output channel 3	Allocated to output channel 3	Allocated to output channel 3
Biquad Filter 4	Allocated to output channel 4	Allocated to output channel 4	Allocated to output channel 4
Biquad Filter 5	Not Used	Allocated to output channel 1	Allocated to output channel 1
Biquad Filter 6	Not Used	Allocated to output channel 2	Allocated to output channel 2
Biquad Filter 7	Not Used	Allocated to output channel 3	Allocated to output channel 3
Biquad Filter 8	Not Used	Allocated to output channel 4	Allocated to output channel 4
Biquad Filter 9	Not Used	Not Used	Allocated to output channel 1
Biquad Filter 10	Not Used	Not Used	Allocated to output channel 2
Biquad Filter 11	Not Used	Not Used	Allocated to output channel 3
Biquad Filter 12	Not Used	Not Used	Allocated to output channel 4

Table 3-3. Biquad Filter Coefficients Register Mapping for the Record Channels

Biquad Filter	Register Mapping of Coefficients	Biquad Filter	Register Mapping of Coefficients
Biquad Filter 1	P8_R8 to P8_R27	Biquad Filter 7	P9_R8 to P9_R27
Biquad Filter 2	P8_R28 to P8_R47	Biquad Filter 8	P9_R28 to P9_R47
Biquad Filter 3	P8_R48 to P8_R67	Biquad Filter 9	P9_R48 to P9_R67
Biquad Filter 4	P8_R68 to P8_R87	Biquad Filter 10	P9_R68 to P9_R87
Biquad Filter 5	P8_R88 to P8_R107	Biquad Filter 11	P9_R88 to P9_R107
Biquad Filter 6	P8_R108 to P8_R127	Biquad Filter 12	P9_R108 to P9_R127

Table 3-4 shows the programmable coefficient registers of the biquad filters 1-6 in page 8 of the TAC5x1x registers.

Table 3-4. Programmable Coefficient Registers for Digital Biquad Filters 1–6

Page 0x08 Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x00	PAGE[7:0]	Device page register	0x00		
0x08	ADC_BQ1_N0_BYT1[7:0]	Programmable ADC biquad 1, N0 coefficient byte[31:24]	0x7F	1	N_0
0x09	ADC_BQ1_N0_BYT2[7:0]	Programmable ADC biquad 1, N0 coefficient byte[23:16]	0xFF		
0x0A	ADC_BQ1_N0_BYT3[7:0]	Programmable ADC biquad 1, N0 coefficient byte[15:8]	0xFF		
0x0B	ADC_BQ1_N0_BYT4[7:0]	Programmable ADC biquad 1, N0 coefficient byte[7:0]	0xFF		
0x0C	ADC_BQ1_N1_BYT1[7:0]	Programmable ADC biquad 1, N1 coefficient byte[31:24]	0x00		N_1
0x0D	ADC_BQ1_N1_BYT2[7:0]	Programmable ADC biquad 1, N1 coefficient byte[23:16]	0x00		
0x0E	ADC_BQ1_N1_BYT3[7:0]	Programmable ADC biquad 1, N1 coefficient byte[15:8]	0x00		
0x0F	ADC_BQ1_N1_BYT4[7:0]	Programmable ADC biquad 1, N1 coefficient byte[7:0]	0x00		
0x10	ADC_BQ1_N2_BYT1[7:0]	Programmable ADC biquad 1, N2 coefficient byte[31:24]	0x00		N_2
0x11	ADC_BQ1_N2_BYT2[7:0]	Programmable ADC biquad 1, N2 coefficient byte[23:16]	0x00		
0x12	ADC_BQ1_N2_BYT3[7:0]	Programmable ADC biquad 1, N2 coefficient byte[15:8]	0x00		
0x13	ADC_BQ1_N2_BYT4[7:0]	Programmable ADC biquad 1, N2 coefficient byte[7:0]	0x00		
0x14	ADC_BQ1_D1_BYT1[7:0]	Programmable ADC biquad 1, D1 coefficient byte[31:24]	0x00		D_1
0x15	ADC_BQ1_D1_BYT2[7:0]	Programmable ADC biquad 1, D1 coefficient byte[23:16]	0x00		
0x16	ADC_BQ1_D1_BYT3[7:0]	Programmable ADC biquad 1, D1 coefficient byte[15:8]	0x00		
0x17	ADC_BQ1_D1_BYT4[7:0]	Programmable ADC biquad 1, D1 coefficient byte[7:0]	0x00		
0x18	ADC_BQ1_D2_BYT1[7:0]	Programmable ADC biquad 1, D2 coefficient byte[31:24]	0x00		D_2
0x19	ADC_BQ1_D2_BYT2[7:0]	Programmable ADC biquad 1, D2 coefficient byte[23:16]	0x00		
0x1A	ADC_BQ1_D2_BYT3[7:0]	Programmable ADC biquad 1, D2 coefficient byte[15:8]	0x00		
0x1B	ADC_BQ1_D2_BYT4[7:0]	Programmable ADC biquad 1, D2 coefficient byte[7:0]	0x00		

Table 3-4. Programmable Coefficient Registers for Digital Biquad Filters 1–6 (continued)

Page 0x08 Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x1C	ADC_BQ2_N0_BYT1[7:0]	Programmable ADC biquad 2, N0 coefficient byte[31:24]	0x7F	2	N_0
0x1D	ADC_BQ2_N0_BYT2[7:0]	Programmable ADC biquad 2, N0 coefficient byte[23:16]	0xFF		
0x1E	ADC_BQ2_N0_BYT3[7:0]	Programmable ADC biquad 2, N0 coefficient byte[15:8]	0xFF		
0x1F	ADC_BQ2_N0_BYT4[7:0]	Programmable ADC biquad 2, N0 coefficient byte[7:0]	0xFF		
0x20	ADC_BQ2_N1_BYT1[7:0]	Programmable ADC biquad 2, N1 coefficient byte[31:24]	0x00		N_1
0x21	ADC_BQ2_N1_BYT2[7:0]	Programmable ADC biquad 2, N1 coefficient byte[23:16]	0x00		
0x22	ADC_BQ2_N1_BYT3[7:0]	Programmable ADC biquad 2, N1 coefficient byte[15:8]	0x00		
0x23	ADC_BQ2_N1_BYT4[7:0]	Programmable ADC biquad 2, N1 coefficient byte[7:0]	0x00		
0x24	ADC_BQ2_N2_BYT1[7:0]	Programmable ADC biquad 2, N2 coefficient byte[31:24]	0x00		N_2
0x25	ADC_BQ2_N2_BYT2[7:0]	Programmable ADC biquad 2, N2 coefficient byte[23:16]	0x00		
0x26	ADC_BQ2_N2_BYT3[7:0]	Programmable ADC biquad 2, N2 coefficient byte[15:8]	0x00		
0x27	ADC_BQ2_N2_BYT4[7:0]	Programmable ADC biquad 2, N2 coefficient byte[7:0]	0x00		
0x28	ADC_BQ2_D1_BYT1[7:0]	Programmable ADC biquad 2, D1 coefficient byte[31:24]	0x00		D_1
0x29	ADC_BQ2_D1_BYT2[7:0]	Programmable ADC biquad 2, D1 coefficient byte[23:16]	0x00		
0x2A	ADC_BQ2_D1_BYT3[7:0]	Programmable ADC biquad 2, D1 coefficient byte[15:8]	0x00		
0x2B	ADC_BQ2_D1_BYT4[7:0]	Programmable ADC biquad 2, D1 coefficient byte[7:0]	0x00		
0x2C	ADC_BQ2_D2_BYT1[7:0]	Programmable ADC biquad 2, D2 coefficient byte[31:24]	0x00		D_2
0x2D	ADC_BQ2_D2_BYT2[7:0]	Programmable ADC biquad 2, D2 coefficient byte[23:16]	0x00		
0x2E	ADC_BQ2_D2_BYT3[7:0]	Programmable ADC biquad 2, D2 coefficient byte[15:8]	0x00		
0x2F	ADC_BQ2_D2_BYT4[7:0]	Programmable ADC biquad 2, D2 coefficient byte[7:0]	0x00		

Table 3-4. Programmable Coefficient Registers for Digital Biquad Filters 1–6 (continued)

Page 0x08 Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x30	ADC_BQ3_N0_BYT1[7:0]	Programmable ADC biquad 3, N0 coefficient byte[31:24]	0x7F	3	N_0
0x31	ADC_BQ3_N0_BYT2[7:0]	Programmable ADC biquad 3, N0 coefficient byte[23:16]	0xFF		
0x32	ADC_BQ3_N0_BYT3[7:0]	Programmable ADC biquad 3, N0 coefficient byte[15:8]	0xFF		
0x33	ADC_BQ3_N0_BYT4[7:0]	Programmable ADC biquad 3, N0 coefficient byte[7:0]	0xFF		
0x34	ADC_BQ3_N1_BYT1[7:0]	Programmable ADC biquad 3, N1 coefficient byte[31:24]	0x00		N_1
0x35	ADC_BQ3_N1_BYT2[7:0]	Programmable ADC biquad 3, N1 coefficient byte[23:16]	0x00		
0x36	ADC_BQ3_N1_BYT3[7:0]	Programmable ADC biquad 3, N1 coefficient byte[15:8]	0x00		
0x37	ADC_BQ3_N1_BYT4[7:0]	Programmable ADC biquad 3, N1 coefficient byte[7:0]	0x00		
0x38	ADC_BQ3_N2_BYT1[7:0]	Programmable ADC biquad 3, N2 coefficient byte[31:24]	0x00		N_2
0x39	ADC_BQ3_N2_BYT2[7:0]	Programmable ADC biquad 3, N2 coefficient byte[23:16]	0x00		
0x3A	ADC_BQ3_N2_BYT3[7:0]	Programmable ADC biquad 3, N2 coefficient byte[15:8]	0x00		
0x3B	ADC_BQ3_N2_BYT4[7:0]	Programmable ADC biquad 3, N2 coefficient byte[7:0]	0x00		
0x3C	ADC_BQ3_D1_BYT1[7:0]	Programmable ADC biquad 3, D1 coefficient byte[31:24]	0x00		D_1
0x3D	ADC_BQ3_D1_BYT2[7:0]	Programmable ADC biquad 3, D1 coefficient byte[23:16]	0x00		
0x3E	ADC_BQ3_D1_BYT3[7:0]	Programmable ADC biquad 3, D1 coefficient byte[15:8]	0x00		
0x3F	ADC_BQ3_D1_BYT4[7:0]	Programmable ADC biquad 3, D1 coefficient byte[7:0]	0x00		
0x40	ADC_BQ3_D2_BYT1[7:0]	Programmable ADC biquad 3, D2 coefficient byte[31:24]	0x00		D_2
0x41	ADC_BQ3_D2_BYT2[7:0]	Programmable ADC biquad 3, D2 coefficient byte[23:16]	0x00		
0x42	ADC_BQ3_D2_BYT3[7:0]	Programmable ADC biquad 3, D2 coefficient byte[15:8]	0x00		
0x43	ADC_BQ3_D2_BYT4[7:0]	Programmable ADC biquad 3, D2 coefficient byte[7:0]	0x00		

Table 3-4. Programmable Coefficient Registers for Digital Biquad Filters 1–6 (continued)

Page 0x08 Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x44	ADC_BQ4_N0_BYT1[7:0]	Programmable ADC biquad 4, N0 coefficient byte[31:24]	0x7F	4	N_0
0x45	ADC_BQ4_N0_BYT2[7:0]	Programmable ADC biquad 4, N0 coefficient byte[23:16]	0xFF		
0x46	ADC_BQ4_N0_BYT3[7:0]	Programmable ADC biquad 4, N0 coefficient byte[15:8]	0xFF		
0x47	ADC_BQ4_N0_BYT4[7:0]	Programmable ADC biquad 4, N0 coefficient byte[7:0]	0xFF		
0x48	ADC_BQ4_N1_BYT1[7:0]	Programmable ADC biquad 4, N1 coefficient byte[31:24]	0x00		N_1
0x49	ADC_BQ4_N1_BYT2[7:0]	Programmable ADC biquad 4, N1 coefficient byte[23:16]	0x00		
0x4A	ADC_BQ4_N1_BYT3[7:0]	Programmable ADC biquad 4, N1 coefficient byte[15:8]	0x00		
0x4B	ADC_BQ4_N1_BYT4[7:0]	Programmable ADC biquad 4, N1 coefficient byte[7:0]	0x00		
0x4C	ADC_BQ4_N2_BYT1[7:0]	Programmable ADC biquad 4, N2 coefficient byte[31:24]	0x00		N_2
0x4D	ADC_BQ4_N2_BYT2[7:0]	Programmable ADC biquad 4, N2 coefficient byte[23:16]	0x00		
0x4E	ADC_BQ4_N2_BYT3[7:0]	Programmable ADC biquad 4, N2 coefficient byte[15:8]	0x00		
0x4F	ADC_BQ4_N2_BYT4[7:0]	Programmable ADC biquad 4, N2 coefficient byte[7:0]	0x00		
0x50	ADC_BQ4_D1_BYT1[7:0]	Programmable ADC biquad 4, D1 coefficient byte[31:24]	0x00		D_1
0x51	ADC_BQ4_D1_BYT2[7:0]	Programmable ADC biquad 4, D1 coefficient byte[23:16]	0x00		
0x52	ADC_BQ4_D1_BYT3[7:0]	Programmable ADC biquad 4, D1 coefficient byte[15:8]	0x00		
0x53	ADC_BQ4_D1_BYT4[7:0]	Programmable ADC biquad 4, D1 coefficient byte[7:0]	0x00		
0x54	ADC_BQ4_D2_BYT1[7:0]	Programmable ADC biquad 4, D2 coefficient byte[31:24]	0x00		D_2
0x55	ADC_BQ4_D2_BYT2[7:0]	Programmable ADC biquad 4, D2 coefficient byte[23:16]	0x00		
0x56	ADC_BQ4_D2_BYT3[7:0]	Programmable ADC biquad 4, D2 coefficient byte[15:8]	0x00		
0x57	ADC_BQ4_D2_BYT4[7:0]	Programmable ADC biquad 4, D2 coefficient byte[7:0]	0x00		

Table 3-4. Programmable Coefficient Registers for Digital Biquad Filters 1–6 (continued)

Page 0x08 Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x58	ADC_BQ5_N0_BYT1[7:0]	Programmable ADC biquad 5, N0 coefficient byte[31:24]	0x7F	5	N_0
0x59	ADC_BQ5_N0_BYT2[7:0]	Programmable ADC biquad 5, N0 coefficient byte[23:16]	0xFF		
0x5A	ADC_BQ5_N0_BYT3[7:0]	Programmable ADC biquad 5, N0 coefficient byte[15:8]	0xFF		
0x5B	ADC_BQ5_N0_BYT4[7:0]	Programmable ADC biquad 5, N0 coefficient byte[7:0]	0xFF		
0x5C	ADC_BQ5_N1_BYT1[7:0]	Programmable ADC biquad 5, N1 coefficient byte[31:24]	0x00		N_1
0x5D	ADC_BQ5_N1_BYT2[7:0]	Programmable ADC biquad 5, N1 coefficient byte[23:16]	0x00		
0x5E	ADC_BQ5_N1_BYT3[7:0]	Programmable ADC biquad 5, N1 coefficient byte[15:8]	0x00		
0x5F	ADC_BQ5_N1_BYT4[7:0]	Programmable ADC biquad 5, N1 coefficient byte[7:0]	0x00		
0x60	ADC_BQ5_N2_BYT1[7:0]	Programmable ADC biquad 5, N2 coefficient byte[31:24]	0x00		N_2
0x61	ADC_BQ5_N2_BYT2[7:0]	Programmable ADC biquad 5, N2 coefficient byte[23:16]	0x00		
0x62	ADC_BQ5_N2_BYT3[7:0]	Programmable ADC biquad 5, N2 coefficient byte[15:8]	0x00		
0x63	ADC_BQ5_N2_BYT4[7:0]	Programmable ADC biquad 5, N2 coefficient byte[7:0]	0x00		
0x64	ADC_BQ5_D1_BYT1[7:0]	Programmable ADC biquad 5, D1 coefficient byte[31:24]	0x00		D_1
0x65	ADC_BQ5_D1_BYT2[7:0]	Programmable ADC biquad 5, D1 coefficient byte[23:16]	0x00		
0x66	ADC_BQ5_D1_BYT3[7:0]	Programmable ADC biquad 5, D1 coefficient byte[15:8]	0x00		
0x67	ADC_BQ5_D1_BYT4[7:0]	Programmable ADC biquad 5, D1 coefficient byte[7:0]	0x00		
0x68	ADC_BQ5_D2_BYT1[7:0]	Programmable ADC biquad 5, D2 coefficient byte[31:24]	0x00		D_2
0x69	ADC_BQ5_D2_BYT2[7:0]	Programmable ADC biquad 5, D2 coefficient byte[23:16]	0x00		
0x6A	ADC_BQ5_D2_BYT3[7:0]	Programmable ADC biquad 5, D2 coefficient byte[15:8]	0x00		
0x6B	ADC_BQ5_D2_BYT4[7:0]	Programmable ADC biquad 5, D2 coefficient byte[7:0]	0x00		

Table 3-4. Programmable Coefficient Registers for Digital Biquad Filters 1–6 (continued)

Page 0x08 Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x6C	ADC_BQ6_N0_BYT1[7:0]	Programmable ADC biquad 6, N0 coefficient byte[31:24]	0x7F	6	N_0
0x6D	ADC_BQ6_N0_BYT2[7:0]	Programmable ADC biquad 6, N0 coefficient byte[23:16]	0xFF		
0x6E	ADC_BQ6_N0_BYT3[7:0]	Programmable ADC biquad 6, N0 coefficient byte[15:8]	0xFF		
0x6F	ADC_BQ6_N0_BYT4[7:0]	Programmable ADC biquad 6, N0 coefficient byte[7:0]	0xFF		
0x70	ADC_BQ6_N1_BYT1[7:0]	Programmable ADC biquad 6, N1 coefficient byte[31:24]	0x00		N_1
0x71	ADC_BQ6_N1_BYT2[7:0]	Programmable ADC biquad 6, N1 coefficient byte[23:16]	0x00		
0x72	ADC_BQ6_N1_BYT3[7:0]	Programmable ADC biquad 6, N1 coefficient byte[15:8]	0x00		
0x73	ADC_BQ6_N1_BYT4[7:0]	Programmable ADC biquad 6, N1 coefficient byte[7:0]	0x00		
0x74	ADC_BQ6_N2_BYT1[7:0]	Programmable ADC biquad 6, N2 coefficient byte[31:24]	0x00		N_2
0x75	ADC_BQ6_N2_BYT2[7:0]	Programmable ADC biquad 6, N2 coefficient byte[23:16]	0x00		
0x76	ADC_BQ6_N2_BYT3[7:0]	Programmable ADC biquad 6, N2 coefficient byte[15:8]	0x00		
0x77	ADC_BQ6_N2_BYT4[7:0]	Programmable ADC biquad 6, N2 coefficient byte[7:0]	0x00		
0x78	ADC_BQ6_D1_BYT1[7:0]	Programmable ADC biquad 6, D1 coefficient byte[31:24]	0x00		D_1
0x79	ADC_BQ6_D1_BYT2[7:0]	Programmable ADC biquad 6, D1 coefficient byte[23:16]	0x00		
0x7A	ADC_BQ6_D1_BYT3[7:0]	Programmable ADC biquad 6, D1 coefficient byte[15:8]	0x00		
0x7B	ADC_BQ6_D1_BYT4[7:0]	Programmable ADC biquad 6, D1 coefficient byte[7:0]	0x00		
0x7C	ADC_BQ6_D2_BYT1[7:0]	Programmable ADC biquad 6, D2 coefficient byte[31:24]	0x00		D_2
0x7D	ADC_BQ6_D2_BYT2[7:0]	Programmable ADC biquad 6, D2 coefficient byte[23:16]	0x00		
0x7E	ADC_BQ6_D2_BYT3[7:0]	Programmable ADC biquad 6, D2 coefficient byte[15:8]	0x00		
0x7F	ADC_BQ6_D2_BYT4[7:0]	Programmable ADC biquad 6, D2 coefficient byte[7:0]	0x00		

Similarly, Table 3-5 shows the programmable coefficient registers of the biquad filters 7-12 in page 9 of the TAC5x1x registers.

Table 3-5. Programmable Coefficient Registers for Digital Biquad Filters 7-12

Page 0x09 Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x00	PAGE[7:0]	Device page register	0x00		
0x08	ADC_BQ7_N0_BYT1[7:0]	Programmable ADC biquad 7, N0 coefficient byte[31:24]	0x7F	7	N_0
0x09	ADC_BQ7_N0_BYT2[7:0]	Programmable ADC biquad 7, N0 coefficient byte[23:16]	0xFF		
0x0A	ADC_BQ7_N0_BYT3[7:0]	Programmable ADC biquad 7, N0 coefficient byte[15:8]	0xFF		
0x0B	ADC_BQ7_N0_BYT4[7:0]	Programmable ADC biquad 7, N0 coefficient byte[7:0]	0xFF		
0x0C	ADC_BQ7_N1_BYT1[7:0]	Programmable ADC biquad 7, N1 coefficient byte[31:24]	0x00		N_1
0x0D	ADC_BQ7_N1_BYT2[7:0]	Programmable ADC biquad 7, N1 coefficient byte[23:16]	0x00		
0x0E	ADC_BQ7_N1_BYT3[7:0]	Programmable ADC biquad 7, N1 coefficient byte[15:8]	0x00		
0x0F	ADC_BQ7_N1_BYT4[7:0]	Programmable ADC biquad 7, N1 coefficient byte[7:0]	0x00		
0x10	ADC_BQ7_N2_BYT1[7:0]	Programmable ADC biquad 7, N2 coefficient byte[31:24]	0x00		N_2
0x11	ADC_BQ7_N2_BYT2[7:0]	Programmable ADC biquad 7, N2 coefficient byte[23:16]	0x00		
0x12	ADC_BQ7_N2_BYT3[7:0]	Programmable ADC biquad 7, N2 coefficient byte[15:8]	0x00		
0x13	ADC_BQ7_N2_BYT4[7:0]	Programmable ADC biquad 7, N2 coefficient byte[7:0]	0x00		
0x14	ADC_BQ7_D1_BYT1[7:0]	Programmable ADC biquad 7, D1 coefficient byte[31:24]	0x00		D_1
0x15	ADC_BQ7_D1_BYT2[7:0]	Programmable ADC biquad 7, D1 coefficient byte[23:16]	0x00		
0x16	ADC_BQ7_D1_BYT3[7:0]	Programmable ADC biquad 7, D1 coefficient byte[15:8]	0x00		
0x17	ADC_BQ7_D1_BYT4[7:0]	Programmable ADC biquad 7, D1 coefficient byte[7:0]	0x00		
0x18	ADC_BQ7_D2_BYT1[7:0]	Programmable ADC biquad 7, D2 coefficient byte[31:24]	0x00		D_2
0x19	ADC_BQ7_D2_BYT2[7:0]	Programmable ADC biquad 7, D2 coefficient byte[23:16]	0x00		
0x1A	ADC_BQ7_D2_BYT3[7:0]	Programmable ADC biquad 7, D2 coefficient byte[15:8]	0x00		
0x1B	ADC_BQ7_D2_BYT4[7:0]	Programmable ADC biquad 7, D2 coefficient byte[7:0]	0x00		

Table 3-5. Programmable Coefficient Registers for Digital Biquad Filters 7-12 (continued)

Page 0x09 Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x1C	ADC_BQ8_N0_BYT1[7:0]	Programmable ADC biquad 8, N0 coefficient byte[31:24]	0x7F	8	N_0
0x1D	ADC_BQ8_N0_BYT2[7:0]	Programmable ADC biquad 8, N0 coefficient byte[23:16]	0xFF		
0x1E	ADC_BQ8_N0_BYT3[7:0]	Programmable ADC biquad 8, N0 coefficient byte[15:8]	0xFF		
0x1F	ADC_BQ8_N0_BYT4[7:0]	Programmable ADC biquad 8, N0 coefficient byte[7:0]	0xFF		
0x20	ADC_BQ8_N1_BYT1[7:0]	Programmable ADC biquad 8, N1 coefficient byte[31:24]	0x00		N_1
0x21	ADC_BQ8_N1_BYT2[7:0]	Programmable ADC biquad 8, N1 coefficient byte[23:16]	0x00		
0x22	ADC_BQ8_N1_BYT3[7:0]	Programmable ADC biquad 8, N1 coefficient byte[15:8]	0x00		
0x23	ADC_BQ8_N1_BYT4[7:0]	Programmable ADC biquad 8, N1 coefficient byte[7:0]	0x00		
0x24	ADC_BQ8_N2_BYT1[7:0]	Programmable ADC biquad 8, N2 coefficient byte[31:24]	0x00		N_2
0x25	ADC_BQ8_N2_BYT2[7:0]	Programmable ADC biquad 8, N2 coefficient byte[23:16]	0x00		
0x26	ADC_BQ8_N2_BYT3[7:0]	Programmable ADC biquad 8, N2 coefficient byte[15:8]	0x00		
0x27	ADC_BQ8_N2_BYT4[7:0]	Programmable ADC biquad 8, N2 coefficient byte[7:0]	0x00		
0x28	ADC_BQ8_D1_BYT1[7:0]	Programmable ADC biquad 8, D1 coefficient byte[31:24]	0x00		D_1
0x29	ADC_BQ8_D1_BYT2[7:0]	Programmable ADC biquad 8, D1 coefficient byte[23:16]	0x00		
0x2A	ADC_BQ8_D1_BYT3[7:0]	Programmable ADC biquad 8, D1 coefficient byte[15:8]	0x00		
0x2B	ADC_BQ8_D1_BYT4[7:0]	Programmable ADC biquad 8, D1 coefficient byte[7:0]	0x00		
0x2C	ADC_BQ8_D2_BYT1[7:0]	Programmable ADC biquad 8, D2 coefficient byte[31:24]	0x00		D_2
0x2D	ADC_BQ8_D2_BYT2[7:0]	Programmable ADC biquad 8, D2 coefficient byte[23:16]	0x00		
0x2E	ADC_BQ8_D2_BYT3[7:0]	Programmable ADC biquad 8, D2 coefficient byte[15:8]	0x00		
0x2F	ADC_BQ8_D2_BYT4[7:0]	Programmable ADC biquad 8, D2 coefficient byte[7:0]	0x00		

Table 3-5. Programmable Coefficient Registers for Digital Biquad Filters 7-12 (continued)

Page 0x09 Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x30	ADC_BQ9_N0_BYT1[7:0]	Programmable ADC biquad 9, N0 coefficient byte[31:24]	0x7F	9	N_0
0x31	ADC_BQ9_N0_BYT2[7:0]	Programmable ADC biquad 9, N0 coefficient byte[23:16]	0xFF		
0x32	ADC_BQ9_N0_BYT3[7:0]	Programmable ADC biquad 9, N0 coefficient byte[15:8]	0xFF		
0x33	ADC_BQ9_N0_BYT4[7:0]	Programmable ADC biquad 9, N0 coefficient byte[7:0]	0xFF		
0x34	ADC_BQ9_N1_BYT1[7:0]	Programmable ADC biquad 9, N1 coefficient byte[31:24]	0x00		N_1
0x35	ADC_BQ9_N1_BYT2[7:0]	Programmable ADC biquad 9, N1 coefficient byte[23:16]	0x00		
0x36	ADC_BQ9_N1_BYT3[7:0]	Programmable ADC biquad 9, N1 coefficient byte[15:8]	0x00		
0x37	ADC_BQ9_N1_BYT4[7:0]	Programmable ADC biquad 9, N1 coefficient byte[7:0]	0x00		
0x38	ADC_BQ9_N2_BYT1[7:0]	Programmable ADC biquad 9, N2 coefficient byte[31:24]	0x00		N_2
0x39	ADC_BQ9_N2_BYT2[7:0]	Programmable ADC biquad 9, N2 coefficient byte[23:16]	0x00		
0x3A	ADC_BQ9_N2_BYT3[7:0]	Programmable ADC biquad 9, N2 coefficient byte[15:8]	0x00		
0x3B	ADC_BQ9_N2_BYT4[7:0]	Programmable ADC biquad 9, N2 coefficient byte[7:0]	0x00		
0x3C	ADC_BQ9_D1_BYT1[7:0]	Programmable ADC biquad 9, D1 coefficient byte[31:24]	0x00		D_1
0x3D	ADC_BQ9_D1_BYT2[7:0]	Programmable ADC biquad 9, D1 coefficient byte[23:16]	0x00		
0x3E	ADC_BQ9_D1_BYT3[7:0]	Programmable ADC biquad 9, D1 coefficient byte[15:8]	0x00		
0x3F	ADC_BQ9_D1_BYT4[7:0]	Programmable ADC biquad 9, D1 coefficient byte[7:0]	0x00		
0x40	ADC_BQ9_D2_BYT1[7:0]	Programmable ADC biquad 9, D2 coefficient byte[31:24]	0x00		D_2
0x41	ADC_BQ9_D2_BYT2[7:0]	Programmable ADC biquad 9, D2 coefficient byte[23:16]	0x00		
0x42	ADC_BQ9_D2_BYT3[7:0]	Programmable ADC biquad 9, D2 coefficient byte[15:8]	0x00		
0x43	ADC_BQ9_D2_BYT4[7:0]	Programmable ADC biquad 9, D2 coefficient byte[7:0]	0x00		

Table 3-5. Programmable Coefficient Registers for Digital Biquad Filters 7-12 (continued)

Page 0x09 Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x44	ADC_BQ10_N0_BYT1[7:0]	Programmable ADC biquad 10, N0 coefficient byte[31:24]	0x7F	10	N_0
0x45	ADC_BQ10_N0_BYT2[7:0]	Programmable ADC biquad 10, N0 coefficient byte[23:16]	0xFF		
0x46	ADC_BQ10_N0_BYT3[7:0]	Programmable ADC biquad 10, N0 coefficient byte[15:8]	0xFF		
0x47	ADC_BQ10_N0_BYT4[7:0]	Programmable ADC biquad 10, N0 coefficient byte[7:0]	0xFF		
0x48	ADC_BQ10_N1_BYT1[7:0]	Programmable ADC biquad 10, N1 coefficient byte[31:24]	0x00		N_1
0x49	ADC_BQ10_N1_BYT2[7:0]	Programmable ADC biquad 10, N1 coefficient byte[23:16]	0x00		
0x4A	ADC_BQ10_N1_BYT3[7:0]	Programmable ADC biquad 10, N1 coefficient byte[15:8]	0x00		
0x4B	ADC_BQ10_N1_BYT4[7:0]	Programmable ADC biquad 10, N1 coefficient byte[7:0]	0x00		
0x4C	ADC_BQ10_N2_BYT1[7:0]	Programmable ADC biquad 10, N2 coefficient byte[31:24]	0x00		N_2
0x4D	ADC_BQ10_N2_BYT2[7:0]	Programmable ADC biquad 10, N2 coefficient byte[23:16]	0x00		
0x4E	ADC_BQ10_N2_BYT3[7:0]	Programmable ADC biquad 10, N2 coefficient byte[15:8]	0x00		
0x4F	ADC_BQ10_N2_BYT4[7:0]	Programmable ADC biquad 10, N2 coefficient byte[7:0]	0x00		
0x50	ADC_BQ10_D1_BYT1[7:0]	Programmable ADC biquad 10, D1 coefficient byte[31:24]	0x00		D_1
0x51	ADC_BQ10_D1_BYT2[7:0]	Programmable ADC biquad 10, D1 coefficient byte[23:16]	0x00		
0x52	ADC_BQ10_D1_BYT3[7:0]	Programmable ADC biquad 10, D1 coefficient byte[15:8]	0x00		
0x53	ADC_BQ10_D1_BYT4[7:0]	Programmable ADC biquad 10, D1 coefficient byte[7:0]	0x00		
0x54	ADC_BQ10_D2_BYT1[7:0]	Programmable ADC biquad 10, D2 coefficient byte[31:24]	0x00		D_2
0x55	ADC_BQ10_D2_BYT2[7:0]	Programmable ADC biquad 10, D2 coefficient byte[23:16]	0x00		
0x56	ADC_BQ10_D2_BYT3[7:0]	Programmable ADC biquad 10, D2 coefficient byte[15:8]	0x00		
0x57	ADC_BQ10_D2_BYT4[7:0]	Programmable ADC biquad 10, D2 coefficient byte[7:0]	0x00		

Table 3-5. Programmable Coefficient Registers for Digital Biquad Filters 7-12 (continued)

Page 0x09 Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x58	ADC_BQ11_N0_BYT1[7:0]	Programmable ADC biquad 11, N0 coefficient byte[31:24]	0x7F	11	N_0
0x59	ADC_BQ11_N0_BYT2[7:0]	Programmable ADC biquad 11, N0 coefficient byte[23:16]	0xFF		
0x5A	ADC_BQ11_N0_BYT3[7:0]	Programmable ADC biquad 11, N0 coefficient byte[15:8]	0xFF		
0x5B	ADC_BQ11_N0_BYT4[7:0]	Programmable ADC biquad 11, N0 coefficient byte[7:0]	0xFF		
0x5C	ADC_BQ11_N1_BYT1[7:0]	Programmable ADC biquad 11, N1 coefficient byte[31:24]	0x00		N_1
0x5D	ADC_BQ11_N1_BYT2[7:0]	Programmable ADC biquad 11, N1 coefficient byte[23:16]	0x00		
0x5E	ADC_BQ11_N1_BYT3[7:0]	Programmable ADC biquad 11, N1 coefficient byte[15:8]	0x00		
0x5F	ADC_BQ11_N1_BYT4[7:0]	Programmable ADC biquad 11, N1 coefficient byte[7:0]	0x00		
0x60	ADC_BQ11_N2_BYT1[7:0]	Programmable ADC biquad 11, N2 coefficient byte[31:24]	0x00		N_2
0x61	ADC_BQ11_N2_BYT2[7:0]	Programmable ADC biquad 11, N2 coefficient byte[23:16]	0x00		
0x62	ADC_BQ11_N2_BYT3[7:0]	Programmable ADC biquad 11, N2 coefficient byte[15:8]	0x00		
0x63	ADC_BQ11_N2_BYT4[7:0]	Programmable ADC biquad 11, N2 coefficient byte[7:0]	0x00		
0x64	ADC_BQ11_D1_BYT1[7:0]	Programmable ADC biquad 11, D1 coefficient byte[31:24]	0x00		D_1
0x65	ADC_BQ11_D1_BYT2[7:0]	Programmable ADC biquad 11, D1 coefficient byte[23:16]	0x00		
0x66	ADC_BQ11_D1_BYT3[7:0]	Programmable ADC biquad 11, D1 coefficient byte[15:8]	0x00		
0x67	ADC_BQ11_D1_BYT4[7:0]	Programmable ADC biquad 11, D1 coefficient byte[7:0]	0x00		
0x68	ADC_BQ11_D2_BYT1[7:0]	Programmable ADC biquad 11, D2 coefficient byte[31:24]	0x00		D_2
0x69	ADC_BQ11_D2_BYT2[7:0]	Programmable ADC biquad 11, D2 coefficient byte[23:16]	0x00		
0x6A	ADC_BQ11_D2_BYT3[7:0]	Programmable ADC biquad 11, D2 coefficient byte[15:8]	0x00		
0x6B	ADC_BQ11_D2_BYT4[7:0]	Programmable ADC biquad 11, D2 coefficient byte[7:0]	0x00		

Table 3-5. Programmable Coefficient Registers for Digital Biquad Filters 7-12 (continued)

Page 0x09 Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x6C	ADC_BQ12_N0_BYT1[7:0]	Programmable ADC biquad 12, N0 coefficient byte[31:24]	0x7F	12	N_0
0x6D	ADC_BQ12_N0_BYT2[7:0]	Programmable ADC biquad 12, N0 coefficient byte[23:16]	0xFF		
0x6E	ADC_BQ12_N0_BYT3[7:0]	Programmable ADC biquad 12, N0 coefficient byte[15:8]	0xFF		
0x6F	ADC_BQ12_N0_BYT4[7:0]	Programmable ADC biquad 12, N0 coefficient byte[7:0]	0xFF		
0x70	ADC_BQ12_N1_BYT1[7:0]	Programmable ADC biquad 12, N1 coefficient byte[31:24]	0x00		N_1
0x71	ADC_BQ12_N1_BYT2[7:0]	Programmable ADC biquad 12, N1 coefficient byte[23:16]	0x00		
0x72	ADC_BQ12_N1_BYT3[7:0]	Programmable ADC biquad 12, N1 coefficient byte[15:8]	0x00		
0x73	ADC_BQ12_N1_BYT4[7:0]	Programmable ADC biquad 12, N1 coefficient byte[7:0]	0x00		
0x74	ADC_BQ12_N2_BYT1[7:0]	Programmable ADC biquad 12, N2 coefficient byte[31:24]	0x00		N_2
0x75	ADC_BQ12_N2_BYT2[7:0]	Programmable ADC biquad 12, N2 coefficient byte[23:16]	0x00		
0x76	ADC_BQ12_N2_BYT3[7:0]	Programmable ADC biquad 12, N2 coefficient byte[15:8]	0x00		
0x77	ADC_BQ12_N2_BYT4[7:0]	Programmable ADC biquad 12, N2 coefficient byte[7:0]	0x00		
0x78	ADC_BQ12_D1_BYT1[7:0]	Programmable ADC biquad 12, D1 coefficient byte[31:24]	0x00		D_1
0x79	ADC_BQ12_D1_BYT2[7:0]	Programmable ADC biquad 12, D1 coefficient byte[23:16]	0x00		
0x7A	ADC_BQ12_D1_BYT3[7:0]	Programmable ADC biquad 12, D1 coefficient byte[15:8]	0x00		
0x7B	ADC_BQ12_D1_BYT4[7:0]	Programmable ADC biquad 12, D1 coefficient byte[7:0]	0x00		
0x7C	ADC_BQ12_D2_BYT1[7:0]	Programmable ADC biquad 12, D2 coefficient byte[31:24]	0x00		D_2
0x7D	ADC_BQ12_D2_BYT2[7:0]	Programmable ADC biquad 12, D2 coefficient byte[23:16]	0x00		
0x7E	ADC_BQ12_D2_BYT3[7:0]	Programmable ADC biquad 12, D2 coefficient byte[15:8]	0x00		
0x7F	ADC_BQ12_D2_BYT4[7:0]	Programmable ADC biquad 12, D2 coefficient byte[7:0]	0x00		

3.5 Biquad Filter Allocation on Playback Channel

Table 3-6 shows the assignment of these biquad filters to a specific channel on the DAC playback path based on the DAC_DSP_BQ_CFG[1:0] register setting of DSP_CFG1 (P0_R115) register. When no additional filtering is needed for the system application, setting DAC_DSP_BQ_CFG[1:0] to 2'b00 disables the Digital Biquad Filters for all channels. Table 3-7 also shows the mapping of the biquad filter coefficients in the TAC5x1x register space.

Table 3-6. Biquad Filter Allocation to the Playback Channel

Programmable Biquad Filter	Record Channel Allocation Using P0_R115_D[3:2] Register Setting		
	DAC_DSP_BQ_CFG[1:0] = 2'b01 (1 Biquad per Channel)	DAC_DSP_BQ_CFG[1:0] = 2'b10 (Default) (2 Biquads per Channel)	DAC_DSP_BQ_CFG[1:0] = 2'b11 (3 Biquads per Channel)
Biquad Filter 1	Allocated to output channel 1	Allocated to output channel 1	Allocated to output channel 1
Biquad Filter 2	Allocated to output channel 2	Allocated to output channel 2	Allocated to output channel 2
Biquad Filter 3	Allocated to output channel 3	Allocated to output channel 3	Allocated to output channel 3
Biquad Filter 4	Allocated to output channel 4	Allocated to output channel 4	Allocated to output channel 4
Biquad Filter 5	Not Used	Allocated to output channel 1	Allocated to output channel 1
Biquad Filter 6	Not Used	Allocated to output channel 2	Allocated to output channel 2
Biquad Filter 7	Not Used	Allocated to output channel 3	Allocated to output channel 3
Biquad Filter 8	Not Used	Allocated to output channel 4	Allocated to output channel 4
Biquad Filter 9	Not Used	Not Used	Allocated to output channel 1
Biquad Filter 10	Not Used	Not Used	Allocated to output channel 2
Biquad Filter 11	Not Used	Not Used	Allocated to output channel 3
Biquad Filter 12	Not Used	Not Used	Allocated to output channel 4

Table 3-7. Biquad Filter Coefficients Register Mapping for the Playback Channels

Biquad Filter	Register Mapping of Coefficients	Biquad Filter	Register Mapping of Coefficients
Biquad Filter 1	P15_R8 to P15_R27	Biquad Filter 7	P16_R8 to P16_R27
Biquad Filter 2	P15_R28 to P15_R47	Biquad Filter 8	P16_R28 to P16_R47
Biquad Filter 3	P15_R48 to P15_R67	Biquad Filter 9	P16_R48 to P16_R67
Biquad Filter 4	P15_R68 to P15_R87	Biquad Filter 10	P16_R68 to P16_R87
Biquad Filter 5	P15_R88 to P15_R107	Biquad Filter 11	P16_R88 to P16_R107
Biquad Filter 6	P15_R108 to P15_R127	Biquad Filter 12	P16_R108 to P16_R127

Table 3-8 shows the programmable coefficient registers of the biquad filters 1-6 in page 15 of the TAC5x1x registers.

Table 3-8. Programmable Coefficient Registers for Digital Biquad Filters 1–6

Page 0x0F Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x00	PAGE[7:0]	Device page register	0x00		
0x08	DAC_BQ1_N0_BYT1[7:0]	Programmable DAC biquad 1, N0 coefficient byte[31:24]	0x7F	1	N_0
0x09	DAC_BQ1_N0_BYT2[7:0]	Programmable DAC biquad 1, N0 coefficient byte[23:16]	0xFF		
0x0A	DAC_BQ1_N0_BYT3[7:0]	Programmable DAC biquad 1, N0 coefficient byte[15:8]	0xFF		
0x0B	DAC_BQ1_N0_BYT4[7:0]	Programmable DAC biquad 1, N0 coefficient byte[7:0]	0xFF		
0x0C	DAC_BQ1_N1_BYT1[7:0]	Programmable DAC biquad 1, N1 coefficient byte[31:24]	0x00		N_1
0x0D	DAC_BQ1_N1_BYT2[7:0]	Programmable DAC biquad 1, N1 coefficient byte[23:16]	0x00		
0x0E	DAC_BQ1_N1_BYT3[7:0]	Programmable DAC biquad 1, N1 coefficient byte[15:8]	0x00		
0x0F	DAC_BQ1_N1_BYT4[7:0]	Programmable DAC biquad 1, N1 coefficient byte[7:0]	0x00		
0x10	DAC_BQ1_N2_BYT1[7:0]	Programmable DAC biquad 1, N2 coefficient byte[31:24]	0x00		N_2
0x11	DAC_BQ1_N2_BYT2[7:0]	Programmable DAC biquad 1, N2 coefficient byte[23:16]	0x00		
0x12	DAC_BQ1_N2_BYT3[7:0]	Programmable DAC biquad 1, N2 coefficient byte[15:8]	0x00		
0x13	DAC_BQ1_N2_BYT4[7:0]	Programmable DAC biquad 1, N2 coefficient byte[7:0]	0x00		
0x14	DAC_BQ1_D1_BYT1[7:0]	Programmable DAC biquad 1, D1 coefficient byte[31:24]	0x00		D_1
0x15	DAC_BQ1_D1_BYT2[7:0]	Programmable DAC biquad 1, D1 coefficient byte[23:16]	0x00		
0x16	DAC_BQ1_D1_BYT3[7:0]	Programmable DAC biquad 1, D1 coefficient byte[15:8]	0x00		
0x17	DAC_BQ1_D1_BYT4[7:0]	Programmable DAC biquad 1, D1 coefficient byte[7:0]	0x00		
0x18	DAC_BQ1_D2_BYT1[7:0]	Programmable DAC biquad 1, D2 coefficient byte[31:24]	0x00		D_2
0x19	DAC_BQ1_D2_BYT2[7:0]	Programmable DAC biquad 1, D2 coefficient byte[23:16]	0x00		
0x1A	DAC_BQ1_D2_BYT3[7:0]	Programmable DAC biquad 1, D2 coefficient byte[15:8]	0x00		
0x1B	DAC_BQ1_D2_BYT4[7:0]	Programmable DAC biquad 1, D2 coefficient byte[7:0]	0x00		

Table 3-8. Programmable Coefficient Registers for Digital Biquad Filters 1–6 (continued)

Page 0x0F Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x1C	DAC_BQ2_N0_BYT1[7:0]	Programmable DAC biquad 2, N0 coefficient byte[31:24]	0x7F	2	N_0
0x1D	DAC_BQ2_N0_BYT2[7:0]	Programmable DAC biquad 2, N0 coefficient byte[23:16]	0xFF		
0x1E	DAC_BQ2_N0_BYT3[7:0]	Programmable DAC biquad 2, N0 coefficient byte[15:8]	0xFF		
0x1F	DAC_BQ2_N0_BYT4[7:0]	Programmable DAC biquad 2, N0 coefficient byte[7:0]	0xFF		
0x20	DAC_BQ2_N1_BYT1[7:0]	Programmable DAC biquad 2, N1 coefficient byte[31:24]	0x00		N_1
0x21	DAC_BQ2_N1_BYT2[7:0]	Programmable DAC biquad 2, N1 coefficient byte[23:16]	0x00		
0x22	DAC_BQ2_N1_BYT3[7:0]	Programmable DAC biquad 2, N1 coefficient byte[15:8]	0x00		
0x23	DAC_BQ2_N1_BYT4[7:0]	Programmable DAC biquad 2, N1 coefficient byte[7:0]	0x00		
0x24	DAC_BQ2_N2_BYT1[7:0]	Programmable DAC biquad 2, N2 coefficient byte[31:24]	0x00		N_2
0x25	DAC_BQ2_N2_BYT2[7:0]	Programmable DAC biquad 2, N2 coefficient byte[23:16]	0x00		
0x26	DAC_BQ2_N2_BYT3[7:0]	Programmable DAC biquad 2, N2 coefficient byte[15:8]	0x00		
0x27	DAC_BQ2_N2_BYT4[7:0]	Programmable DAC biquad 2, N2 coefficient byte[7:0]	0x00		
0x28	DAC_BQ2_D1_BYT1[7:0]	Programmable DAC biquad 2, D1 coefficient byte[31:24]	0x00		D_1
0x29	DAC_BQ2_D1_BYT2[7:0]	Programmable DAC biquad 2, D1 coefficient byte[23:16]	0x00		
0x2A	DAC_BQ2_D1_BYT3[7:0]	Programmable DAC biquad 2, D1 coefficient byte[15:8]	0x00		
0x2B	DAC_BQ2_D1_BYT4[7:0]	Programmable DAC biquad 2, D1 coefficient byte[7:0]	0x00		
0x2C	DAC_BQ2_D2_BYT1[7:0]	Programmable DAC biquad 2, D2 coefficient byte[31:24]	0x00		D_2
0x2D	DAC_BQ2_D2_BYT2[7:0]	Programmable DAC biquad 2, D2 coefficient byte[23:16]	0x00		
0x2E	DAC_BQ2_D2_BYT3[7:0]	Programmable DAC biquad 2, D2 coefficient byte[15:8]	0x00		
0x2F	DAC_BQ2_D2_BYT4[7:0]	Programmable DAC biquad 2, D2 coefficient byte[7:0]	0x00		

Table 3-8. Programmable Coefficient Registers for Digital Biquad Filters 1–6 (continued)

Page 0x0F Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x30	DAC_BQ3_N0_BYT1[7:0]	Programmable DAC biquad 3, N0 coefficient byte[31:24]	0x7F	3	N_0
0x31	DAC_BQ3_N0_BYT2[7:0]	Programmable DAC biquad 3, N0 coefficient byte[23:16]	0xFF		
0x32	DAC_BQ3_N0_BYT3[7:0]	Programmable DAC biquad 3, N0 coefficient byte[15:8]	0xFF		
0x33	DAC_BQ3_N0_BYT4[7:0]	Programmable DAC biquad 3, N0 coefficient byte[7:0]	0xFF		
0x34	DAC_BQ3_N1_BYT1[7:0]	Programmable DAC biquad 3, N1 coefficient byte[31:24]	0x00		N_1
0x35	DAC_BQ3_N1_BYT2[7:0]	Programmable DAC biquad 3, N1 coefficient byte[23:16]	0x00		
0x36	DAC_BQ3_N1_BYT3[7:0]	Programmable DAC biquad 3, N1 coefficient byte[15:8]	0x00		
0x37	DAC_BQ3_N1_BYT4[7:0]	Programmable DAC biquad 3, N1 coefficient byte[7:0]	0x00		
0x38	DAC_BQ3_N2_BYT1[7:0]	Programmable DAC biquad 3, N2 coefficient byte[31:24]	0x00		N_2
0x39	DAC_BQ3_N2_BYT2[7:0]	Programmable DAC biquad 3, N2 coefficient byte[23:16]	0x00		
0x3A	DAC_BQ3_N2_BYT3[7:0]	Programmable DAC biquad 3, N2 coefficient byte[15:8]	0x00		
0x3B	DAC_BQ3_N2_BYT4[7:0]	Programmable DAC biquad 3, N2 coefficient byte[7:0]	0x00		
0x3C	DAC_BQ3_D1_BYT1[7:0]	Programmable DAC biquad 3, D1 coefficient byte[31:24]	0x00		D_1
0x3D	DAC_BQ3_D1_BYT2[7:0]	Programmable DAC biquad 3, D1 coefficient byte[23:16]	0x00		
0x3E	DAC_BQ3_D1_BYT3[7:0]	Programmable DAC biquad 3, D1 coefficient byte[15:8]	0x00		
0x3F	DAC_BQ3_D1_BYT4[7:0]	Programmable DAC biquad 3, D1 coefficient byte[7:0]	0x00		
0x40	DAC_BQ3_D2_BYT1[7:0]	Programmable DAC biquad 3, D2 coefficient byte[31:24]	0x00		D_2
0x41	DAC_BQ3_D2_BYT2[7:0]	Programmable DAC biquad 3, D2 coefficient byte[23:16]	0x00		
0x42	DAC_BQ3_D2_BYT3[7:0]	Programmable DAC biquad 3, D2 coefficient byte[15:8]	0x00		
0x43	DAC_BQ3_D2_BYT4[7:0]	Programmable DAC biquad 3, D2 coefficient byte[7:0]	0x00		

Table 3-8. Programmable Coefficient Registers for Digital Biquad Filters 1–6 (continued)

Page 0x0F Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x44	DAC_BQ4_N0_BYT1[7:0]	Programmable DAC biquad 4, N0 coefficient byte[31:24]	0x7F	4	N_0
0x45	DAC_BQ4_N0_BYT2[7:0]	Programmable DAC biquad 4, N0 coefficient byte[23:16]	0xFF		
0x46	DAC_BQ4_N0_BYT3[7:0]	Programmable DAC biquad 4, N0 coefficient byte[15:8]	0xFF		
0x47	DAC_BQ4_N0_BYT4[7:0]	Programmable DAC biquad 4, N0 coefficient byte[7:0]	0xFF		
0x48	DAC_BQ4_N1_BYT1[7:0]	Programmable DAC biquad 4, N1 coefficient byte[31:24]	0x00		N_1
0x49	DAC_BQ4_N1_BYT2[7:0]	Programmable DAC biquad 4, N1 coefficient byte[23:16]	0x00		
0x4A	DAC_BQ4_N1_BYT3[7:0]	Programmable DAC biquad 4, N1 coefficient byte[15:8]	0x00		
0x4B	DAC_BQ4_N1_BYT4[7:0]	Programmable DAC biquad 4, N1 coefficient byte[7:0]	0x00		
0x4C	DAC_BQ4_N2_BYT1[7:0]	Programmable DAC biquad 4, N2 coefficient byte[31:24]	0x00		N_2
0x4D	DAC_BQ4_N2_BYT2[7:0]	Programmable DAC biquad 4, N2 coefficient byte[23:16]	0x00		
0x4E	DAC_BQ4_N2_BYT3[7:0]	Programmable DAC biquad 4, N2 coefficient byte[15:8]	0x00		
0x4F	DAC_BQ4_N2_BYT4[7:0]	Programmable DAC biquad 4, N2 coefficient byte[7:0]	0x00		
0x50	DAC_BQ4_D1_BYT1[7:0]	Programmable DAC biquad 4, D1 coefficient byte[31:24]	0x00		D_1
0x51	DAC_BQ4_D1_BYT2[7:0]	Programmable DAC biquad 4, D1 coefficient byte[23:16]	0x00		
0x52	DAC_BQ4_D1_BYT3[7:0]	Programmable DAC biquad 4, D1 coefficient byte[15:8]	0x00		
0x53	DAC_BQ4_D1_BYT4[7:0]	Programmable DAC biquad 4, D1 coefficient byte[7:0]	0x00		
0x54	DAC_BQ4_D2_BYT1[7:0]	Programmable DAC biquad 4, D2 coefficient byte[31:24]	0x00		D_2
0x55	DAC_BQ4_D2_BYT2[7:0]	Programmable DAC biquad 4, D2 coefficient byte[23:16]	0x00		
0x56	DAC_BQ4_D2_BYT3[7:0]	Programmable DAC biquad 4, D2 coefficient byte[15:8]	0x00		
0x57	DAC_BQ4_D2_BYT4[7:0]	Programmable DAC biquad 4, D2 coefficient byte[7:0]	0x00		

Table 3-8. Programmable Coefficient Registers for Digital Biquad Filters 1–6 (continued)

Page 0x0F Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x58	DAC_BQ5_N0_BYT1[7:0]	Programmable DAC biquad 5, N0 coefficient byte[31:24]	0x7F	5	N_0
0x59	DAC_BQ5_N0_BYT2[7:0]	Programmable DAC biquad 5, N0 coefficient byte[23:16]	0xFF		
0x5A	DAC_BQ5_N0_BYT3[7:0]	Programmable DAC biquad 5, N0 coefficient byte[15:8]	0xFF		
0x5B	DAC_BQ5_N0_BYT4[7:0]	Programmable DAC biquad 5, N0 coefficient byte[7:0]	0xFF		
0x5C	DAC_BQ5_N1_BYT1[7:0]	Programmable DAC biquad 5, N1 coefficient byte[31:24]	0x00		N_1
0x5D	DAC_BQ5_N1_BYT2[7:0]	Programmable DAC biquad 5, N1 coefficient byte[23:16]	0x00		
0x5E	DAC_BQ5_N1_BYT3[7:0]	Programmable DAC biquad 5, N1 coefficient byte[15:8]	0x00		
0x5F	DAC_BQ5_N1_BYT4[7:0]	Programmable DAC biquad 5, N1 coefficient byte[7:0]	0x00		
0x60	DAC_BQ5_N2_BYT1[7:0]	Programmable DAC biquad 5, N2 coefficient byte[31:24]	0x00		N_2
0x61	DAC_BQ5_N2_BYT2[7:0]	Programmable DAC biquad 5, N2 coefficient byte[23:16]	0x00		
0x62	DAC_BQ5_N2_BYT3[7:0]	Programmable DAC biquad 5, N2 coefficient byte[15:8]	0x00		
0x63	DAC_BQ5_N2_BYT4[7:0]	Programmable DAC biquad 5, N2 coefficient byte[7:0]	0x00		
0x64	DAC_BQ5_D1_BYT1[7:0]	Programmable DAC biquad 5, D1 coefficient byte[31:24]	0x00		D_1
0x65	DAC_BQ5_D1_BYT2[7:0]	Programmable DAC biquad 5, D1 coefficient byte[23:16]	0x00		
0x66	DAC_BQ5_D1_BYT3[7:0]	Programmable DAC biquad 5, D1 coefficient byte[15:8]	0x00		
0x67	DAC_BQ5_D1_BYT4[7:0]	Programmable DAC biquad 5, D1 coefficient byte[7:0]	0x00		
0x68	DAC_BQ5_D2_BYT1[7:0]	Programmable DAC biquad 5, D2 coefficient byte[31:24]	0x00		D_2
0x69	DAC_BQ5_D2_BYT2[7:0]	Programmable DAC biquad 5, D2 coefficient byte[23:16]	0x00		
0x6A	DAC_BQ5_D2_BYT3[7:0]	Programmable DAC biquad 5, D2 coefficient byte[15:8]	0x00		
0x6B	DAC_BQ5_D2_BYT4[7:0]	Programmable DAC biquad 5, D2 coefficient byte[7:0]	0x00		

Table 3-8. Programmable Coefficient Registers for Digital Biquad Filters 1–6 (continued)

Page 0x0F Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x6C	DAC_BQ6_N0_BYT1[7:0]	Programmable DAC biquad 6, N0 coefficient byte[31:24]	0x7F	6	N_0
0x6D	DAC_BQ6_N0_BYT2[7:0]	Programmable DAC biquad 6, N0 coefficient byte[23:16]	0xFF		
0x6E	DAC_BQ6_N0_BYT3[7:0]	Programmable DAC biquad 6, N0 coefficient byte[15:8]	0xFF		
0x6F	DAC_BQ6_N0_BYT4[7:0]	Programmable DAC biquad 6, N0 coefficient byte[7:0]	0xFF		
0x70	DAC_BQ6_N1_BYT1[7:0]	Programmable DAC biquad 6, N1 coefficient byte[31:24]	0x00		N_1
0x71	DAC_BQ6_N1_BYT2[7:0]	Programmable DAC biquad 6, N1 coefficient byte[23:16]	0x00		
0x72	DAC_BQ6_N1_BYT3[7:0]	Programmable DAC biquad 6, N1 coefficient byte[15:8]	0x00		
0x73	DAC_BQ6_N1_BYT4[7:0]	Programmable DAC biquad 6, N1 coefficient byte[7:0]	0x00		
0x74	DAC_BQ6_N2_BYT1[7:0]	Programmable DAC biquad 6, N2 coefficient byte[31:24]	0x00		N_2
0x75	DAC_BQ6_N2_BYT2[7:0]	Programmable DAC biquad 6, N2 coefficient byte[23:16]	0x00		
0x76	DAC_BQ6_N2_BYT3[7:0]	Programmable DAC biquad 6, N2 coefficient byte[15:8]	0x00		
0x77	DAC_BQ6_N2_BYT4[7:0]	Programmable DAC biquad 6, N2 coefficient byte[7:0]	0x00		
0x78	DAC_BQ6_D1_BYT1[7:0]	Programmable DAC biquad 6, D1 coefficient byte[31:24]	0x00		D_1
0x79	DAC_BQ6_D1_BYT2[7:0]	Programmable DAC biquad 6, D1 coefficient byte[23:16]	0x00		
0x7A	DAC_BQ6_D1_BYT3[7:0]	Programmable DAC biquad 6, D1 coefficient byte[15:8]	0x00		
0x7B	DAC_BQ6_D1_BYT4[7:0]	Programmable DAC biquad 6, D1 coefficient byte[7:0]	0x00		
0x7C	DAC_BQ6_D2_BYT1[7:0]	Programmable DAC biquad 6, D2 coefficient byte[31:24]	0x00		D_2
0x7D	DAC_BQ6_D2_BYT2[7:0]	Programmable DAC biquad 6, D2 coefficient byte[23:16]	0x00		
0x7E	DAC_BQ6_D2_BYT3[7:0]	Programmable DAC biquad 6, D2 coefficient byte[15:8]	0x00		
0x7F	DAC_BQ6_D2_BYT4[7:0]	Programmable DAC biquad 6, D2 coefficient byte[7:0]	0x00		

Similarly, Table 3-9 shows the programmable coefficient registers of the biquad filters 1-6 in page 16 of the TAC5x1x registers.

Table 3-9. Programmable Coefficient Registers for Digital Biquad Filters 7-12

Page 0x10 Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x00	PAGE[7:0]	Device page register	0x00		
0x08	DAC_BQ7_N0_BYT1[7:0]	Programmable DAC biquad 7, N0 coefficient byte[31:24]	0x7F	7	N0
0x09	DAC_BQ7_N0_BYT2[7:0]	Programmable DAC biquad 7, N0 coefficient byte[23:16]	0xFF		
0x0A	DAC_BQ7_N0_BYT3[7:0]	Programmable DAC biquad 7, N0 coefficient byte[15:8]	0xFF		
0x0B	DAC_BQ7_N0_BYT4[7:0]	Programmable DAC biquad 7, N0 coefficient byte[7:0]	0xFF		
0x0C	DAC_BQ7_N1_BYT1[7:0]	Programmable DAC biquad 7, N1 coefficient byte[31:24]	0x00		N1
0x0D	DAC_BQ7_N1_BYT2[7:0]	Programmable DAC biquad 7, N1 coefficient byte[23:16]	0x00		
0x0E	DAC_BQ7_N1_BYT3[7:0]	Programmable DAC biquad 7, N1 coefficient byte[15:8]	0x00		
0x0F	DAC_BQ7_N1_BYT4[7:0]	Programmable DAC biquad 7, N1 coefficient byte[7:0]	0x00		
0x10	DAC_BQ7_N2_BYT1[7:0]	Programmable DAC biquad 7, N2 coefficient byte[31:24]	0x00		N2
0x11	DAC_BQ7_N2_BYT2[7:0]	Programmable DAC biquad 7, N2 coefficient byte[23:16]	0x00		
0x12	DAC_BQ7_N2_BYT3[7:0]	Programmable DAC biquad 7, N2 coefficient byte[15:8]	0x00		
0x13	DAC_BQ7_N2_BYT4[7:0]	Programmable DAC biquad 7, N2 coefficient byte[7:0]	0x00		
0x14	DAC_BQ7_D1_BYT1[7:0]	Programmable DAC biquad 7, D1 coefficient byte[31:24]	0x00		D1
0x15	DAC_BQ7_D1_BYT2[7:0]	Programmable DAC biquad 7, D1 coefficient byte[23:16]	0x00		
0x16	DAC_BQ7_D1_BYT3[7:0]	Programmable DAC biquad 7, D1 coefficient byte[15:8]	0x00		
0x17	DAC_BQ7_D1_BYT4[7:0]	Programmable DAC biquad 7, D1 coefficient byte[7:0]	0x00		
0x18	DAC_BQ7_D2_BYT1[7:0]	Programmable DAC biquad 7, D2 coefficient byte[31:24]	0x00		D2
0x19	DAC_BQ7_D2_BYT2[7:0]	Programmable DAC biquad 7, D2 coefficient byte[23:16]	0x00		
0x1A	DAC_BQ7_D2_BYT3[7:0]	Programmable DAC biquad 7, D2 coefficient byte[15:8]	0x00		
0x1B	DAC_BQ7_D2_BYT4[7:0]	Programmable DAC biquad 7, D2 coefficient byte[7:0]	0x00		

Table 3-9. Programmable Coefficient Registers for Digital Biquad Filters 7-12 (continued)

Page 0x10 Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x1C	DAC_BQ8_N0_BYT1[7:0]	Programmable DAC biquad 8, N0 coefficient byte[31:24]	0x7F	8	N0
0x1D	DAC_BQ8_N0_BYT2[7:0]	Programmable DAC biquad 8, N0 coefficient byte[23:16]	0xFF		
0x1E	DAC_BQ8_N0_BYT3[7:0]	Programmable DAC biquad 8, N0 coefficient byte[15:8]	0xFF		
0x1F	DAC_BQ8_N0_BYT4[7:0]	Programmable DAC biquad 8, N0 coefficient byte[7:0]	0xFF		
0x20	DAC_BQ8_N1_BYT1[7:0]	Programmable DAC biquad 8, N1 coefficient byte[31:24]	0x00		N1
0x21	DAC_BQ8_N1_BYT2[7:0]	Programmable DAC biquad 8, N1 coefficient byte[23:16]	0x00		
0x22	DAC_BQ8_N1_BYT3[7:0]	Programmable DAC biquad 8, N1 coefficient byte[15:8]	0x00		
0x23	DAC_BQ8_N1_BYT4[7:0]	Programmable DAC biquad 8, N1 coefficient byte[7:0]	0x00		
0x24	DAC_BQ8_N2_BYT1[7:0]	Programmable DAC biquad 8, N2 coefficient byte[31:24]	0x00		N2
0x25	DAC_BQ8_N2_BYT2[7:0]	Programmable DAC biquad 8, N2 coefficient byte[23:16]	0x00		
0x26	DAC_BQ8_N2_BYT3[7:0]	Programmable DAC biquad 8, N2 coefficient byte[15:8]	0x00		
0x27	DAC_BQ8_N2_BYT4[7:0]	Programmable DAC biquad 8, N2 coefficient byte[7:0]	0x00		
0x28	DAC_BQ8_D1_BYT1[7:0]	Programmable DAC biquad 8, D1 coefficient byte[31:24]	0x00		D1
0x29	DAC_BQ8_D1_BYT2[7:0]	Programmable DAC biquad 8, D1 coefficient byte[23:16]	0x00		
0x2A	DAC_BQ8_D1_BYT3[7:0]	Programmable DAC biquad 8, D1 coefficient byte[15:8]	0x00		
0x2B	DAC_BQ8_D1_BYT4[7:0]	Programmable DAC biquad 8, D1 coefficient byte[7:0]	0x00		
0x2C	DAC_BQ8_D2_BYT1[7:0]	Programmable DAC biquad 8, D2 coefficient byte[31:24]	0x00		D2
0x2D	DAC_BQ8_D2_BYT2[7:0]	Programmable DAC biquad 8, D2 coefficient byte[23:16]	0x00		
0x2E	DAC_BQ8_D2_BYT3[7:0]	Programmable DAC biquad 8, D2 coefficient byte[15:8]	0x00		
0x2F	DAC_BQ8_D2_BYT4[7:0]	Programmable DAC biquad 8, D2 coefficient byte[7:0]	0x00		

Table 3-9. Programmable Coefficient Registers for Digital Biquad Filters 7-12 (continued)

Page 0x10 Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x30	DAC_BQ9_N0_BYT1[7:0]	Programmable DAC biquad 9, N0 coefficient byte[31:24]	0x7F	9	N0
0x31	DAC_BQ9_N0_BYT2[7:0]	Programmable DAC biquad 9, N0 coefficient byte[23:16]	0xFF		
0x32	DAC_BQ9_N0_BYT3[7:0]	Programmable DAC biquad 9, N0 coefficient byte[15:8]	0xFF		
0x33	DAC_BQ9_N0_BYT4[7:0]	Programmable DAC biquad 9, N0 coefficient byte[7:0]	0xFF		
0x34	DAC_BQ9_N1_BYT1[7:0]	Programmable DAC biquad 9, N1 coefficient byte[31:24]	0x00		N1
0x35	DAC_BQ9_N1_BYT2[7:0]	Programmable DAC biquad 9, N1 coefficient byte[23:16]	0x00		
0x36	DAC_BQ9_N1_BYT3[7:0]	Programmable DAC biquad 9, N1 coefficient byte[15:8]	0x00		
0x37	DAC_BQ9_N1_BYT4[7:0]	Programmable DAC biquad 9, N1 coefficient byte[7:0]	0x00		
0x38	DAC_BQ9_N2_BYT1[7:0]	Programmable DAC biquad 9, N2 coefficient byte[31:24]	0x00		N2
0x39	DAC_BQ9_N2_BYT2[7:0]	Programmable DAC biquad 9, N2 coefficient byte[23:16]	0x00		
0x3A	DAC_BQ9_N2_BYT3[7:0]	Programmable DAC biquad 9, N2 coefficient byte[15:8]	0x00		
0x3B	DAC_BQ9_N2_BYT4[7:0]	Programmable DAC biquad 9, N2 coefficient byte[7:0]	0x00		
0x3C	DAC_BQ9_D1_BYT1[7:0]	Programmable DAC biquad 9, D1 coefficient byte[31:24]	0x00		D1
0x3D	DAC_BQ9_D1_BYT2[7:0]	Programmable DAC biquad 9, D1 coefficient byte[23:16]	0x00		
0x3E	DAC_BQ9_D1_BYT3[7:0]	Programmable DAC biquad 9, D1 coefficient byte[15:8]	0x00		
0x3F	DAC_BQ9_D1_BYT4[7:0]	Programmable DAC biquad 9, D1 coefficient byte[7:0]	0x00		
0x40	DAC_BQ9_D2_BYT1[7:0]	Programmable DAC biquad 9, D2 coefficient byte[31:24]	0x00		D2
0x41	DAC_BQ9_D2_BYT2[7:0]	Programmable DAC biquad 9, D2 coefficient byte[23:16]	0x00		
0x42	DAC_BQ9_D2_BYT3[7:0]	Programmable DAC biquad 9, D2 coefficient byte[15:8]	0x00		
0x43	DAC_BQ9_D2_BYT4[7:0]	Programmable DAC biquad 9, D2 coefficient byte[7:0]	0x00		

Table 3-9. Programmable Coefficient Registers for Digital Biquad Filters 7-12 (continued)

Page 0x10 Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x44	DAC_BQ10_N0_BYT1[7:0]	Programmable DAC biquad 10, N0 coefficient byte[31:24]	0x7F	10	N0
0x45	DAC_BQ10_N0_BYT2[7:0]	Programmable DAC biquad 10, N0 coefficient byte[23:16]	0xFF		
0x46	DAC_BQ10_N0_BYT3[7:0]	Programmable DAC biquad 10, N0 coefficient byte[15:8]	0xFF		
0x47	DAC_BQ10_N0_BYT4[7:0]	Programmable DAC biquad 10, N0 coefficient byte[7:0]	0xFF		
0x48	DAC_BQ10_N1_BYT1[7:0]	Programmable DAC biquad 10, N1 coefficient byte[31:24]	0x00		N1
0x49	DAC_BQ10_N1_BYT2[7:0]	Programmable DAC biquad 10, N1 coefficient byte[23:16]	0x00		
0x4A	DAC_BQ10_N1_BYT3[7:0]	Programmable DAC biquad 10, N1 coefficient byte[15:8]	0x00		
0x4B	DAC_BQ10_N1_BYT4[7:0]	Programmable DAC biquad 10, N1 coefficient byte[7:0]	0x00		
0x4C	DAC_BQ10_N2_BYT1[7:0]	Programmable DAC biquad 10, N2 coefficient byte[31:24]	0x00		N2
0x4D	DAC_BQ10_N2_BYT2[7:0]	Programmable DAC biquad 10, N2 coefficient byte[23:16]	0x00		
0x4E	DAC_BQ10_N2_BYT3[7:0]	Programmable DAC biquad 10, N2 coefficient byte[15:8]	0x00		
0x4F	DAC_BQ10_N2_BYT4[7:0]	Programmable DAC biquad 10, N2 coefficient byte[7:0]	0x00		
0x50	DAC_BQ10_D1_BYT1[7:0]	Programmable DAC biquad 10, D1 coefficient byte[31:24]	0x00		D1
0x51	DAC_BQ10_D1_BYT2[7:0]	Programmable DAC biquad 10, D1 coefficient byte[23:16]	0x00		
0x52	DAC_BQ10_D1_BYT3[7:0]	Programmable DAC biquad 10, D1 coefficient byte[15:8]	0x00		
0x53	DAC_BQ10_D1_BYT4[7:0]	Programmable DAC biquad 10, D1 coefficient byte[7:0]	0x00		
0x54	DAC_BQ10_D2_BYT1[7:0]	Programmable DAC biquad 10, D2 coefficient byte[31:24]	0x00		D2
0x55	DAC_BQ10_D2_BYT2[7:0]	Programmable DAC biquad 10, D2 coefficient byte[23:16]	0x00		
0x56	DAC_BQ10_D2_BYT3[7:0]	Programmable DAC biquad 10, D2 coefficient byte[15:8]	0x00		
0x57	DAC_BQ10_D2_BYT4[7:0]	Programmable DAC biquad 10, D2 coefficient byte[7:0]	0x00		

Table 3-9. Programmable Coefficient Registers for Digital Biquad Filters 7-12 (continued)

Page 0x10 Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x58	DAC_BQ11_N0_BYT1[7:0]	Programmable DAC biquad 11, N0 coefficient byte[31:24]	0x7F	11	N0
0x59	DAC_BQ11_N0_BYT2[7:0]	Programmable DAC biquad 11, N0 coefficient byte[23:16]	0xFF		
0x5A	DAC_BQ11_N0_BYT3[7:0]	Programmable DAC biquad 11, N0 coefficient byte[15:8]	0xFF		
0x5B	DAC_BQ11_N0_BYT4[7:0]	Programmable DAC biquad 11, N0 coefficient byte[7:0]	0xFF		
0x5C	DAC_BQ11_N1_BYT1[7:0]	Programmable DAC biquad 11, N1 coefficient byte[31:24]	0x00		N1
0x5D	DAC_BQ11_N1_BYT2[7:0]	Programmable DAC biquad 11, N1 coefficient byte[23:16]	0x00		
0x5E	DAC_BQ11_N1_BYT3[7:0]	Programmable DAC biquad 11, N1 coefficient byte[15:8]	0x00		
0x5F	DAC_BQ11_N1_BYT4[7:0]	Programmable DAC biquad 11, N1 coefficient byte[7:0]	0x00		
0x60	DAC_BQ11_N2_BYT1[7:0]	Programmable DAC biquad 11, N2 coefficient byte[31:24]	0x00		N2
0x61	DAC_BQ11_N2_BYT2[7:0]	Programmable DAC biquad 11, N2 coefficient byte[23:16]	0x00		
0x62	DAC_BQ11_N2_BYT3[7:0]	Programmable DAC biquad 11, N2 coefficient byte[15:8]	0x00		
0x63	DAC_BQ11_N2_BYT4[7:0]	Programmable DAC biquad 11, N2 coefficient byte[7:0]	0x00		
0x64	DAC_BQ11_D1_BYT1[7:0]	Programmable DAC biquad 11, D1 coefficient byte[31:24]	0x00		D1
0x65	DAC_BQ11_D1_BYT2[7:0]	Programmable DAC biquad 11, D1 coefficient byte[23:16]	0x00		
0x66	DAC_BQ11_D1_BYT3[7:0]	Programmable DAC biquad 11, D1 coefficient byte[15:8]	0x00		
0x67	DAC_BQ11_D1_BYT4[7:0]	Programmable DAC biquad 11, D1 coefficient byte[7:0]	0x00		
0x68	DAC_BQ11_D2_BYT1[7:0]	Programmable DAC biquad 11, D2 coefficient byte[31:24]	0x00		D2
0x69	DAC_BQ11_D2_BYT2[7:0]	Programmable DAC biquad 11, D2 coefficient byte[23:16]	0x00		
0x6A	DAC_BQ11_D2_BYT3[7:0]	Programmable DAC biquad 11, D2 coefficient byte[15:8]	0x00		
0x6B	DAC_BQ11_D2_BYT4[7:0]	Programmable DAC biquad 11, D2 coefficient byte[7:0]	0x00		

Table 3-9. Programmable Coefficient Registers for Digital Biquad Filters 7-12 (continued)

Page 0x10 Address	Register	Register Description	Reset Value	Biquad Filter	Coefficient
0x6C	DAC_BQ12_N0_BYT1[7:0]	Programmable DAC biquad 12, N0 coefficient byte[31:24]	0x7F	12	N0
0x6D	DAC_BQ12_N0_BYT2[7:0]	Programmable DAC biquad 12, N0 coefficient byte[23:16]	0xFF		
0x6E	DAC_BQ12_N0_BYT3[7:0]	Programmable DAC biquad 12, N0 coefficient byte[15:8]	0xFF		
0x6F	DAC_BQ12_N0_BYT4[7:0]	Programmable DAC biquad 12, N0 coefficient byte[7:0]	0xFF		
0x70	DAC_BQ12_N1_BYT1[7:0]	Programmable DAC biquad 12, N1 coefficient byte[31:24]	0x00		N1
0x71	DAC_BQ12_N1_BYT2[7:0]	Programmable DAC biquad 12, N1 coefficient byte[23:16]	0x00		
0x72	DAC_BQ12_N1_BYT3[7:0]	Programmable DAC biquad 12, N1 coefficient byte[15:8]	0x00		
0x73	DAC_BQ12_N1_BYT4[7:0]	Programmable DAC biquad 12, N1 coefficient byte[7:0]	0x00		
0x74	DAC_BQ12_N2_BYT1[7:0]	Programmable DAC biquad 12, N2 coefficient byte[31:24]	0x00		N2
0x75	DAC_BQ12_N2_BYT2[7:0]	Programmable DAC biquad 12, N2 coefficient byte[23:16]	0x00		
0x76	DAC_BQ12_N2_BYT3[7:0]	Programmable DAC biquad 12, N2 coefficient byte[15:8]	0x00		
0x77	DAC_BQ12_N2_BYT4[7:0]	Programmable DAC biquad 12, N2 coefficient byte[7:0]	0x00		
0x78	DAC_BQ12_D1_BYT1[7:0]	Programmable DAC biquad 12, D1 coefficient byte[31:24]	0x00		D1
0x79	DAC_BQ12_D1_BYT2[7:0]	Programmable DAC biquad 12, D1 coefficient byte[23:16]	0x00		
0x7A	DAC_BQ12_D1_BYT3[7:0]	Programmable DAC biquad 12, D1 coefficient byte[15:8]	0x00		
0x7B	DAC_BQ12_D1_BYT4[7:0]	Programmable DAC biquad 12, D1 coefficient byte[7:0]	0x00		
0x7C	DAC_BQ12_D2_BYT1[7:0]	Programmable DAC biquad 12, D2 coefficient byte[31:24]	0x00		D2
0x7D	DAC_BQ12_D2_BYT2[7:0]	Programmable DAC biquad 12, D2 coefficient byte[23:16]	0x00		
0x7E	DAC_BQ12_D2_BYT3[7:0]	Programmable DAC biquad 12, D2 coefficient byte[15:8]	0x00		
0x7F	DAC_BQ12_D2_BYT4[7:0]	Programmable DAC biquad 12, D2 coefficient byte[7:0]	0x00		

3.6 Biquad Filter Programming Example on the TAC5x1x

Coefficients of Digital Biquad Filters can be implemented by running a command script to send an I^2C command to the EVM. The following script segment shows how to program the coefficients for a set of filters for 5dB boost at 500Hz with bandwidth of 400Hz, cut –5dB at 4kHz with 5kHz bandwidth, and a notch filter at 60Hz with 50Hz bandwidth on channel 1 of the recording path, with the frequency response being as shown in Figure 3-3. Here, the filter coefficients are programmed as follows:

- Filter 1: N_0 = 0x7FFFFFFF, N_1 = 0x85F4B2CB, N_2 = 0x749CADCB, D_1 = 0x7C77A718, D_2 = 0x8687F4EE
- Filter 2: N_0 = 0x6B645FE5, N_1 = 0xB9ED52C9, N_2 = 0x366F3978, D_1 = 0x4612AD37, D_2 = 0xDE2C66A1
- Filter 3: N_0 = 0x7F951DC9, N_1 = 0x806BE418, N_2 = 0x7F951DC9, D_1 = 0x7F941BE8, D_2 = 0x80D5C46D

```
#Select Page 8
w a0 00 08
#Program coefficients N0, N1, N2, D1, D2 of biquad filter 1
w a0 08 7f ff ff ff 85 f4 b2 cb 74 9c ad cb 7c 77 a7 18 86 87 f4 ee
#Program coefficients N0, N1, N2, D1, D2 of biquad filter 5
w a0 58 6b 64 5f e5 b9 ed 52 c9 36 6f 39 78 46 12 ad 37 de 2c 66 a1
#Select Page 9
w a0 00 09
#Program coefficients N0, N1, N2, D1, D2 of biquad filter 9
w a0 30 7f 95 1d c9 80 6b e4 18 7f 95 1d c9 7f 94 1b e8 80 d5 c4 6d
```

Similarly, following script segment shows how to program the coefficients for a set of filters including a Low Pass Butterworth at 8kHz, a notch filter at 60Hz with 50Hz bandwidth, and an equalizer that boosts 6dB at 4kHz with a bandwidth of 2kHz on channel 1 of the playback path, with the frequency response being as shown in Figure 3-5. Here, the filter coefficients are programmed as follows:

- Filter 1: N_0 = 0x13D8B646, N_1 = 0x13D8B646, N_2 = 0x13D8B646, D_1 = 0x27B16C8C, D_2 = 0xE13A4DCD
- Filter 2: N_0 = 0x7F951DC9, N_1 = 0x806BE418, N_2 = 0x7F951DC9, D_1 = 0x7F941BE8, D_2 = 0x80D5C46D
- Filter 3: N_0 = 0x7FFFFFFF, N_1 = 0xA81AE64B, N_2 = 0x4AFC10C8, D_1 = 0x62053997, D_2 = 0x9DA1ADE4

```
#Select Page 15
w a0 00 0f
#Program coefficients N0, N1, N2, D1, D2 of biquad filter 1
w a0 08 13 d8 b6 46 13 d8 b6 46 13 d8 b6 46 27 b1 6c 8c e1 3a 4d cd
#Program coefficients N0, N1, N2, D1, D2 of biquad filter 5
w a0 58 7f 95 1d c9 80 6b e4 18 7f 95 1d c9 7f 94 1b e8 80 d5 c4 6d
#Select Page 16
w a0 00 10
#Program coefficients N0, N1, N2, D1, D2 of biquad filter 9
w a0 30 7f ff ff ff a8 1a e6 4b 4a fc 10 c8 62 05 39 97 9d a1 ad e4
```

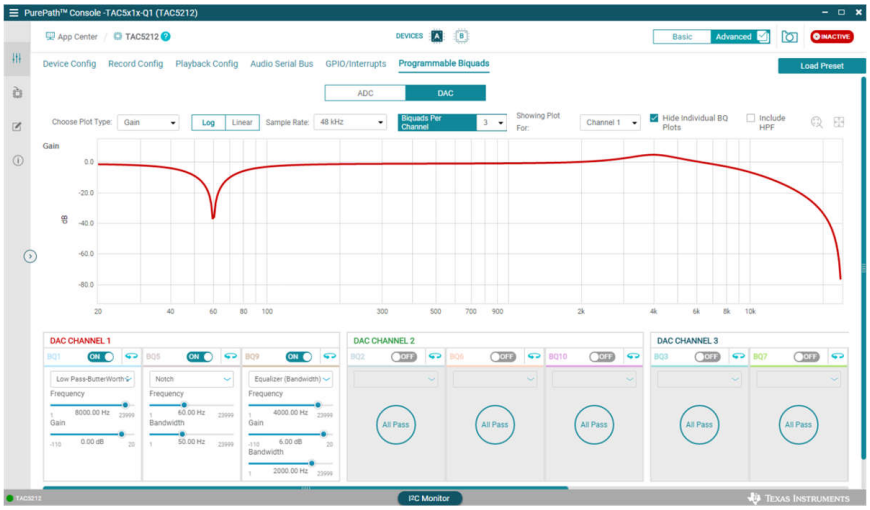

Figure 3-5. Expected DAC Biquad Filter Response Using the Script

4 Typical Audio Applications of Biquad Filters

In audio systems, biquad filters offer flexible frequency response filters for the following applications:

- Parametric equalizers
- Crossover networks
- Voice boost
- Bass boost
- Removing 50Hz–60Hz hum with notch filers

4.1 Parametric Equalizers

Cascading several parametric equalizers provide frequency shaping control of the input signal with three control settings: gain, center frequency, and bandwidth or Q-factor. Parametric equalizers control the tone and sound to flatten or match different input sources during mixing or provide particular effect to the input signal. Equalization usually compensates for the physical response of microphones or speakers, balances the tone of several instruments, or changes the timbre of an instrument since these filers provide very selective frequency adjustment during mixing or a specific range effect during recording. For example, small ear-bud headphones might not be able to reproduce low-frequency audio components in a similar fashion as the over-the-head type headphones or woofer speakers.

4.2 Crossover Networks

Crossover networks separate or join together several specific frequency bands. Crossover networks are typically used in speaker systems to separate the low-, mid-, and high-range frequencies to respective drive woofers, midrange, or tweeter drivers. These filters protect the drivers from wasteful, noise inducing, or harmful frequencies that the driver is not designed to handle. For example, there is no need to send high frequency to a woofer. The woofer is not able to reproduce high frequencies and just adds distortion. A tweeter can be damaged by strong low frequencies, thus the recommendation is to filter these before sending the signal to these drivers. Linkwitz Riley implementations are tailored to produce an overall gain of 0dB at the crossover frequency when the low-pass and high-pass filters combine together so the overall musical tone is not changed during reproduction.

4.3 Voice Boost

Human speech has a usable frequency range of 200Hz–8 kHz. Male speech bandwidth is roughly 200Hz–6 kHz while female speech bandwidth is roughly 400Hz–8kHz. To improve speech intelligibility, a bandpass filters or parametric equalizer boosts the voice band frequencies while suppressing other frequencies to lower background noise or other musical instruments.

4.4 Bass Boost

Simple Bass shelf filters provide a bass boost. These are typically used to compensate for speakers that have difficulty reproducing low frequencies. For example, small speakers can require a bass boost to improve low-frequency reproduction.

4.5 Removing 50Hz–60Hz Hum With Notch Filters

Notch filters cut a specific single frequency. These filters are highly efficient for removing 50Hz or 60Hz power line hum, transformer hum, room resonance, acoustic feedback, and any undesired specific frequency component introduced by the room acoustics or recording equipment.

5 Summary

The operation of the Programmable Biquad Filters was described in this application note, along with examples to demonstrate how to configure the same using PurePath™ Console.

6 References

- Texas Instruments, *TAC5212 High-performance stereo audio codec with 118dB dynamic range ADC and 119dB dynamic range DAC*, data sheet
- Texas Instruments, *TAC5112 Low-power stereo audio codec with 100dB dynamic range ADC and 106dB dynamic range DAC*,, data sheet
- Texas Instruments, *TAC5211 High-performance mono audio codec with 118dB dynamic range ADC and 119dB dynamic range DAC* , data sheet
- Texas Instruments, *TAC5111 Low-power mono audio codec with 100dB dynamic range ADC and 106dB dynamic range DAC*, data sheet
- Texas Instruments, *TAA5212 Low-power High-performance stereo audio ADC with 118dB dynamic range*, data sheet
- Texas Instruments, *TAD5212 High-performance stereo audio DAC with 119dB dynamic range* , data sheet
- Texas Instruments, *TAD5112 stereo audio DAC with 106dB dynamic range*, data sheet
- Texas Instruments, *TAC5412-Q1 Automotive Low Power Stereo Audio Codec with integrated programmable boost, micbias and diagnostics*, data sheet
- Texas Instruments, *TAC5312-Q1 Automotive Low Power Stereo Audio Codec with integrated programmable boost, micbias and diagnostics*, data sheet
- Texas Instruments, *TAC5411-Q1 Automotive Low Power Mono Audio Codec with integrated programmable boost, micbias and diagnostics*, data sheet
- Texas Instruments, *TAC5311-Q1 Automotive Low Power Mono Audio Codec with integrated programmable boost, micbias and diagnostics*, data sheet
- Texas Instruments, *TAA5412-Q1 Automotive, 2-Channel, 768kHz, Audio ADC With Integrated Microphone Bias and Input Fault Diagnostics*, data sheet
- Texas Instruments, *TLV320ADCx140/PCMx140-Q1 Programmable Biquad Filter Configuration and Applications*, application note

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