Application Note

MSPM0 C-Series MCU Hardware Development Guide

TEXAS INSTRUMENTS

MSP APP

ABSTRACT

The MSPM0 C-series microcontroller (MCU) portfolio offers a wide variety of low cost 32-bit MCUs with ultra-low-power and integrated analog and digital peripherals for sensing, measurement and control applications. This application note covers information needed for hardware development with MSPM0 C-series MCUs, including detailed hardware design information for power supplies, reset circuitry, clocks, debugger connections, key analog peripherals, communication interfaces, GPIOs, and board layout guidance.

Table of Contents

List of Figures

List of Tables

Trademarks

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1 MSPM0C Hardware Design Check List

Table 1-1 describes the main signal that needs to be checked during the MSPM0C hardware design process. The following sections provide more details.

Table 1-1. MSPM0C Hardware Design Check List

Pin (1)	Description	Requirements
VDD	Power supply positive pin	Place 10µF and 100nF capacitors between VDD and VSS, and keep those part close to VDD and VSS.
VSS	Power supply negative pin	
NRST	Reset pin	Connect an external 47kΩ pullup resistor with a 10nF pulldown capacitor.
VREF+(2)	Voltage reference power supply for external reference input	When using VREF+ and VREF- to bring in an external voltage reference for analog peripherals such as the ADC, a decoupling capacitor must be placed on VREF+ to VREF-/GND with a capacitance based on the external reference source. Keep open is OK if external voltage reference is not used.
VREF-(2)	Voltage reference ground supply for external reference input	
SWCLK	Serial wire clock from debug probe	Internal pulldown to VSS, does not need any external part.
SWDIO	Bidirectional (shared) serial wire data	Internal pullup to VDD, does not need any external part.
PA0, PA1	Open-drain I/O	Pull-up resistor required for output high
PA18(2)	Default BSL invoke pin	Keep pulled down to avoid entering BSL mode after reset. (BSL invoke pin can be remapped.)
PAx (exclude PA0, PA1)	General-purpose I/O	Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unused pins to output low or input with internal pullup or pulldown resistor.

(1) For any unused pin with a function that is shared with general-purpose I/O, follow the Section 8.5.
(2) Only MSPM0C1105 and MSPM0C1106 support external reference input, MSPM0C1103 and MSPM0C1104 just support internal reference. Only MSPM0C1105 and MSPM0C1106 have the default BSL invoke pin, MSPM0C1103 and MSPM0C1104 doesn't have the default BSL invoke pin.

TI recommends connecting a combination of a 10µF and a 0.1nF low-ESR ceramic decoupling capacitor to the VDD and VSS pins. Higher-value capacitors can be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the decoupled pins (within a few millimeters).

The NRST reset pin is required to connect an external 47kΩ pullup resistor with a 10nF pulldown capacitor.

For MSPM0C1105 and MSPM0C1106 which support external crystals, external bypass capacitors for the crystal oscillator pins are required when using external crystals.

For 5V-tolerant open drain (ODIO), a pullup resistor is required to output high, this is required for inter-integrated circuit (I2C) and universal asynchronous receiver/transmitter (UART) functions if the ODIO are used.

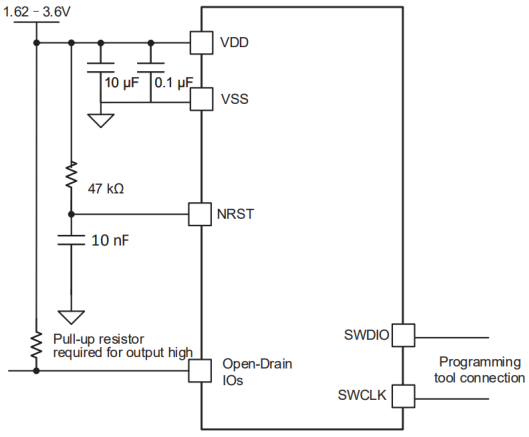

Figure 1-1. MSPM0C Typical Application Schematic

2 Power Supplies in MSPM0C Devices

Power is supplied to the device through the VDD and VSS connections. The device supports operation with a supply voltage of 1.62V to 3.6V and can start with a 1.62V supply. The power management unit (PMU) generates the regulated core supplies for the device and provides supervision of the external supply. The PMU also contains a bandgap voltage reference used by the PMU and other analog peripherals. VDD is used directly to provide the IO supply (VDDIO) and the analog supply (VDDA). VDDIO and VDDA are internally connected to VDD so that additional power supply pins are not required (see the device-specific data sheet for details).

2.1 Digital Power Supply

Core Regulator

There is an internal low-dropout linear voltage regulator to generate a 1.35V supply rail to power the device core. The core regulator is active in all power modes except for shutdown. In all other power modes (run, sleep, stop, and standby), the drive strength of the regulator is configured automatically to support the max load current of each mode. This reduces the quiescent current of the regulator when using low power modes, improving low power performance.

2.2 Analog Power Supply

Analog Mux VBOOST

In MSPM0C1105 and MSPM0C1106 which support COMP, the VBOOST circuit in the PMU generates an internal VBOOST supply that is used by the analog mux in COMP. The VBOOST circuit enables consistent analog mux performance across the external supply voltage (VDD) range.

Enabling and Disabling VBOOST

In MSPM0C1105 and MSPM0C1106, SYSCTL automatically manages the enable request for the VBOOST circuit based on the following parameters:

1. The COMP peripheral PWREN settings.
2. The MODE setting of any COMP which is enabled (FAST vs. ULP mode).
3. The ANACPUMPCFG control bits in the GENCLKCFG register in SYSCTL.

VBOOST is disabled by default following a SYSRST. Use the application software to enable the VBOOST circuit before using the COMP. When a COMP is enabled by application software, SYSCTL also enables the VBOOST circuit to support the analog peripheral.

The VBOOST circuit has a startup time requirement (12µs typical) to transition from a disabled state to an enabled state. In the event that the startup time of the COMP is less than the VBOOST startup time, the peripheral startup time is extended to account for the VBOOST startup time.

Bandgap Voltage Reference

The PMU provides a temperature and supply voltage stable bandgap voltage reference which is used by the device for internal functions, including:

- Driving the brownout reset circuit thresholds.
- Supporting the core regulator.
- Driving the on-chip VREF levels for on-chip analog peripherals.

The bandgap reference is enabled in RUN, SLEEP, and STOP modes. Bandgap voltage operates in a sampled mode in STANDBY to reduce power consumption, and is disabled in SHUTDOWN mode. SYSCTL manages the bandgap state automatically, no user configuration is required.

2.3 Built-in Power Supply and Voltage Reference

The VREF module for the MSPM0C family is a shared voltage reference module that can be leveraged by a variety on on-board analog peripherals.

The VREF module features include:

- 1.4V and 2.5V user-selectable internal references.
- Support for receiving external reference on the VREF+ and VREF- device pins.
- Sample and hold mode support VREF operation down to STANDBY operating mode.
- Internal reference supports for ADC, COMP.

When supplying the MCU with an external reference, TI recommends connecting a decoupling capacitor on the reference pins with a value based on the voltage source (see Figure 2-1).

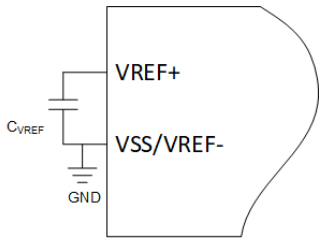

Figure 2-1. VREF Circuit

2.4 Recommended Decoupling Circuit for Power Supply

A combination of a 10µF plus a 100nF low-ESR ceramic decoupling capacitor is recommended to connect to the DVCC pin (see Figure 2-2). Higher-value capacitors can be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the decoupled pins (within a few millimeters).

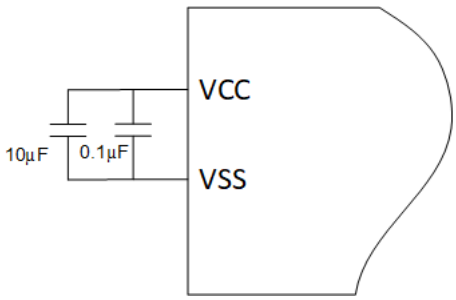

Figure 2-2. Power Supply Decoupling Circuit

3 Reset and Power Supply Supervisor

3.1 Digital Power Supply

The device has five reset levels:

- Power-on reset (POR)
- Brown-out reset (BOR)
- Boot reset (BOOTRST)
- System reset (SYSRST)
- CPU reset (CPURST)

The details of the relationships between reset levels is described in the MSPM0 C-Series 24MHz Microcontrollers Technical Reference Manual.

After a cold start, the NRST pin is configured in NRST mode. The NRST pin must be high for the device to boot successfully. There is no internal pullup resistor on NRST. External circuitry (either a pullup resistor to DVCC or a reset control circuit) must actively pull NRST high for the device to start. A capacitor and an open button are needed for manual reset (see Figure 3-1). After the device is started, a low pulse on NRST that is <1 second in duration triggers a BOOTRST. If a low pulse on NRST is held for >1 second, a POR is triggered.

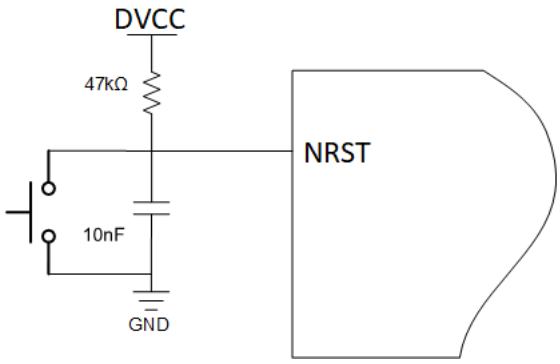

Figure 3-1. NRST Recommended Circuit

3.2 Power Supply Supervisor

3.2.1 Power-On Reset (POR) Monitor

The power-on reset (POR) monitor supervises the external supply (VDD) and asserts or de-asserts a POR violation to SYSCTL. During cold power-up, the device is held in a POR state until VDD passes the POR+. Once VDD has passed POR+, the POR state is released and the bandgap reference and BOR monitor circuit are started. If VDD drops below the POR- level, then a POR- violation is asserted and the device is again held in a POR reset state.

The POR monitor does not indicate that VDD has reached a level high enough to support correct operation of the device. Rather, this is the first step in the boot process and is used to determine if the supply voltage is sufficient to power up the bandgap reference and BOR circuit, which are then used to determine if the supply has reached a level sufficient to for the device to run correctly. The POR monitor is active in all power modes including SHUTDOWN, and cannot be disabled. The POR triggered waveform is shown in Section 3.2.3.

3.2.2 Brownout Reset (BOR) Monitor

The brown-out reset (BOR) monitor supervises the external supply (VDD) and asserts or deasserts a BOR violation to SYSCTL. The primary responsibility of the BOR circuit is to verify that the external supply is maintained high enough to enable correct operation of internal circuits, including the core regulator. The BOR threshold reference is derived from the internal bandgap circuit. The threshold is programmable and is always higher than the POR threshold. During cold start, after VDD passes the POR+ threshold the bandgap reference and BOR circuit are started. The device is then held in a BOR state until VDD passes the BOR0+ threshold. Once VDD passes BOR0+, the BOR monitor releases the device to continue the boot process, and the PMU is started. The BOR triggered waveform is shown in Section 3.2.3.

3.2.3 POR and BOR Behavior During Supply Changes

When the supply voltage (VDD) drops below POR-, the entire device state is cleared. Small variations in VDD which do not pass below the BOR0- threshold do not cause a BOR- violation, and the device can continue to run. Behavior for BORx thresholds other than BOR0 (for example, BOR1-BOR3) is the same as is shown for BOR0, except that the BOR circuit is configured to generate an interrupt rather than immediately triggering a BOR reset.

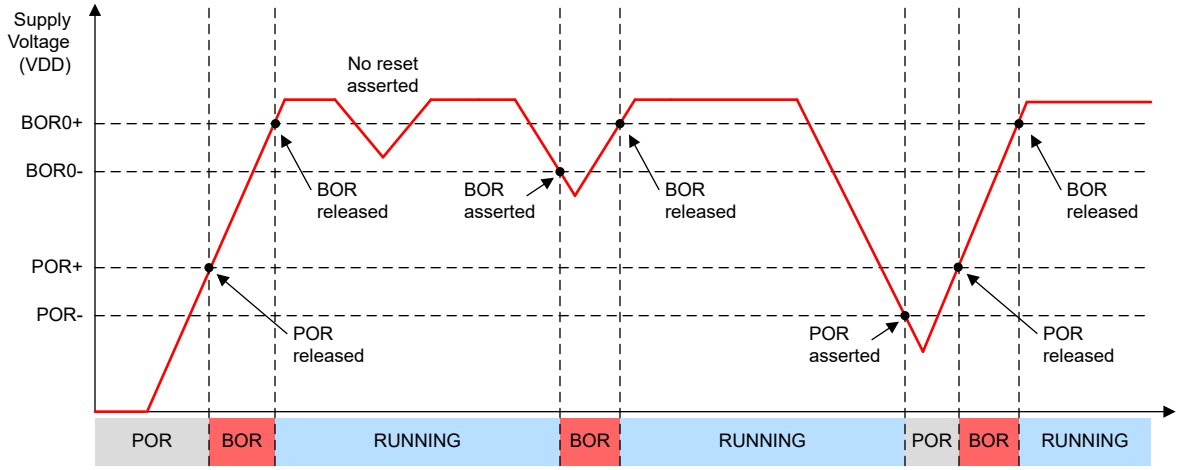

Figure 3-2. POR/BOR vs. Supply Voltage (VDD)

4 Clock System

The clock system of MSPM0C series contains the internal oscillators, the clock monitors, and the clock selection and control logic. A frequency clock counter is also provided for checking or calibrating the frequency of high-speed clocks against a reference period or pulse provided on an IO pin. This section describes the clock resources on different MSPM0C family devices and the interaction with external signals or devices. MSPM0C1105 and MSPM0C1106 support external oscillators but MSPM0C1103 and MSPM0C1104 do not.

4.1 Internal Oscillators

4.1.1 Internal Low-Frequency Oscillator (LFOSC)

LFOSC is an on-chip low-power oscillator that is factory trimmed to a frequency of 32.768kHz. LFOSC provides a low-frequency clock that can be used to help the system achieve low power. LFOSC can provide higher accuracy when used over a reduced temperature range. See the device-specific data sheet for details.

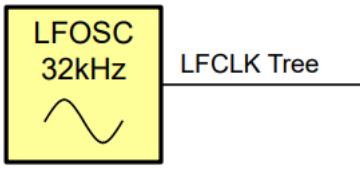

Figure 4-1. MSPM0C Series LFOSC

4.1.2 Internal System Oscillator (SYSOSC)

SYSOSC is an on-chip, accurate, and configurable oscillator with factory-trimmed frequencies. On MSPM0C1103 and MSPM0C1104, the base frequency is 24MHz and low frequency is 4MHz. On MSPM0C1105 and MSPM0C1106, the base frequency is 32MHz and low frequency is 4MHz. SYSOSC provides a high-frequency clock that lets the CPU run at high speed for executing code and processing performance.

SYSOSC Frequency Correction Loop

The overall SYSOSC application accuracy is determined by whether the internal ROSC resistor is used and the temperature. On MSPM0C1103 and MSPM0C1104, the SYSOSC circuit error in FCL mode is ±1.2% for 25°C, -1.6% to 1.4% for 0°C to 85°C, -2% to 1.4% for -40°C to 125°C. On MSPM0C1105 and MSPM0C1106, the SYSOSC circuit error in FCL mode is ±1.5% for -40°C to 125°C.

4.2 External Oscillators & External Clock Input

Both MSPM0C1103 and MSPM0C1104 and MSPM0C1105 and MSPM0C1106 support to use external digital clock input via LFCLK_IN and HFCLK_IN Pin. And MSPM0C1105 and MSPM0C1106 support external oscillators for applications that require even higher clock accuracy across devices and temperature. LFXT can replace LFOSC, and HFXT can replace SYSOSC.

4.2.1 Low-Frequency Crystal Oscillator (LFXT)

MSPM0C1105 and MSPM0C1106 support LFXT function. The LFXT is an ultra-low power crystal oscillator that supports driving a standard 32.768kHz watch crystal. To use the LFXT, populate a watch crystal between the LFXIN and LFXOUT pins. Place loading capacitors on both LFXIN and LFXOUT pins to circuit ground (VSS). Size the crystal load capacitors according to the specifications of the crystal being used. A variety of crystal types are supported through a programmable drive strength mechanism. For the layout advice, refer to Layout Guides.

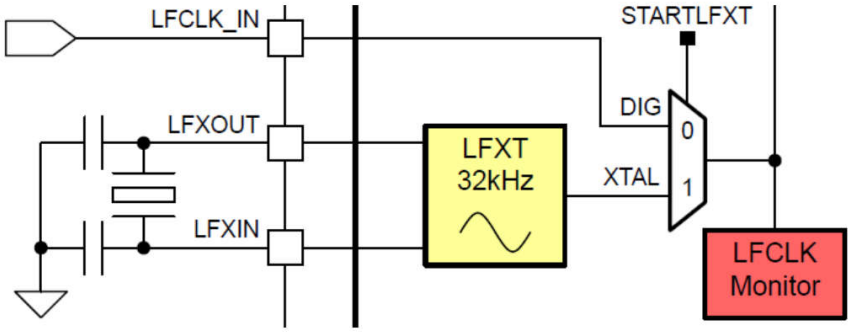

Figure 4-2. MSPM0C1105 and MSPM0C1106 LFXT Circuit

4.2.2 LFCLK_IN (Digital Clock)

A 32.76kHz typical frequency digital clock can be brought into the device to use as the LFCLK source. In MSPM0C1105 and MSPM0C1106. LFCLK_IN and LFXT are mutually exclusive and must not be enabled at the same time.

LFCLK_IN is compatible with digital square wave CMOS clock inputs and a typical duty cycle of 50% is recommended. Users can check for a valid clock signal on LFCLK_IN by enabling the LFCLK monitor. By default, the LFCLK monitor can check LFCLK_IN if the LFXT was not started.

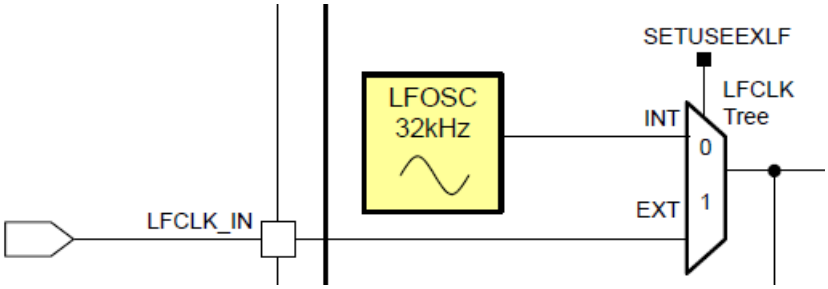

Figure 4-3. MSPM0C1103 and MSPM0C1104 External Clock Input LFCLK_IN

4.2.3 High-Frequency Crystal Oscillator (HFXT)

MSPM0C1105 and MSPM0C1106 support HFXT function. The high frequency crystal oscillator (HFXT) can be used with standard crystals and resonators in the 4 to 32MHz range to generate a stable high-speed reference clock for the system.

To use the HFXT, populate a crystal or resonator between the HFXIN and HFXOUT pins. Place loading capacitors on both pins to circuit ground (VSS). Size the crystal load capacitors according to the specifications of the crystal being used. A programmable HFXT startup time is provided with 64µs resolution. For layout advice, refer to Layout Guides.

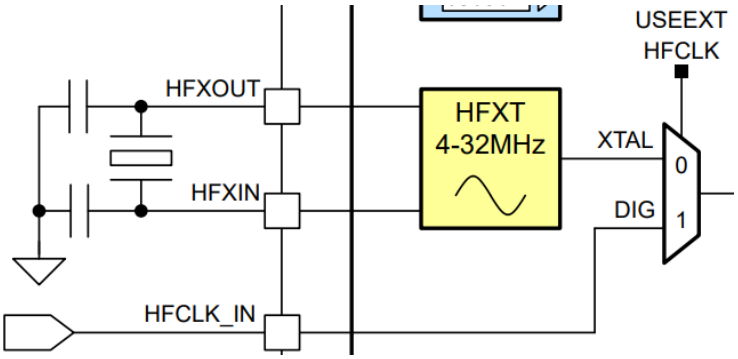

Figure 4-4. MSPM0C1105 and MSPM0C1106 HFXT Circuit

4.2.4 HFCLK_IN (Digital Clock)

On MSPM0C1103 and MSPM0C1104, a 4 to 24MHz typical frequency digital clock can be brought into the device to use as the HFCLK source. On MSPM0C1105 and MSPM0C1106, a 4 to 32MHz typical frequency digital clock can be brought into the device to use as the HFCLK source instead of HFXT. And HFCLK_IN and HFXT are mutually exclusive and must not be enabled at the same time.

HFCLK_IN is compatible with digital square wave CMOS clock inputs and a typical duty cycle of 50% is recommended.

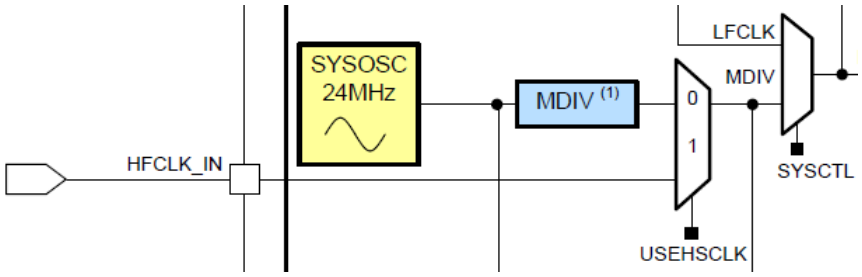

Figure 4-5. MSPM0C1103 and MSPM0C1104 External Clock Input HFCLK_IN

4.3 External Clock Output (CLK_OUT)

A clock output unit is provided for pushing out digital clocks from the device to external circuits or to the frequency clock counter. This feature is useful for clocking external circuitry such as an external ADC that does not have a clock source. The clock output unit has a flexible set of sources to select from and includes a programmable divider.

CLK_OUT on MSPM0C1103 or MSPM0C1104

The MSPM0C1103 and MSPM0C1104 have available clock sources for CLK_OUT:

- SYSOSC
- ULPCLK
- LFCLK

The selected clock source is divided by 2, 4, 6, 8, 10, 12, 14, or 16 before being output to the pin or to the frequency clock counter.

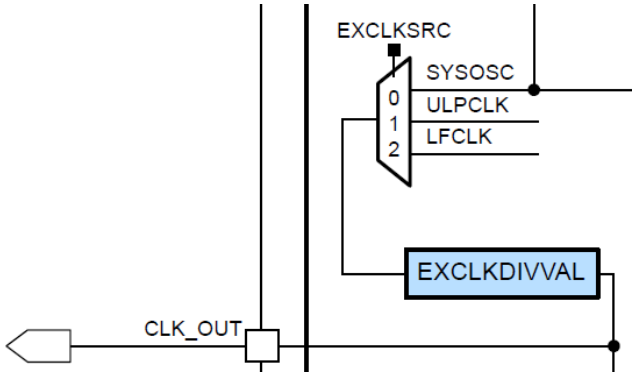

Figure 4-6. MSPM0C1103 MSPM0C1104 External Clock Output

CLK_OUT on MSPM0C1105 and MSPM0C1106

The MSPM0C1105 and MSPM0C1106 have available sources for CLK_OUT:

- SYSOSC
- ULPCLK
- LFCLK
- HFCLK
- MFPCLK

The selected clock source is divided by 2, 4, 6, 8, 10, 12, 14, or 16 before being output to the pin or to the frequency clock counter.

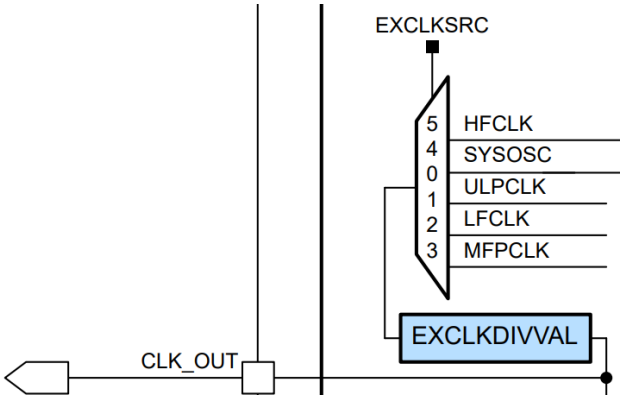

Figure 4-7. MSPM0C1105 and MSPM0C1106 External Clock Output

4.4 Frequency Clock Counter (FCC)

The frequency clock counter (FCC) enables flexible in-system testing and calibration of a variety of oscillators and clocks on the device. The FCC counts the number of clock periods seen on the selected source clock within a known fixed trigger period (derived from a secondary reference source) to provide an estimation of the frequency of the source clock.

FCC on MSPM0C1103 and MSPM0C1104

On MSPM0C1103 and MSPM0C1104, application software can use the FCC to measure the frequency of the following oscillators and clocks:

- MCLK
- SYSOSC
- CLK_OUT
- The external FCC input (FCC_IN)

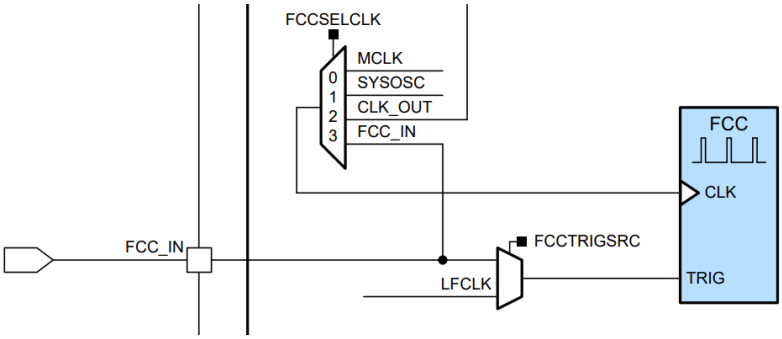

Figure 4-8. MSPM0C1103 and MSPM0C1104 Frequency Clock Counter Block Diagram

FCC on MSPM0C1105 and MSPM0C1106

On MSPM0C1105 and MSPM0C1106, application software can use the FCC to measure the frequency of the following oscillators and clocks:

- MCLK
- SYSOSC
- CLK_OUT
- HFCLK
- The external FCC input (FCC_IN)

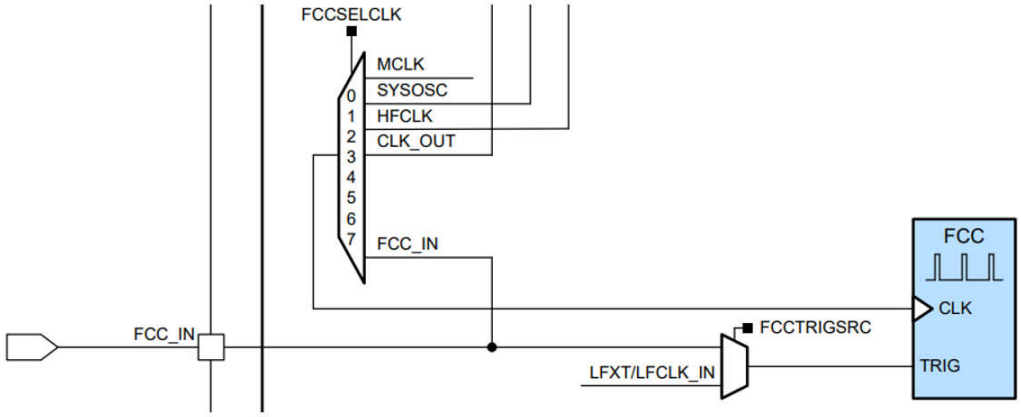

Figure 4-9. MSPM0C1105 and MSPM0C1106 Frequency Clock Counter Block Diagram

Note

While the external FCC input (FCC_IN function) can be used as either the FCC clock source or the FCC trigger input, FCC input cannot be used for both functions during the same FCC capture. FCC input must be configured as either the FCC clock source or the FCC trigger.

5 Debugger

The debug sub system (DEBUGSS) interfaces the serial wire debug (SWD) two-wire physical interface to multiple debug functions within the device. MSPM0C devices support debugging of processor execution, the device state, and the power state (using EnergyTrace technology).

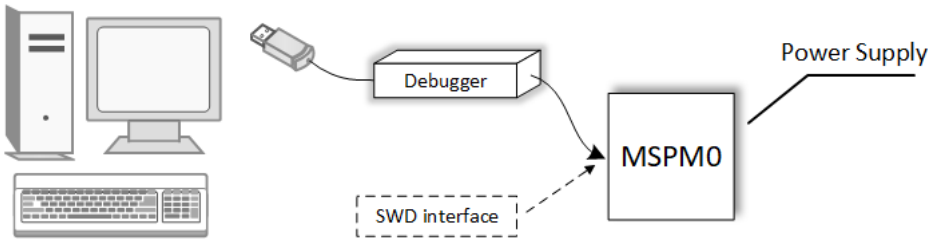

Figure 5-1. Host to Target Device Connection

5.1 Debug Port Pins and Pinout

The debug port contains SWCLK and SWDIO (see Table 5-1) which have internal pull-down and pull-up resistors (see Figure 5-2). The MSPM0L MCU family is offered in various packages with different numbers of available pins. Refer to the device-specific data sheet for details.

Table 5-1. MSPM0C Debug Ports

Device Signal	Direction	SWD Function
SWCLK	Input	Serial wire clock from debug probe
SWDIO	Input/Output	Bi-directional (shared) serial wire data

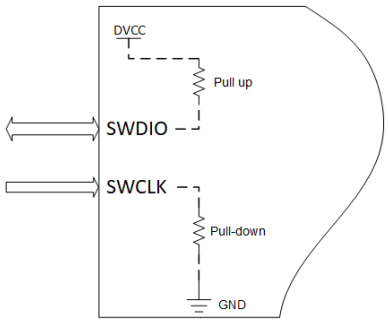

Figure 5-2. MSPM0C SWD Internal Pull

5.2 Debug Port Connection With Standard JTAG Connector

Figure 5-3 shows the connection between MSPM0C family MCU SWD debug port with the standard JTAG interface.

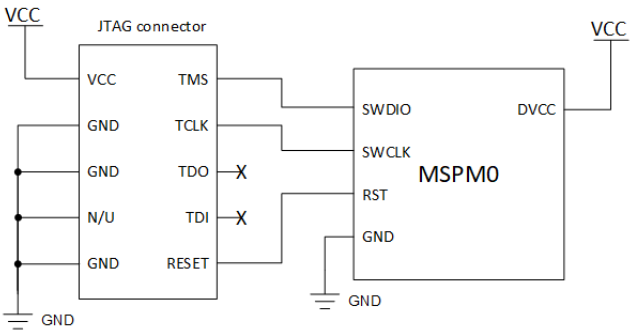

Figure 5-3. JTAG and MSPM0C Connection

For MSPM0C device, you can use XDS110 to implement debug/download function. Here list the contents of the XDS110 and provides instruction on installing the hardware.

5.2.1 Standard XDS110

You can purchase a standard XDS110 in ti.com. Figure 5-4 shows a high-level diagram of the major functional areas and interfaces of the XDS110 probe.

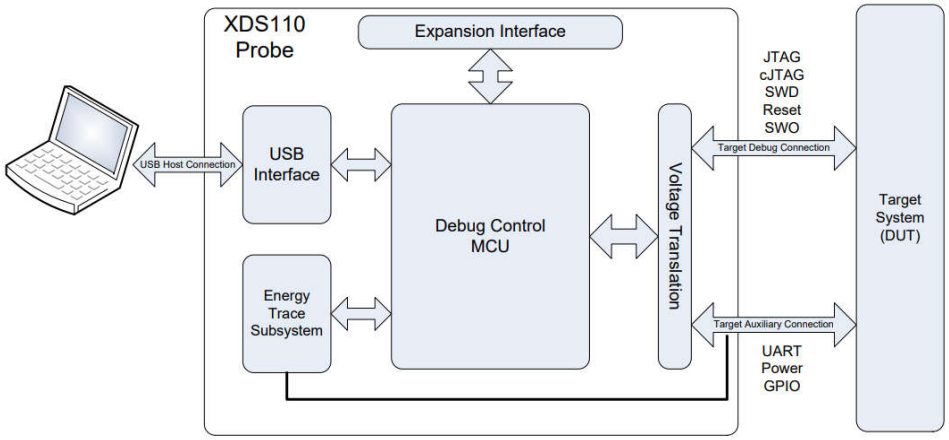

Figure 5-4. XDS110 Probe High-Level Block Diagram

More standard XDS110 information, see the *XDS110 Debug Probe User's Guide*.

5.2.2 Lite XDS110 (MSPM0 LaunchPad™ kit)

The MSPM0 LaunchPad kit include the XDS110 (Lite) circuit. You can also use this debugger to download your firmware into MSPM0 device. Figure 5-5shows the 2.54mm probe on LP-MSPM0C1104. And Figure 5-6 shows the 2.54mm probe and 10-pin probe on LP-MSPM0C1106.

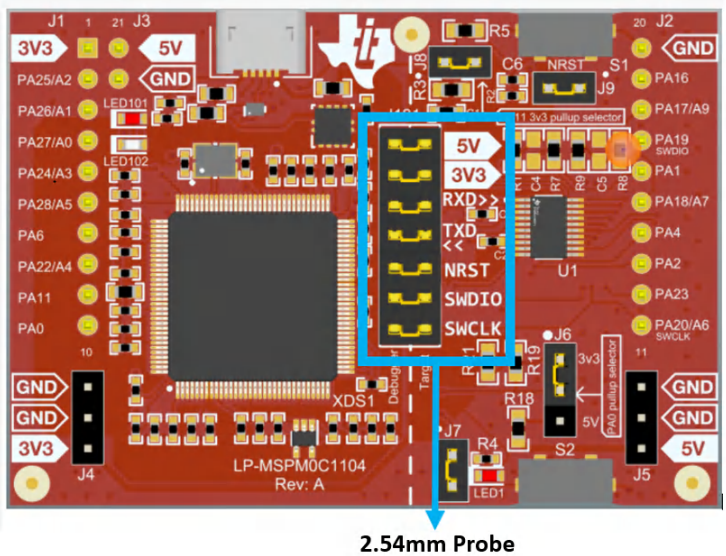

Figure 5-5. Probe on LP-MSPM0C1104

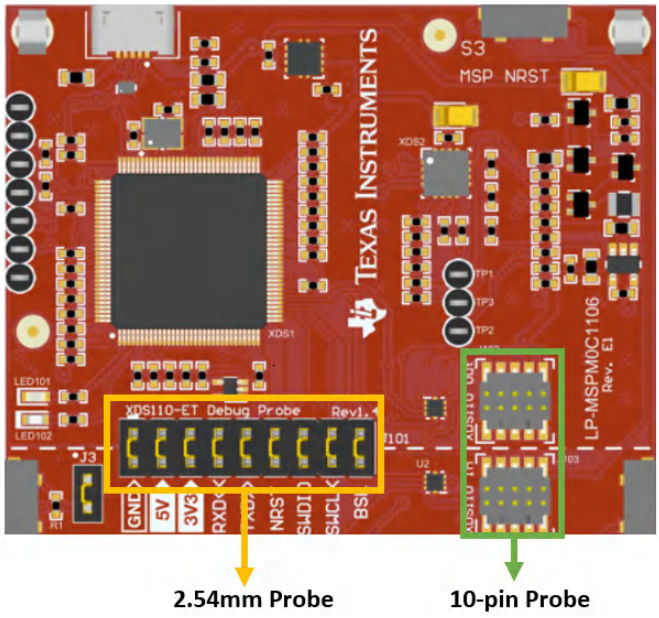

Figure 5-6. Probe on LP-MSPM0C1106

2.54mm probe: This port supports the SWD protocol and includes a 5V or 3.3V power supply. You can connect SWDIO SWCLK 3V3 GND to the board and download firmware into the MSPM0C device. The 2.54mm Probe on LP-MSPM0C1106 also supports EnergyTrace technology to measure power consumption precisely in real time. For more information for EnergyTrace technology, refer to the EnergyTrace Technology tool page.

10-pin probe: On LP-MSPM0C1106, this port supports the JTAG and SWD protocols and includes a 3.3V power supply. Users can use a 10-pin cable to connect the board and XDS110 and download firmware into an MSPM0C device.

Note

- Standard XDS110 support level shift for debug ports, XDS110 just support 3.3V probe level.
- TI does not recommend using the XDS110 to power other devices except the MSPM0C MCU. The XDS110 integrates an LDO with limited current drive capability.
- XDS110 2.54mm probe does not support JTAG protocol.
- XDS110 10-pin probe does not support EnergyTrace technology.

6 Key Analog Peripherals

The MSPM0C series MCU includes high-performance analog peripheral resources, which can provide basic analog signal conditioning functions inside the chip. To maximize the use of the MSPM0C analog peripheral performance, some considerations need to be made in the hardware design. This section discusses analog design considerations for many typical analog circuit configurations.

6.1 ADC Design Considerations

MSPM0C1103 and MSPM0C1104 have a 12bit, up to 1.5Msps, analog-to-digital converter (ADC), and MSPM0C1105 and MSPM0C1106 have a 12bit, up to 1.6Msps, ADC. The ADC supports fast 12, 10, and 8bit analog-to-digital conversions. The ADC implements a 12bit SAR core, sample and conversion mode control, and up to four independent conversion-and-control buffers.

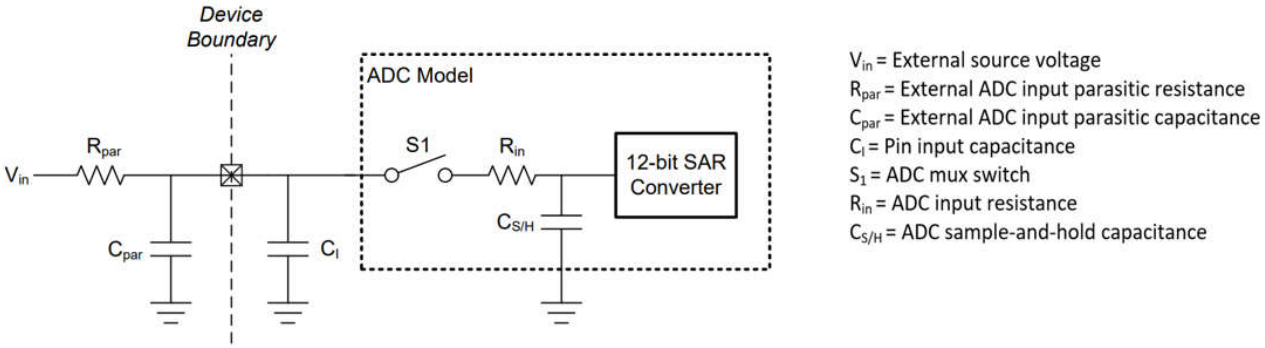

Figure 6-1. ADC Input Network

To achieve the desired conversion speed and keep high accuracy, set the proper sampling time in the hardware design. Sampling (sample-and-hold) time determines how long to sample a signal before digital conversion. During sample time, an internal switch lets the input capacitor charge. The required time to fully charge the capacitor is dependent on the external analog front-end (AFE) connected to the ADC input pin. Figure 6-1 shows a typical ADC model of an MSPM0C MCU. The R_{in} and $C_{S/H}$ values can be obtained from the device-specific data sheet. Understand the AFE drive capability and calculate the minimum sampling time required to sample the signal. The resistance of R_{par} and R_{in} affects t_{sample}. Equation 1 can be used to calculate a conservative value of the minimum sample time tsample for an n-bit and fixed settling error conversion:

$$t_{sample} \geq (\ln(2^n/\text{Settling error}) - \ln((C_{par} + C_I) / C_{S/H})) \times ((R_{par} + R_{in}) \times C_{S/H} + R_{par} \times (C_{par} + C_I)) \quad (1)$$

6.2 COMP and DAC Design Considerations

MSPM0C1105 and MSPM0C1106 support comparator module (COMP) which is an analog voltage comparator with general comparator functionality. Notice that MSPM0C1103 and MSPM0C1104 does not support COMP module. The comparator module includes internal and external input; users can use these structures flexibly to process analog signals. An internal temperature sensor is able to work as the COMP input directly. Figure 6-2 shows the comparator block diagram of MSPM0C1105 and MSPM0C1106.

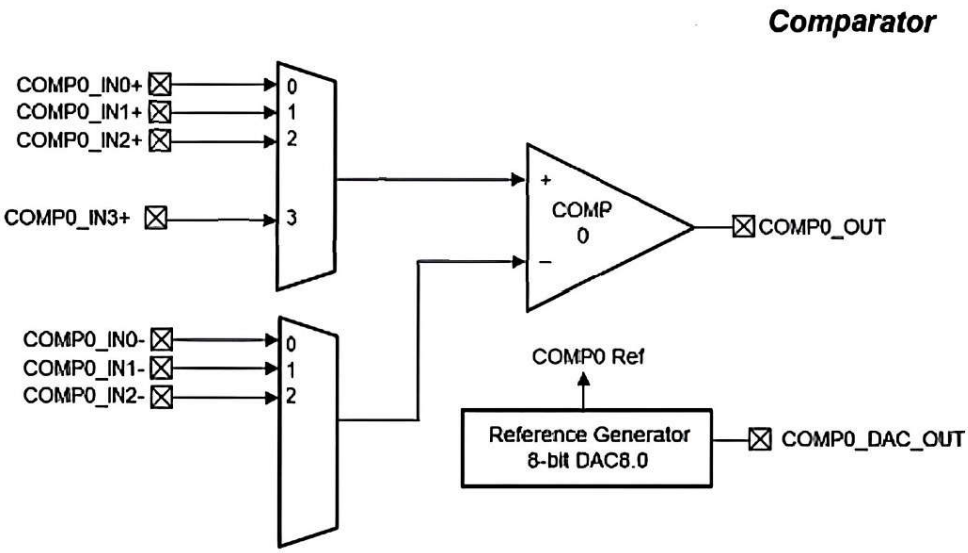

Figure 6-2. MSPM0C1105 and MSPM0C1106 Comparator Block Diagram

On MSPM0C1105 and MSPM0C1106, the 8-bit DAC can be used to generate the reference voltage for COMP, and also can be output to device pin (PA11). When want DAC output to device pin, some register setting is needed:

- Set ENABLE bit = 1h in COMP PWREN register to enable power for COMP
- Set DACOUTEN bit = 1h in COMP CTL1 register to enable DAC output to pin function
- Set ANACPUMPCFG bit = 2h in GENCLKCFG register to confirm the VBOOST is always enabled

Note that the 8-bit DAC output driving ability is weak, so DACOUT cannot be used to drive external resistor load.

7 Key Digital Peripherals

The MSPM0C series MCU includes digital peripheral resources including the Timer, UART, LIN, I2C and serial peripheral interface (SPI), among others, that provide rich communication capabilities. To maximize the use of the MSPM0C digital peripherals, some considerations need to be made in the hardware design. This section discusses design considerations for many typical digital peripheral configurations.

7.1 Timer Resources and Design Considerations

Timers are one of the most basic and important modules in any MCU, and this resource is used in all applications. Timers can be used to process tasks regularly, delay, output PWM waveforms to drive devices, detect the width and frequency of external pulses, simulate waveform outputs, and more.

The MSPM0C series MCU includes general-purpose timer (TIMG) and advanced control timers (TIMA). That can be used for a variety of functions, including measuring the input signal edge and period (capture mode) or generating output waveforms (compare mode output) like PWM signals. A summary of the different features and configurations of each timer is shown in the Table 7-1.

Table 7-1. TIMx Instance Configuration

Instance	Power Domain	Counter Resolution	Prescaler	Repeat Counter	CCP Channels	Phase Load	Shadow Load	Pipelined CC	Dead band	Fault Handler	QEI
TIMG0	PD0	16-bit	8-bit	-	2	-	-	-	-	-	-
TIMG1	PD0	16-bit	8-bit	-	2	-	-	-	-	-	-
TIMG2	PD0	16-bit	8-bit	-	2	-	-	-	-	-	-
TIMG3	PD0	16-bit	8-bit	-	2	-	-	-	-	-	-
TIMG4	PD0	16-bit	8-bit	-	2	-	Yes	Yes	-	-	-
TIMG5	PD0	16-bit	8-bit	-	2	-	Yes	Yes	-	-	-
TIMG6	PD1	16-bit	8-bit	-	2	-	Yes	Yes	-	-	-
TIMG7	PD1	16-bit	8-bit	-	2	-	Yes	Yes	-	-	-
TIMG8	PD0	16-bit	8-bit	-	2	-	-	-	-	-	Yes
TIMG9	PD0	16-bit	8-bit	-	2	-	-	-	-	-	Yes
TIMG10	PD1	16-bit	8-bit	-	2	-	-	-	-	-	Yes
TIMG11	PD1	16-bit	8-bit	-	2	-	-	-	-	-	Yes
TIMG12	PD1	32-bit	-	-	2	-	-	Yes	-	-	-
TIMG13	PD0	32-bit	-	-	2	-	-	Yes	-	-	-
TIMG14	PD1	16-bit	8-bit	-	4	-	-	-	-	-	-
TIMA0	PD1	16-bit	8-bit	Yes	4/2	Yes	Yes	Yes	Yes	Yes	-
TIMA1	PD1	16-bit	8-bit	Yes	2/2	Yes	Yes	Yes	Yes	Yes	-

- Refer to the device-specific data sheet to check which TIMG instances and TIMA instances are available on the device
- Check what features are available for each TIMG instance and each TIMA instance in the device-specific technical reference manual

7.2 UART and LIN Resources and Design Considerations

The MSPM0C series MCU includes Universal Asynchronous Receiver-Transmitter (UART). MSPM0C1103 and MSPM0C1104 only support UART0, and MSPM0C1105 and MSPM0C1106 support UART0, UART1, UART2. As seen in Table 7-2, UART0 supports LIN, DALI, IrDA, ISO7816 Manchester Coding function.

Table 7-2. UART Features

UART Features	UART0 (Extend)	UART1, UART2 (Main)
Active in Stop and Standby Mode	Yes	Yes
Separate transmit and receive FIFOs	Yes	Yes
Support hardware flow control	Yes	Yes
Support 9-bit configuration	Yes	Yes
Support LIN mode	Yes	-
Support DALI	Yes	-
Support IrDA	Yes	-
Support ISO7816 Smart Card	Yes	-
Support Manchester coding	Yes	-

Table 7-3. MSPM0C UART Specifications

PARAMETERS		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{UART}	UART input clock frequency	MSPM0C1103 and MSPM0C1104				24	MHz
		MSPM0C1105 and MSPM0C1106				32	
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)	MSPM0C1103 and MSPM0C1104				3	MHz
		MSPM0C1105 and MSPM0C1106				4	
t_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0	MSPM0C1103 and MSPM0C1104		11	35	ns
			MSPM0C1105 and MSPM0C1106		6		
		AGFSELx = 1			14	35	ns
		AGFSELx = 2			22	60	ns
		AGFSELx = 3			35	90	ns

The MSPM0C1103 and MSPM0C1104 UART module can support up to 3MHz baud rate. The MSPM0C1105 and MSPM0C1106 UART module can support up to 4MHz baud rate. These baud rates can support almost all UART applications.

Local Interconnect Network (LIN) is a commonly used low-speed network interface that consists of a commander node communicating with multiple remote responder nodes. Only a single wire is required for communication and is commonly included in the vehicle wiring harness.

The TLIN1021A-Q1 transmitter supports data rates up to 20kbps. The transceiver controls the state of the LIN bus through the TXD pin and reports the state of the bus on the open-drain RXD output pin. The device has a current-limited wave-shaping driver to reduce electromagnetic emissions (EME).

The TLIN1021A-Q1 is designed to support 12V applications with a wide input voltage operating range. The device supports low-power sleep mode, as well as wake-up from low-power mode by wake over LIN, the WAKE pin, or the EN pin. The device allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that can be present on a node through the TLIN1021A-Q1 INH output pin. Figure 7-1 shows a typical interface implemented using the TI TLIN1021A LIN transceiver.

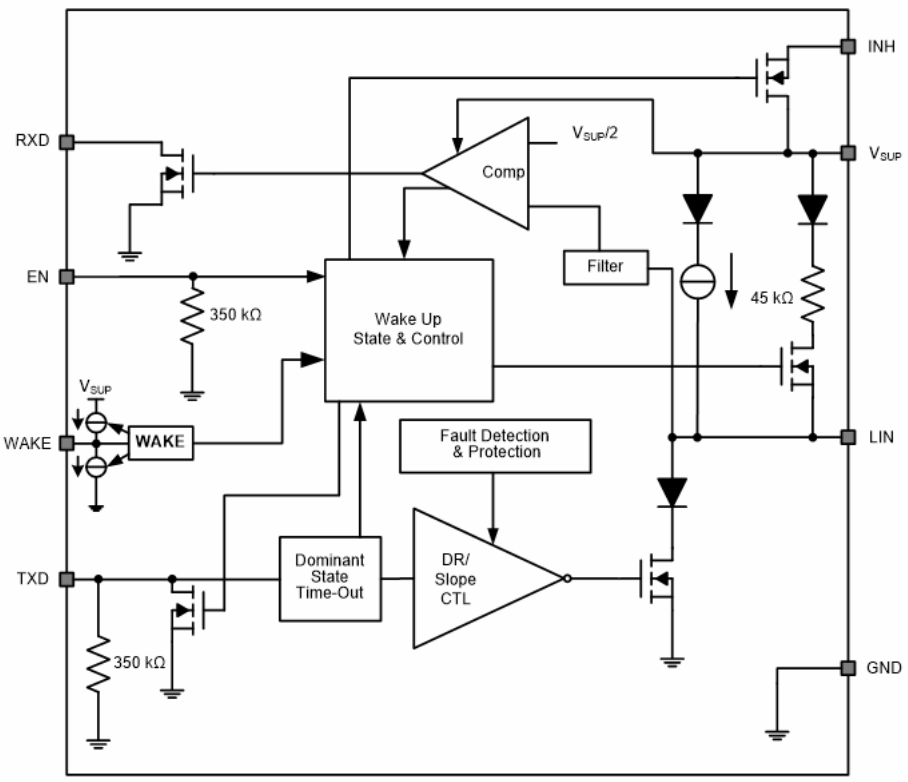

Figure 7-1. Typical LIN TLIN1021A Transceiver

Only a single wire is required for communication and is commonly included in the vehicle wiring harness. Figure 7-2 and Figure 7-3 shows a typical interface implemented using the TI TLIN1021A LIN transceiver. For more details, see the device-specific TLIN1021 data sheet.

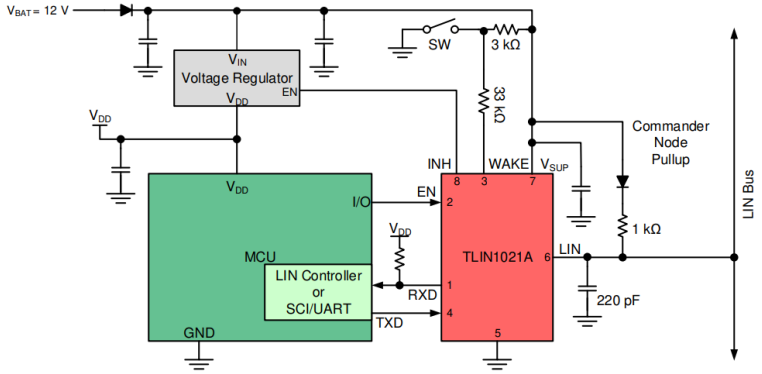

Figure 7-2. Typical LIN Application(Commander) with MSPM0C

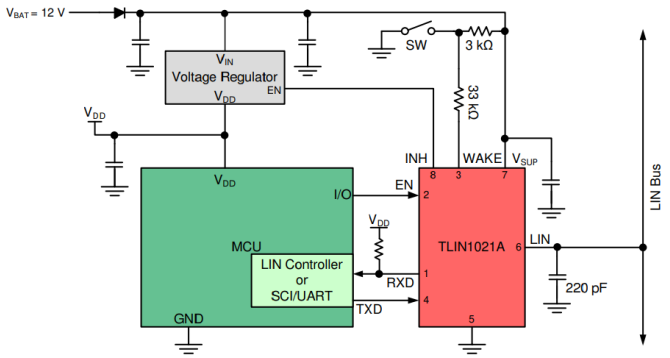

Figure 7-3. Typical LIN Application (Responder) with MSPM0C

7.3 I2C and SPI Design Considerations

SPI and I2C protocols are widely used in communication between devices or boards, such as data exchange between an MCU and a sensor. MSPM0C1103 and MSPM0C1104 include up to 12MHz high-speed SPI, and MSPM0C1105 and MSPM0C1106 include up to 16MHz high-speed SPI. The SPI supports 3wire, 4wire, chip select, and command mode. To design a system based on the requirements, see Figure 7-4.

Some SPI peripheral devices need PICO (Peripherals Input Controller Output) keep high logic. In this case, add a pullup resistor to PICO pin.

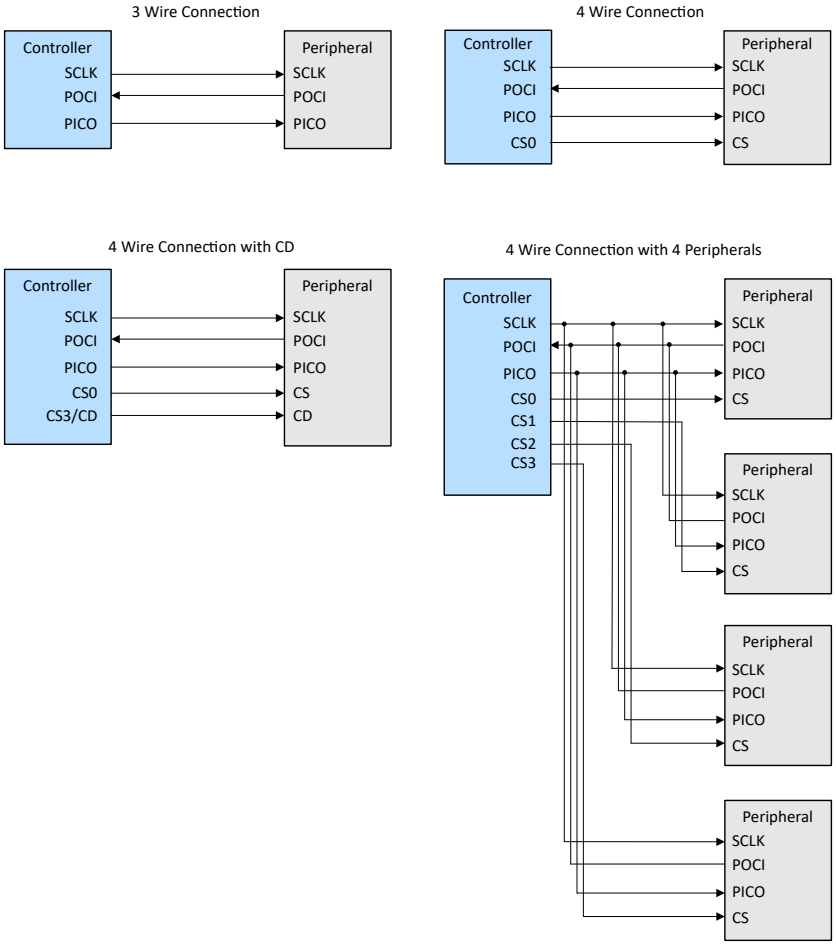

Figure 7-4. External Connections for Different SPI Configurations

For I2C bus, the MSPM0C device supports standard, fast and fast plus mode, as shown in Table 7-4.

External pullup resistors are required when using I2C bus. The value of these resistors depends on the I2C speed; TI recommends 2.2k to support Fast mode+. For systems concerned with power consumption, large resistor values can be used. ODIO (see Section 8) can be used to implement communication with a 5V device.

Table 7-4. MSPM0C I2C Characteristics

PARAMETERS		TEST CONDITIONS		Standard Mode		Fast Mode		Fast Mode Plus		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{I2C}	I2C input clock frequency	I2C in Power Domain0	MSPM0C1103 and MSPM0C1104		24		24		24	MHz
			MSPM0C1105 and MSPM0C1106	2	32	8	32	20	32	
f_{SCL}	SCL clock frequency				100K		400K		1M	Hz
$t_{HD,STA}$	Hold time (repeated) START			4		0.6		0.26		us
t_{LOW}	Low period of the SCL clock			4.7		1.3		0.5		us
t_{HIGH}	High period of the SCL clock			4		0.6		0.26		us
$t_{SU,STA}$	Setup time for a repeated START			4.7		0.6		0.26		us
$t_{HD,DAT}$	Data hold time			0		0		0		us
$t_{SU,DAT}$	Data setup time			250		100		50		us
$t_{SU,STO}$	Setup time for STOP			4		0.6		0.26		us
t_{BUF}	Bus free time between a STOP and START condition			4.7		1.3		0.5		us
$t_{VD;DAT}$	Data valid time				3.45		0.9		0.45	us
$t_{VD;ACK}$	Data valid acknowledge time				3.45		0.9		0.45	us

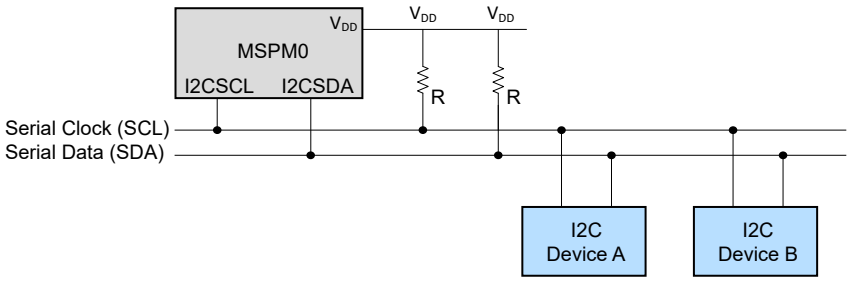

Figure 7-5. Typical I2C Bus Connection

8 GPIOs

MSPM0C series MCUs include Standard-Drive I/O (SDIO) and 5V tolerant Open-Drain I/O (ODIO). Users can flexibly choose the appropriate I/O type based on actual requirements. And the following characteristics need to be considered in hardware design.

8.1 GPIO Output Switching Speed and Load Capacitance

When using the GPIO as I/O, design considerations must be made to verify the correct operation. As load capacitance becomes larger, the rise/fall time of the I/O pin increases. This capacitance includes pin parasitic capacitance (Ci = 5pF (Typical)) and the effects of the board traces. I/O characteristics are available in the device-specific data sheet. Table 8-1 list the I/O output frequency characteristics of MSPM0C1103 and MSPM0C1104. And list the I/O output frequency characteristics of the MSPM0C1105 and MSPM0C1106.

Table 8-1. MSPM0C1103 and MSPM0C1104 GPIO Switching Characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Port output frequency	SDIO	VDD ≥1.71V, C_L = 20pF			24	MHz
		ODIO	VDD ≥1.71V, FM+, C_L= 20pF to 100pF			1	
t_r,t_f	Output rise or fall time	All output ports except ODIO	VDD ≥ 1.71V			0.3* f_{max}	s
t_f	Output fall time	ODIO	VDD ≥ 1.71V, FM+, C_L= 20 pF to 100pF	20 × VDD / 5.5		120	ns

Table 8-2. MSPM0C1105 and MSPM0C1106 GPIO Switching Characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Port output frequency	SDIO	VDD ≥ 1.71V, CL= 20pF			16	MHz
			VDD ≥ 2.7V, CL= 20pF			32	
		ODIO	VDD ≥ 1.71V, FM+ , CL= 20pF - 100pF			1	
t_r,t_f	Output rise/fall time	SDIO	VDD ≥ 1.71V, CL= 20pF			3.5	ns
		SDIO	VDD ≥ 2.7V, CL= 20pF			6.6	ns
t_f	Output fall time	ODIO	VDD ≥ 1.71V, FM+ , CL= 20pF-100pF			120	ns

Note

- The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.
- The output rise time of open-drain I/Os is determined by the pullup resistance and load capacitance.

8.2 GPIO Current Sink and Source

Table 8-3. MSPM0C GPIO Absolute Maximum Ratings

				MIN	NOM	MAX	UNIT
VDD	Supply voltage			1.62		3.6	V
C_{VDD}	Capacitor placed between VDD and VSS				10		µF
I_{VDD}	Current of VDD pin	MSPM0C1103 and MSPM0C1104	-40°C ≤ Ta ≤ 85°C			80	mA
		MSPM0C1105 and MSPM0C1106	-40°C ≤ Tj ≤ 130°C			100	
			-40°C ≤ Tj ≤ 85°C			80	
I_{IO}	Current for SDIO pin					6	mA
	Current for ODIO pin					20	mA
T_A	Ambient temperature, S version			–40		125	°C
T_J	Max junction temperature, S version					130	°C

Table 8-3. MSPM0C GPIO Absolute Maximum Ratings (continued)

				MIN	NOM	MAX	UNIT
f_{MCLK}	MCLK, CPUCLK, ULPCLK frequency	MSPM0C1103 and MSPM0C1104	with 0 flash wait states			24	MHz
		MSPM0C1105 and MSPM0C1106	with 0 flash wait states			24	
			with 1 flash wait state			32	

Note

- The total current of I/O must be less than the maximum value of I_{VDD}.
- ODIO are patched in a fixed pin; refer to the device data sheet.

SDIO can sink or source a maximum current of 6 mA (typical), which is sufficient to drive a typical LED. The total combined current must be less than I_{VDD}.

8.3 Open-Drain GPIOs Enable 5V Communication Without a Level Shifter

ODIO are tolerant to 5V input. Because ODIO are open drain, an external pullup resistor is needed for the pin to be able to output high. This I/O can used for UART or I2C interface with different voltage levels. To limit the current, a series resistor must be placed between the pin and the pullup resistor, and the RSERIES must be no less than 250Ω. As shown in Figure 8-1, TI recommends 270Ω. The value of the pullup resistor depends on the output frequency (see Section 7.3).

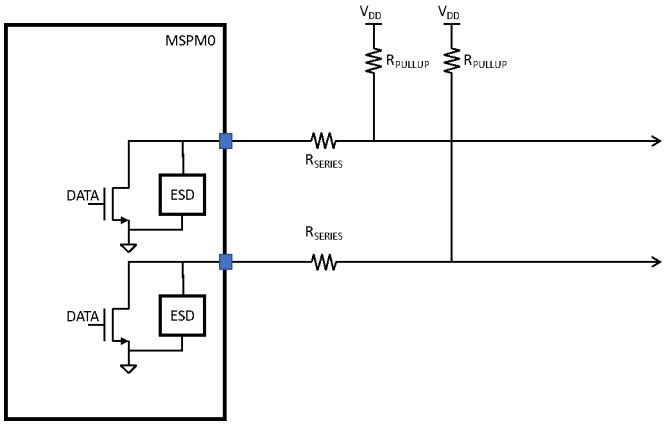

Figure 8-1. Suggested ODIO Circuit

8.4 Communicate With 1.8V Devices Without a Level Shifter

The MSPM0C series devices use a 3.3V logic level (excluding ODIO). To communicate with 1.8V devices without an external level shifter device, Figure 8-2 shows a suggested circuit for interfacing with a 1.8V device.

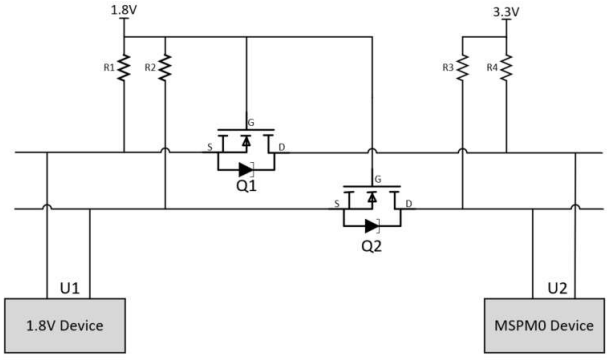

Figure 8-2. Suggested Communication Circuit With 1.8V Device

Two MOSFETs are used in this circuit; check the VGS to make sure the MOSFET is able to fully turn on with a low RDS(on). For a 1.8V device, use less than 1.8V VGS on the MOSFET. However, do not use a very low VGS MOSFET, as this causes the MOSFET to turn on at a very small voltage (MCU logic judges as 0), resulting in communication logic error.

U1 Output and U2 Input

1. U1 output: *1.8V high*, Q1 VGS around 0, thus Q1 turn off, U2 reads *3.3V high* with R4.
2. U1 output: *low*, Q1 VGS near 1.8V, thus Q1 turns on, U2 reads *low*.

U1 Input and U2 Output

1. U2 output: *3.3V high*, U1 keeps 1.8V with R1, and Q1 turns off, thus U1 reads *1.8V high*.
2. U2 output: *low*, U1 keeps 1.8V with R1 at first, but the diode in the MOSFET pulls down U1 to 0.7V (diode voltage drops), and then causes VGS to be greater than the turn-on voltage, Q1 turns on, and U1 reads *low*.

8.5 Unused Pins Connection

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources.

To increase EMC performance, do not leave unused clocks, counters, and I/Os free or floating; for example, set I/Os to 0 or 1 (pullup or pulldown on unused I/O pins) and disable unused features.

Table 8-4. Connection of Unused Pins

Pin	Potential	Comment
PAx	Open	Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unused pins to output low or input with internal pullup or pulldown resistor.
NRST	VDD	NRST is an active-low reset signal; this must be pulled high to VCC or the device does not start.

Note

- To reduce leakage, TI recommends to configure the I/O as an analog input or to push-pull and set to *0*.
- The BSL invoke pin must be pulled down to avoid entering BSL mode after reset.

9 Layout Guides

9.1 Power Supply Layout

Figure 9-1 shows the typical parts placement and routing for the power supply layout; you must modify this appropriately for your MSPM0C part. You can optionally connect a filter inductor in series with the VCC and MCU VDD pins. This inductor is used to filter the switching noise frequency of DCDC. For the value, refer to the data sheet of DCDC vendor. C1, C2, and C3 values and layout in the MSPM0C device data sheets.

Note

- Keep the smallest capacitance, closest to the MCU VDD pin (C1 < C2 < C3).
- All the traces can be direct without any vias.

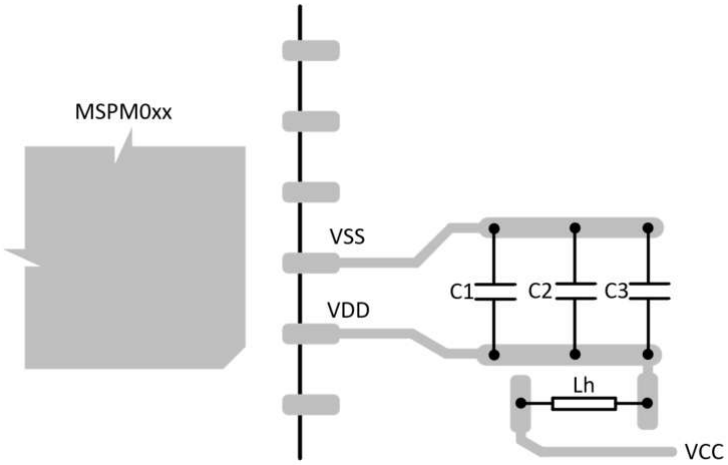

Figure 9-1. Suggested Power Supply Layout

9.2 Considerations for Ground Layout

System ground is the most critical area and foundation related to noise and EMI problems on the board. The most practical way to minimize these problems is to have a separate ground plane.

9.2.1 What is Ground Noise?

Each signal originating from a circuit (for example, driver) has a return current flow to the source by ground path. As the frequency increases, or even for simple but high-current switching like relays, there is a voltage drop due to line impedance generating interference in the grounding scheme. The return path is always by the least resistance. For DC signals, that can be the lowest resistive path. For high frequency signals, that can be the lowest impedance path. This explains how a ground plane simplifies the issue and is the key to making sure of signal integrity.

TI does not recommend that the digital return signals propagate inside the analog return (ground) area; therefore, split the ground plane to keep all the digital signal return loops within the ground area. This splitting must be done carefully. Many designs use a single (common) voltage regulator to generate a digital and analog supply of the same voltage level (for example, 3.3V). Isolate the analog rail and digital supply rails and the respective grounds from each other. Be careful while isolating ground, as both grounds have to be shorted somewhere. Figure 9-2 shows how possible return paths for digital signals are not allowed to form a loop passing through the analog ground. On each design, decide the common point considering the component placements and so forth. Do not add any inductors (ferrite bead) or resistors (not even zero Ω) in the series with any ground trace. The impedance increases due to associated inductance at a high frequency, causing a voltage differential. Do not route a signal referenced to digital ground over analog ground or the other direction.

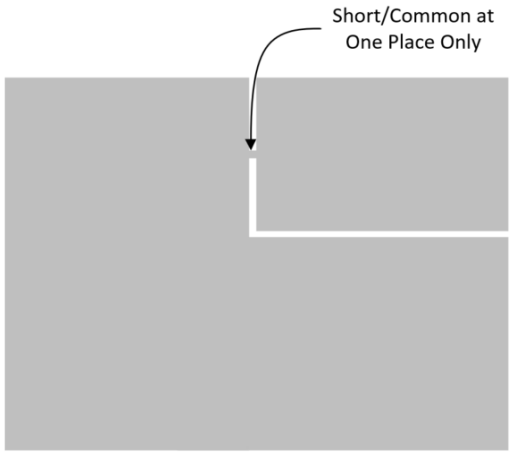

Figure 9-2. Digital and Analog Grounds and Common Area

9.3 Traces, Vias, and Other PCB Components

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner and the characteristic impedance changes. This impedance change causes reflections. Avoid right-angle bends in a trace and try to route them with at least two 45° corners. To minimize any impedance change, the best routing can be a round bend, as shown in Figure 9-3.

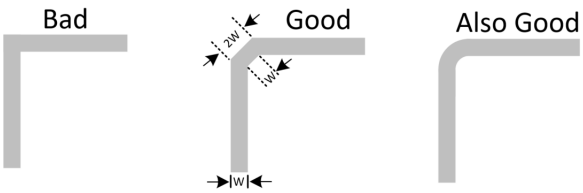

Figure 9-3. Poor and Correct Way of Bending Traces in Right Angle

To minimize crosstalk, not only between two signals on one layer but also between adjacent layers, route 90° to each other. More complex boards need to use vias while routing; however, care must be taken when using vias as this adda additional inductance and capacitance, and reflections occur due to the change in the characteristic impedance. Vias also increase the trace length. When using differential signals, use vias in both traces or compensate the delay in the other trace as well.

For signal traces, pay more attention to the impact of high-frequency pulse signals, especially on relatively small analog signals (like sensor signals). Too many crossovers can couple the electromagnetic noise of the high-frequency signal to the analog signal, which can result in a low signal-to-noise ratio of the signal and affect the signal quality. Therefore, avoid crossing when designing. But, if there is indeed an unavoidable intersection, then TI recommends to intersect vertically to minimize the interference of electromagnetic noise. Figure 9-4 shows how to reduce this noise.

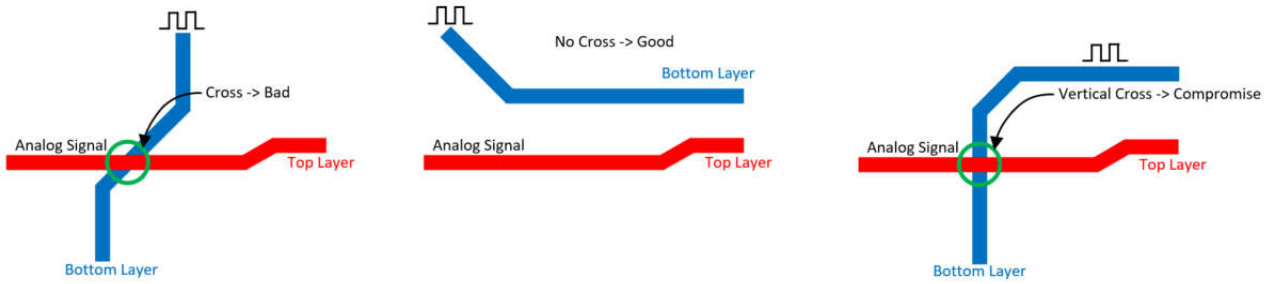

Figure 9-4. Poor and Correct Cross Traces for Analog and High-Frequency Signals

9.4 How to Select Board Layers and Recommended Stack-up

To reduce the reflections on high speed signals, match the impedance between the source, sink and transmission lines. The impedance of a signal trace depends on the geometry and the position with respect to any reference planes.

The trace width and spacing between differential pairs for a specific impedance requirement is dependent on the chosen PCB stack-up. As there are limitations in the minimum trace width and spacing which depend on the type of PCB technology and cost requirements, a PCB stack-up needs to be chosen which allows all the required impedances to be realized.

The minimum configuration that can be used is 2 stack-up. A 4- or 6-layer boards is required for very dense PCBs that have multiple high-speed signals.

The following stack-up (see Figure 9-5) is a 4-layer examples that can be used as a starting point for helping in a stack-up evaluation and selection. These stack-up configurations are using a GND plane adjacent to the power plane to increase the capacitance and reduce the gap between GND and power plane. High speed signals on the top layer can have a solid GND reference plane, which help to reduce EMC emissions, as going up in number of layers and having a GND reference for each PCB signal layer further improves the radiated EMC performance.

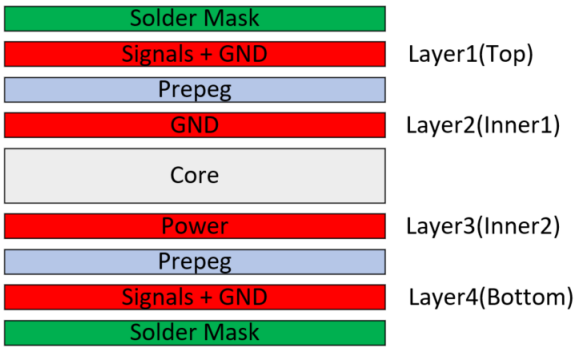

Figure 9-5. Four-Layer PCB Stack-up Example

If the system is not very complicated, then there is no high-speed signal or some sensitive analog signal, then the 2 stack-up structure is sufficient.

10 Bootloader

MSPM0C1103 and MSPM0C1104 do not have ROM BSL. Users need to use the secondary BSL and place the secondary BSL code at 0x0 address in flash. MSPM0C1105 and MSPM0C1106 do not have ROM BSL either, but MSPM0C1105 and MSPM0C1106 support BSL invoke pin setting and secondary BSL address (alternate BSL address) setting in NONMAIN. These configuration allows MSPM0C1105 and MSPM0C1106 check invoke pin in boot process and jump to secondary BSL address directly.

11 Summary

This application note provides comprehensive hardware design guidelines for Texas Instruments' MSPM0 C-series microcontrollers (MCU). The document details essential implementation aspects for developers working with cost-effective 32-bit MCUs, which are designed for low power applications. The application note includes practical instructions for designing and implementing key hardware components including:

- Power supply configurations
- Reset circuit design
- Clock system setup
- Debug interface connections
- Analog peripheral implementation
- Communication interface integration
- GPIO configuration
- PCB layout recommendations

The document serves as a reference manual for engineers developing hardware designs using MSPM0 C-series MCUs in sensing, measurement, and control applications.

12 References

- Texas Instruments, *MSPM0C1104 Mixed-Signal Microcontrollers*, data sheet
- Texas Instruments, MSPM0C1105 and MSPM0C1106 Mixed-Signal Microcontrollers, data sheet
- Texas Instruments, *MSPM0 C-series 24MHz Microcontrollers Technical Reference Manual*
- Texas Instruments, *MSPM0 L-Series MCUs Hardware Development Guide*, application note

13 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2025) to Revision B (July 2025)	Page
• Updated the entire document with new information of MSPM0C1105 and MSPM0C1106	1
• Updated information in Table 1-1	3
• Added *Low-Frequency Crystal Oscillator (LFXT)* section	8
• Added *High-Frequency Crystal Oscillator (HFXT)* section	9
• Added new reference to data sheet	29

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