

Subsystem Design

DMA Ping Pong With ADC



1 Description

The [DMA Ping Pong with ADC](#) example demonstrates how to use the DMA to transfer ADC data between two different buffers, also known as a DMA *Ping Pong*. A DMA Ping Pong is commonly used to transfer data to one buffer while the CPU is working with the other buffer. The blue path in [Figure 1-1](#) shows that the DMA transfers data to Buffer 1 and the CPU gets data from Buffer 2. When the paths switch, the DMA transfers data to Buffer 2 and the CPU gets data from Buffer 1. The benefit to this technique is faster total application runtime because the CPU is free to operate on a section of data at all times. In this example, the ADC is configured in single conversion mode and the DMA and CPU switches between buffers after each conversion.

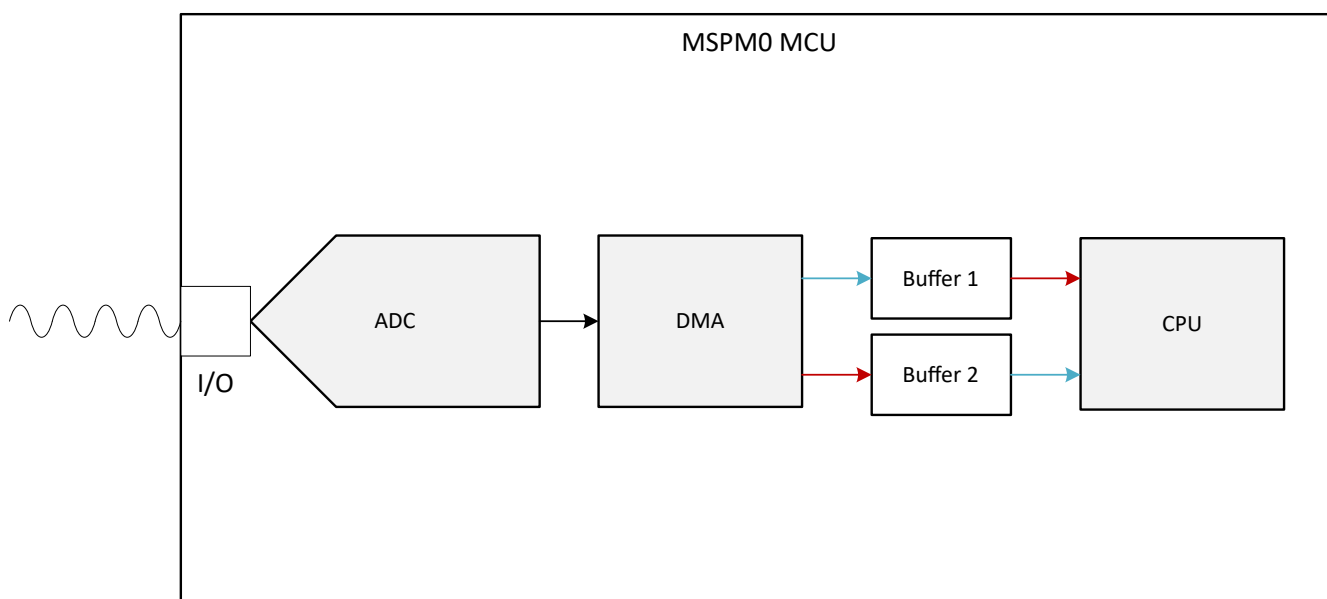


Figure 1-1. Subsystem Functional Block Diagram

2 Required Peripherals

This application requires the integrated ADC and DMA. The internal VREF is an additional option for the ADC reference, if a different reference value is required.

Table 2-1. Required Peripherals

Subblock Functionality	Peripheral Use	Notes
Analog Signal Capture	ADC	Called ADC12_0_INST in code
Moving memory	DMA	Full featured DMA channel is required to utilize the PREIRQ functionality. The example can be altered to work without the PREIRQ.

3 Design Steps

1. Determine the configuration for the ADC including reference source, reference value, resolution, and sampling rate based on the given analog input and design requirements.
2. Generate two array buffers to store the ADC data and set the buffer size and DMA transfer size the same so the DMA fills the whole buffer.
3. Configure the ADC in [SysConfig](#) based on the project requirements discovered in [Step 1](#).

4. Configure the DMA in [SysConfig](#) in the ADC section.
5. Write *Application Code* to dynamically change the destination address of the DMA to alternate between buffers. See [Figure 5-1](#) for an overview or view the code directly.

4 Design Considerations

1. **Maximum Sampling Speed:** The sampling speed of the ADC is based on input signal frequency, analog front end, filters, or any other design parameters that affect sampling.
2. **ADC Reference:** Choose the reference to align with the expected maximum input to utilize the full scale range of the ADC.
3. **Clock Settings:** The clock source determines the total time for the conversion. The clock divider in tandem with the SCOMP setting determines the total sampling time. SysConfig sets the appropriate SCOMP depending on the sampling time setting.

5 Software Flow Chart

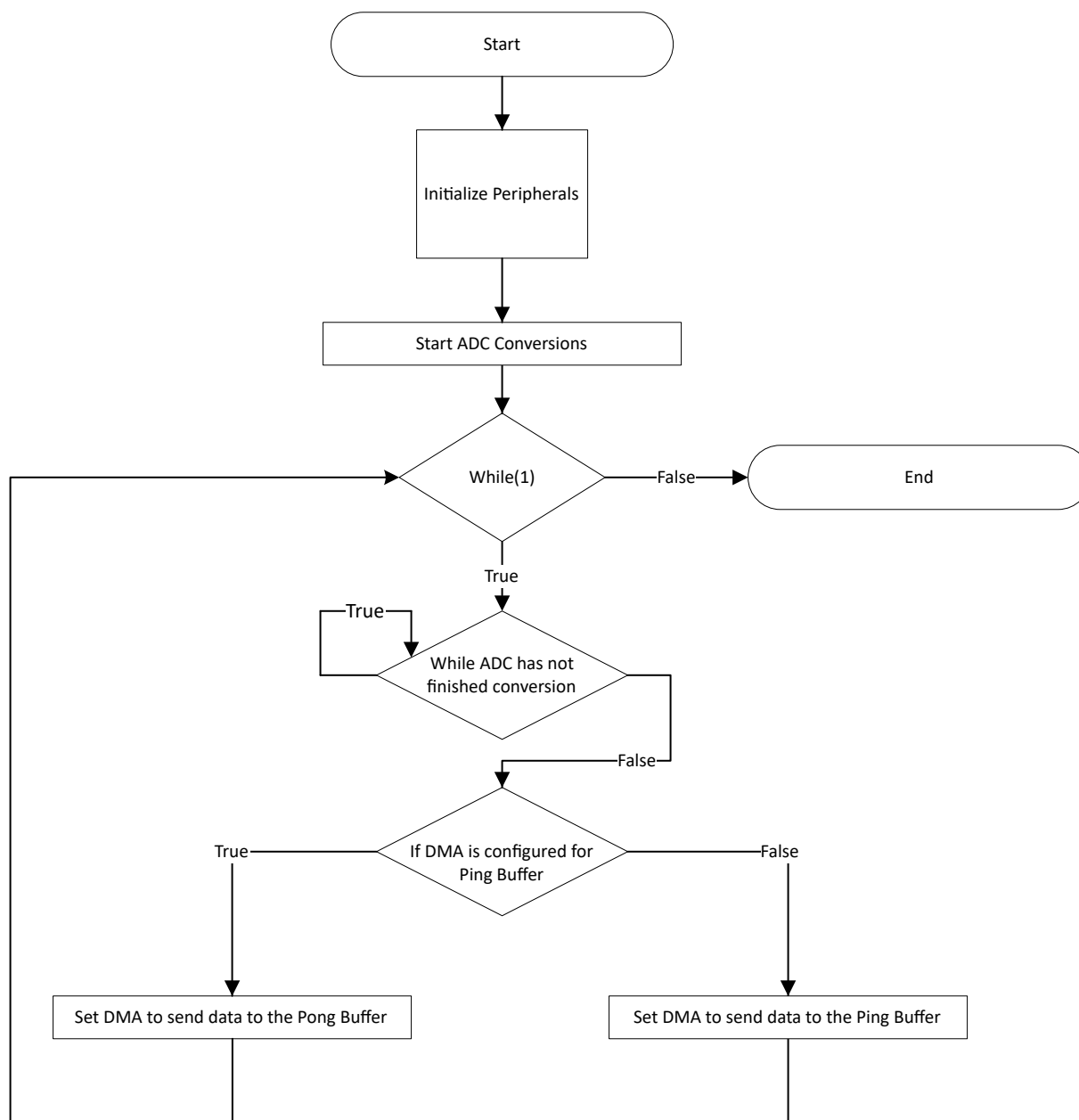


Figure 5-1. Software Flow Chart

6 Design Results

The following contents show the results of the code executing. [Figure 6-1](#) shows the results of the buffers after the first execution of the main loop. After the buffer is filled, the code swaps the DMA destination to the second buffer and the CPU is now free to utilize data in the first buffer.

Expression	Type	Value	Address
gADCSamplesPing	unsigned short[64]	[2612,2704,2792,2885,2965...]	0x20200000
gADCSamplesPong	unsigned short[64]	[0,0,0,0,0...]	0x20200080

Figure 6-1. Buffers After First Pass

[Figure 6-2](#) shows the results of the second buffer after the second execution of the main loop. After the buffer is filled, the code swaps the DMA destination back to the first buffer and now the CPU can use the data in the second buffer.

Expression	Type	Value	Address
gADCSamplesPing	unsigned short[64]	[2612,2704,2792,2885,2965...]	0x20200000
gADCSamplesPong	unsigned short[64]	[3240,3176,3109,3038,2944...]	0x20200080

Figure 6-2. Buffers After Second Pass

7 Additional Resources

- Texas Instruments, [Download the MSPM0 SDK](#)
- Texas Instruments, [Learn more about SysConfig](#)
- Texas Instruments, [MSPM0L LaunchPad™](#)
- Texas Instruments, [MSPM0G LaunchPad™](#)
- Texas Instruments, [MSPM0 ADC Academy](#)
- Texas Instruments, [MSPM0 DMA Academy](#)

8 E2E

See TI's [E2E™](#) support forums to view discussions and post new threads to get technical support for utilizing MSPM0 devices in designs.

9 Trademarks

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10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2024) to Revision B (September 2025)	Page
• Removed Compatible Devices section.....	1

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