Analog Engineer's Circuit

Smart DAC Sine-Wave Generation Circuit

Smart DAC

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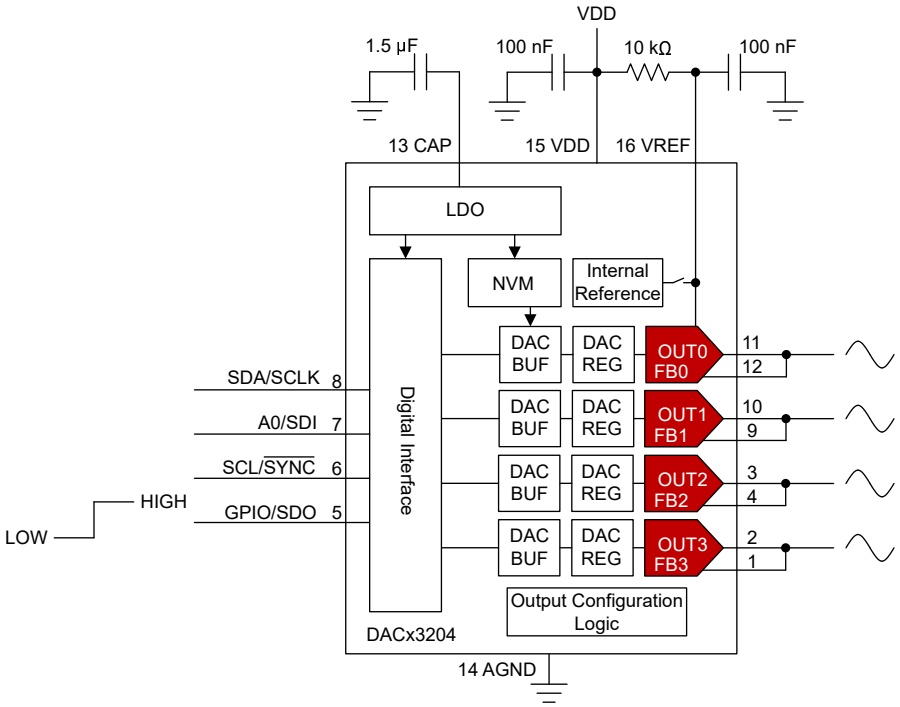
Design Objective

Key Input Parameter	Key Output Signal	Recommended Device
SPI or I^2C communication to set Frequency, Phase and Amplitude, GPI trigger to trigger the Sine Wave	Sine wave with a set frequency, phase and amplitude	DAC63204, DAC53204, DAC43204, DAC63004, DAC53004, DAC63202, DAC53202, DAC63002, DAC53002

Objective: Sine wave generation using a smart DAC.

Design Description

This design uses the internal function generation feature of the DAC63204, DAC53204, and DAC43204 (DACx3204) to generate a sine wave of a particular frequency, phase, and amplitude. The DACx3204 output cycles through 24 fixed DAC codes with variable slew times and gain settings to generate the sine wave. The DAC is used in voltage-output mode with the force sense outputs shorted close to the device. The DACx3204 has a general-purpose input/output (GPIO) pin which can be configured as an input pin to start and stop the sine wave using an external trigger. All register settings are saved using the integrated non-volatile memory (NVM), enabling the device to be used without run-time software, even after a power cycle or reset. This circuit can be used in grid infrastructure applications that use a built-in self-test that requires a sine wave or 3-phase sine wave as a test input, or building automation applications such as gas detectors that use a modulated reference to avoid DC shifts and noise reduction.

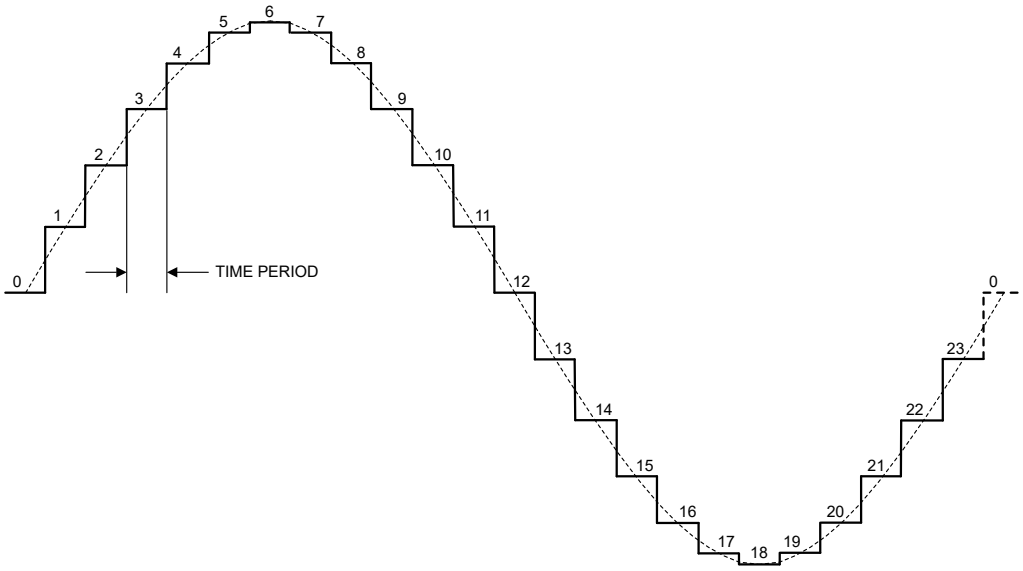


Design Notes

1. The *DACx3204 12-Bit, 10-Bit, and 8-Bit, Quad Voltage and Current Output Smart DACs With Auto-Detected I2C, PMBus™, or SPI Interface* data sheet recommends using a 100-nF decoupling capacitor for the VDD pin and a 1.5-µF or greater bypass capacitor for the CAP pin. The CAP pin is connected to the internal LDO. Place these capacitors close to the device pins.
2. Connect a 100-nF capacitor from VREF to GND if the external reference is used. Ramp up the external reference after VDD. Connect a pullup resistor from the VREF pin to VDD if the external reference is not used. This example uses the internal reference and the VREF pin is pulled up to VDD with a 10-kΩ resistor.
3. The internal sine wave generator uses 24 preprogrammed points per period:

Sine Wave DAC Codes

Sequence	12-Bit Value	Sequence	12-Bit Value
0 (0° phase start)	0x800	12	0x800
1	0x9A8	13	0x658
2	0xB33	14	0x4CD
3	0xC87	15	0x379
4	0xD8B	16 (240° phase start)	0x275
5	0xE2F	17	0x1D1
6 (90° phase start)	0xE66	18	0x19A
7	0xE2F	19	0x1D1
8 (120° phase start)	0xD8B	20	0x275
9	0xC87	21	0x379
10	0xB33	22	0x4CD
11	0x9A8	23	0x658



4. The sine wave function can be enabled by writing 0b100 to the FUNC-CONFIG field of the DAC-X-FUNC-CONFIG register.

5. The frequency for the 24-point sine wave is calculated using:

$$f_{sine\ wave} = \frac{1}{24 \times SLEW - RATE}$$

   Where SLEW-RATE is the time period per step (s/step) selected in the SLEW-RATE field of the DAC-X-FUNC-CONFIG register. SLEW-RATE in s/step is multiplied by the 24 steps to get the period of the sine wave in seconds.
6. The amplitude of the sine wave is determined by the reference and gain settings of the device. The device can use an external reference or VDD as the reference with a gain setting of ×1, or the 1.212-V internal reference with gain settings of ×1.5, ×2, ×3, or ×4. This is configured in the VOUT-GAIN-X field in the DAC-X-VOUT-CMP-CONFIG register. The maximum and minimum DAC codes of the sine wave are 0xE66 and 0x19A respectively (3686 and 410 in decimal). This represents 80% of the total DAC full scale range:

$$\frac{(3686 - 410)}{2^{12}} = 0.8$$

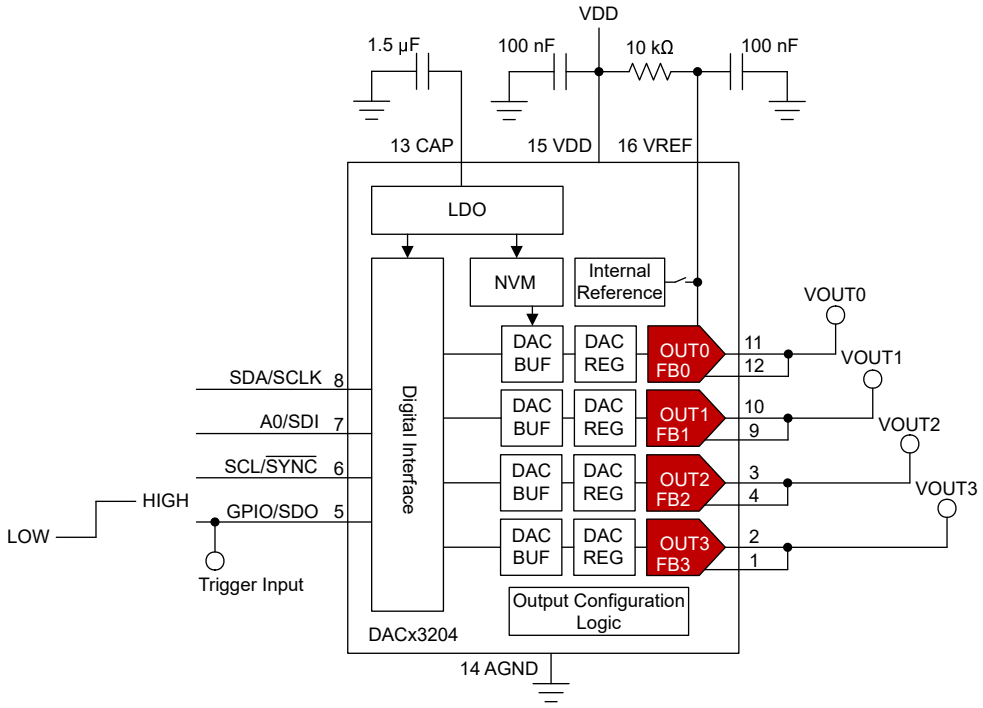
   The peak-to-peak amplitude of the sine wave is calculated in units of peak-to-peak voltage (Vpp) with:

$$A_{sine\ wave} = 0.8 \times Vref \times Gain$$

7. The phase is set using the PHASE-SEL field in the DAC-X-FUNC-CONFIG register. The code that the sine wave starts at when triggered is determined by the phase. PHASE-SEL is a 2-bit field that can set the phase to 0°, 120°, 240°, or 90°.
8. The GPIO pin can be configured to be a digital input pin for the start-stop function generation by appropriately setting the GPI-CONFIG bits in the GPIO-CONFIG register. This enables the sine wave to be triggered on the rising edge of the GPI pin. Disable the SDO output on the GPIO pin before configuring the GPIO pin as an input if the SPI is used.
9. The DACx3204 can be programmed with the initial register settings described in the Register Settings section using I^2C or SPI. Save the initial register settings in the NVM by writing a 1 to the NVM-PROG field of the COMMON-TRIGGER register. After programming the NVM, the device loads all registers with the values stored in the NVM after a reset or a power cycle.

Design Results

This schematic is used for the following design results of the DAC63204. The VOUTX and Trigger Input signals are measured on an oscilloscope at the test points marked on the schematic.

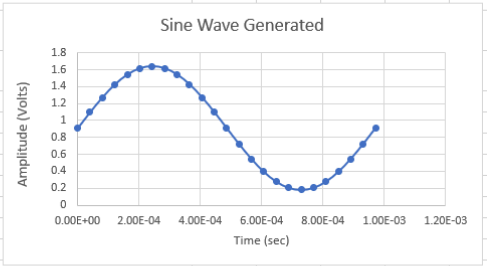


An excel-based calculator tool, DACX3X0X-SINEWAVE-CALC, is available to visualize the sine-wave generation feature on the DACx3x04 family of devices as well as generate the pseudocode required for a sine wave of a particular frequency and phase. The calculator tool shows the configuration settings used for each example in the design results.

Sine Wave Generation Using the Internal Reference

Use the excel calculator to configure the DAC63204 to generate a sine wave with a 1-kHz frequency, 0° phase, and the internal reference:

	A	B	C
1	Legend		
2	Parameters to be entered by the user		DAC Reference / Output Range(V)
3	Parameters calculated and presented to the user		Internal with 1.5x Gain 0-1.818V
4	Disabled cell		Internal with 2x Gain 0-2.424V
			Internal with 3x Gain 0-3.636V
			Internal with 4x Gain 0-4.848V
			VDD as reference 0-VDD
			External reference 0-VREF
5			
6	Device:	VDD (of DAC) (V)	VREF (if external ref selected) (V)
7	DAC63204	5	0
8			
9	Reference Selection	Gain (V/V)	Actual VREF (V)
10	Internal	1.5	1.818
11			
12	Frequency Selected (Hz)	Phase Selection (DEG)	Actual Frequency (Hz)
13	1000	0	1029.314888
14			SLEW-RATE Setting (µs/step)
15			40.48



The setting for the SLEW-RATE field is calculated by:

$$SLEW - RATE = \frac{1}{24\ steps \times 1000\ Hz} = 41.6\ \mu s/step$$

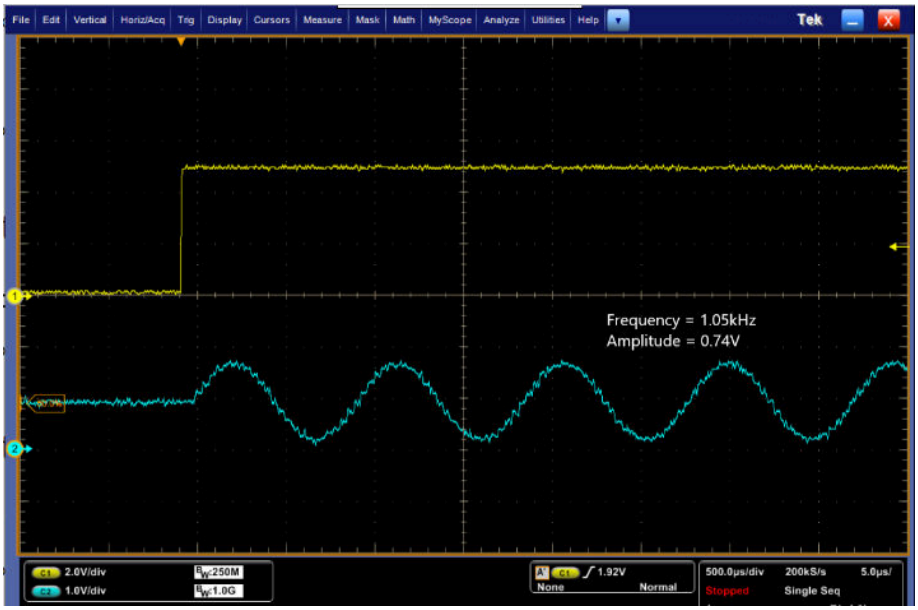
The nearest valid SLEW-RATE setting is 40.48 µs.

This actual frequency using this slew rate value is:

$$Actual\ Frequency = \frac{1}{24\ steps \times 40.48\ \mu s/step} = 1.029\ kHz$$

The peak-to-peak amplitude of this sine wave is:

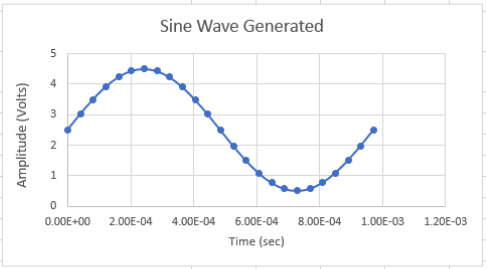
$$A_{sine\ wave} = 0.8 \times 1.212\ V \times 1.5 = 1.454\ Vpp$$



Sine-Wave Generation Using VDD as the Reference

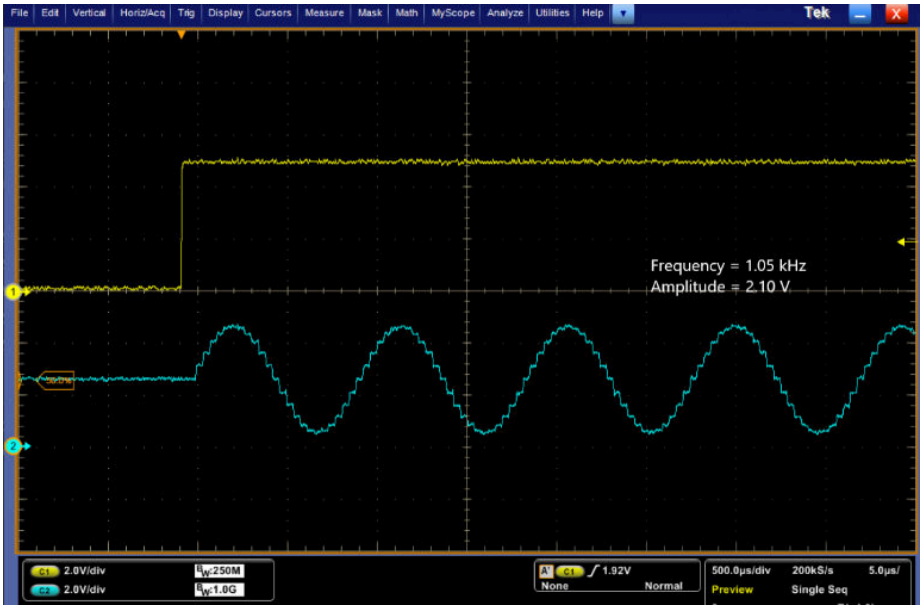
Use the excel calculator to configure the DAC63204 to generate a sine wave with a 1-kHz frequency, 0° phase, and VDD as the reference:

	A	B	C
1	Legend		
2	Parameters to be entered by the user		DAC Reference / Output Range(V)
3	Parameters calculated and presented to the user		Internal with 1.5x Gain 0-1.818V Internal with 2x Gain 0-2.424V Internal with 3x Gain 0-3.636V Internal with 4x Gain 0-4.848V VDD as reference 0-VDD External reference 0-VREF
4	Disabled cell		
5			
6	Device:	VDD (of DAC) (V)	VREF (if external ref selected) (V)
7	DAC63204	5	0
8			
9	Reference Selection	Gain (V/V)	Actual VREF (V)
10	VDD	1.5	5.000
11			
12	Frequency Selected (Hz)	Phase Selection (DEG)	Actual Frequency (Hz)
13	1000	0	1029.314888
14			SLEW-RATE Setting (µs/step)
15			40.48



The peak-to-peak amplitude of this sine wave is:

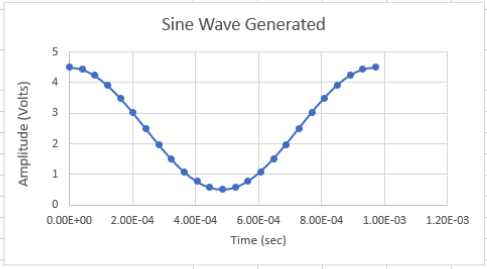
$$A_{sine\ wave} = 0.8 \times 5\ V \times 1 = 4\ Vpp$$

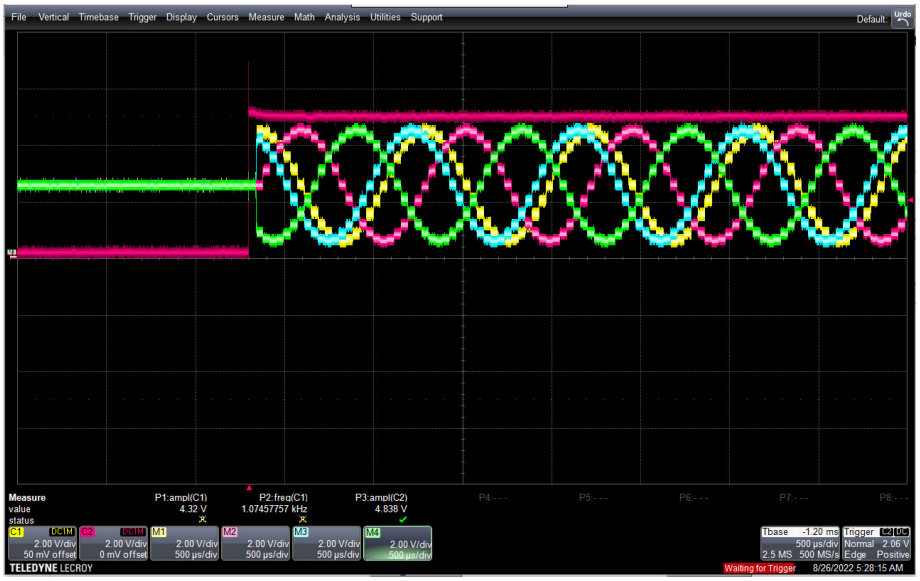


Sine Wave Generation With Four Output Channels

Use the excel calculator to configure the DAC63204 to generate a sine wave with a 1-kHz frequency, and the internal reference. Each channel is configured for a different phase. Channel 1 uses 90° phase:

	A	B	C
1	Legend		
2	Parameters to be entered by the user		DAC Reference / Output Range(V)
3	Parameters calculated and presented to the user		Internal with 1.5x Gain 0-1.818V Internal with 2x Gain 0-2.424V Internal with 3x Gain 0-3.636V Internal with 4x Gain 0-4.848V VDD as reference 0-VDD External reference 0-VREF
4	Disabled cell		
5			
6	Device:	VDD (of DAC) (V)	VREF (if external ref selected) (V)
7	DAC63204	5	0
8			
9	Reference Selection	Gain (V/V)	Actual VREF (V)
10	VDD	1.5	5.000
11			
12	Frequency Selected (Hz)	Phase Selection (DEG)	Actual Frequency (Hz)
13	1000	90	1029.314888
14			SLEW-RATE Setting (µs/step)
15			40.48





Register Settings

The following table shows an example register map for this application. The values given here are for the design choices made in the Sine Wave Generation with Four Output Channels section.

Register Settings for DAC63204 4-Channel Sine Wave Generation

Register Address	Register Name	Setting	Description
0x1F	COMMON-CONFIG	0x0249	[15] 0b0: Write 0b0 to set the window-comparator output to a non-latching output
			[14] 0b0: Device not locked
			[13] 0b0: Fault-dump read enable at address 0x00
			[12] 0b0: Disables the internal reference
			[11:10] 0b00: Powers up VOUT3
			[9] 0b1: Powers down IOUT3
			[8:7] 0b00: Powers up VOUT2
			[6] 0b1: Powers down IOUT2
			[5:4] 0b00: Powers up VOUT1
			[3] 0b1: Powers down IOUT1
			[2:1] 0b00: Powers up VOUT0
			[0] 0b1: Powers down IOUT0
0x24	GPIO-CONFIG	0x01F3	[15] 0b0: Glitch filter disabled for GP input
			[14] 0b0: Don't care
			[13] 0b0: Disable output mode for GPIO pin
			[12:9] 0b0000: Selects the STATUS function setting mapped to GPIO as output
			[8:5] 0b1111: Enables GPI function on all channels
			[4:1] 0b1000: GP input configured to start or stop the function generator
			[0] 0b1: Enables input mode for GPIO pin
0x20	COMMON-TRIGGER	0x0002	[15:12] 0b0000: Write 0b0101 to unlock the device
			[11:8] 0b0000: Write 0b1010 to trigger a POR reset
			[7] 0b0: LDAC is not triggered
			[6] 0b0: DAC clear is not triggered
			[5] 0b0: Don't care
			[4] 0b0: Fault-dump is not triggered
			[3] 0b0: PROTECT function not triggered
			[2] 0b0: Fault-dump read not triggered
			[1] 0b1: Write 0b1 to store applicable register settings to the NVM
			[0] 0b0: NVM reload not triggered. Write 0b1 to reload applicable registers with existing NVM settings
0x03, 0x09, 0x0F, 0x15	DAC-X-VOUT-CMP-CONFIG	0x0400	[15:13] 0b000: Don't care
			[12:10] 0b001: Selects VDD as reference with 1× gain
			[9:5] 0x00: Don't care
			[4] 0b0: Set OUTx pins as push-pull in comparator mode
			[3] 0b0: Comparator output consumed internally
			[2] 0b0: FBx input has high-impedance in comparator mode
			[1] 0b0: Comparator output not inverted
			[0] 0b0: Disable comparator mode

Register Settings for DAC63204 4-Channel Sine Wave Generation (continued)

Register Address	Register Name	Setting	Description
0x06, 0x0C, 0x12, 0x18	DAC-X-FUNC-CONFIG	0x1C06, 0x0406, 0x0C06, 0x1406	[15] 0b0: DAC-X clear mode set to zero-scale
			[14] 0b0: DAC-X output updates immediately after a write command
			[13] 0b0: Do not update DAC-X with broadcast command
			[12:11] 0b11, 0b00, 0b01, 0b10: Selects 90°, 0°, 120°, and 240° phase for output channels 0 to 3 respectively
			[10:8] 0b100: Selects sine wave mode
			[7] 0b0: Enable linear slew
			[6:4] 0b000: Selects CODE-STEP setting
			[3:0] 0x00: Selects SLEW-RATE setting

Pseudocode Example

The following shows a pseudocode sequence to program the initial register values to the NVM of the DAC63204. The values given here are for the design choices made in the Sine Wave Generation with Four Output Channels section.

Pseudocode Example for DAC63204 4-Channel Sine Wave Generation

```
1:  //SYNTAX: WRITE <REGISTER NAME (Hex code)>, <MSB DATA>, <LSB DATA>
2:  //Power-up voltage output on all channels, internal reference disabled
3:  WRITE GENERAL_CONFIG(0x1F), 0x02, 0x49
4:  //Configure Channel 0 with Gain=1x and VDD as reference
5:  WRITE DAC-0-VOUT-CMP-CONFIG(0x03),0x04,0x00
6:  //Configure Channel 1 with Gain=1x and VDD as reference
7:  WRITE DAC-1-VOUT-CMP-CONFIG(0x09),0x04,0x00
8:  //Configure Channel 2 with Gain=1x and VDD as reference
9:  WRITE DAC-2-VOUT-CMP-CONFIG(0x0F),0x04,0x00
10: //Configure Channel 3 with Gain=1x and VDD as reference
11: WRITE DAC-3-VOUT-CMP-CONFIG(0x15),0x04,0x00
12: //Configure GPIO for input and start stop function generation
13: WRITE GPIO_CONFIG(0x24), 0x01, 0xF3
14: //Configure Channel 0 for sine wave generation with 90° phase selection
15: WRITE DAC-0-FUNC-CONFIG(0x06), 0x1C, 0x06
16: //Configure Channel 1 for sine wave generation with 0° phase selection
17: WRITE DAC-1-FUNC-CONFIG(0x0C), 0x04, 0x06
18: //Configure Channel 2 for sine wave generation with 120° phase selection
19: WRITE DAC-2-FUNC-CONFIG(0x12), 0x0C, 0x06
20: //Configure Channel 3 for sine wave generation with 240° phase selection
21: WRITE DAC-3-FUNC-CONFIG(0x18), 0x14, 0x06
22: //Program NVM with the above settings
23: WRITE COMMON-TRIGGER(0x20),0x00,0x02
24: //Start and Stop the sine wave using the GPIO pin or writing to
```

Design Featured Devices

Device	Key Features	Link
DAC43204	4-channel, 8-bit, VOUT and IOUT smart DAC with I^2C, SPI, and Hi-Z out during power off	DAC43204
DAC53204	4-channel, 10-bit, VOUT and IOUT smart DAC with I^2C, SPI, and Hi-Z out during power off	DAC53204
DAC63204	4-channel, 12-bit, VOUT and IOUT smart DAC with I^2C, SPI, and Hi-Z out during power off	DAC63204

Find other possible devices using the Parametric search tool.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, DACX3X0X-SINEWAVE-CALC
- Texas Instruments, *DAC63204 Evaluation Module*
- Texas Instruments, *DAC63204 EVM User's Guide*
- Texas Instruments, Precision Labs - DACs

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