Application Note

TMUXHS4212 MUX vs DS160PR421 or DS160PR412 Redriver in PCIe GEN 4 Applications

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ABSTRACT

This application note details when redrivers or MUX devices are needed in PCIe Gen 4 applications. The document also describes how to set up and configure the HSDC092 evaluation board with TMUXHS4412 MUX or the DS160PR421 or DS160PR412 redriver to test PCI Express® (PCIe®) Generation 4 CBB and AIC compliance test. A test report is presented and discussed.

Table of Contents

List of Figures

List of Tables

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1 Introduction

The HSDC092 evaluation module provides a complete high-bandwidth platform for evaluating the signal-conditioning features of the DS160PR412 and DS160PR421 quad-channel PCI Express 4.0 linear redrivers. This evaluation board can be used for standard compliance testing, performance evaluation, and initial system prototyping.

The TMUXHS4412 is an analog differential passive multiplexer or demultiplexer which is P2P compatible with DS160PR412 and DS160PR421, thus HSDC092 EVM can be used to evaluate PCIe performance with TMUXHS4412 MUX as well.

2 When Redriver or Passive MUX is Needed?

Computer systems continue to become more and more complex. There are many components on the desktop or laptop motherboard. As a system designer, finding the right components for designs can be difficult. Understanding when and where to use multiplexers and redrivers in designs is very important.

2.1 When to use a Redriver

Each component in the system contributes to the loss, like PCB trace, connectors and cables, or gain from a redriver. In PCIe Gen 4.0 applications, the specification requires Rx-Tx link training to establish and optimize signal conditioning settings at 16Gbps . Normally, PCIe-compliant TX and RX are equipped with signal-conditioning functions and can handle channel losses of up to 28 dB at 8 GHz. If the system channel loss is more than 28 db , a redriver is needed to compensate the loss. With the DS160PR421 or DS160PR412 in the link, the total channel loss between a PCIe root complex and an end-point can be extended up to 42 dB at 8 GHz.

Figure 2-1 shows an electric link that models a single channel of a PCIe link and eye diagrams measured at different locations along the link. The source that models a PCIe Transmitter sends a 16-Gbps PRBS-15 signal with P7 presets. After a transmission channel with –30 dB at 8 GHz insertion loss, the eye diagram is fully closed. The DS160PR421, with CTLE set to the maximum (17 dB boost) together with the source TX equalization compensates for the losses of the pre-channel (TL1) and opens the eye at the output of the device.

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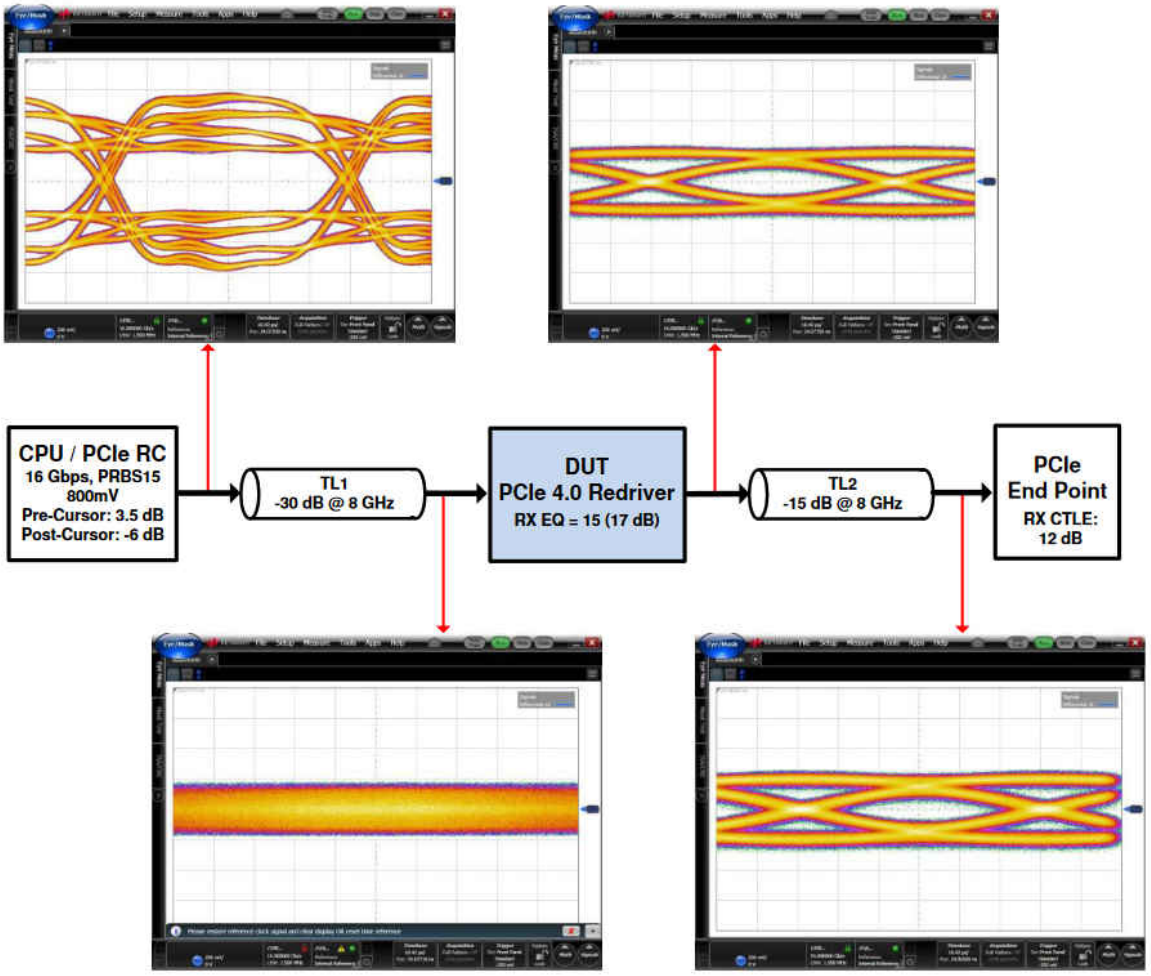

Figure 2-1. PCIe 4.0 Link Reach Extension Using the DS160PR421

2.2 When to use a Multiplexer

For eight-lane PCIe multiplexing applications, a topology is illustrated where two DS160PR412 and two DS160PR421 devices are used. There are system use cases where the PCIe link loss is low enough (< 28 db) that a signal conditioner such as linear redrivers are not needed. In such use cases, system engineers can consider passive multiplexers to achieve the same lane multiplexing topology. The four-channel passive multiplexer or demultiplexer TMUXHS4412 is pin-to-pin (p2p) compatible with the DS160PR412 and DS160PR421. This p2p component availability provides great flexibility for system implementation engineers where the need for a redriver is not completely clear. Figure 2-2 illustrates p2p passive MUX vs redriver option to implement PCIe lane switching.

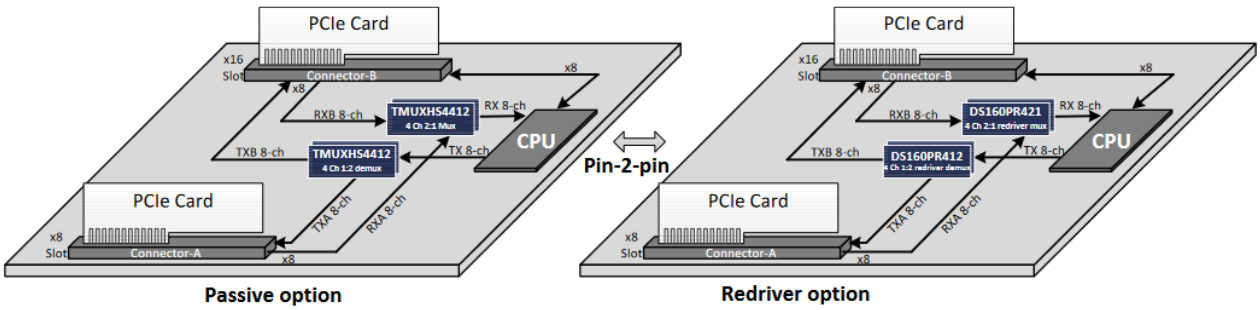

Figure 2-2. Pin-to-Pin Passive vs Redriver Option for PCIe Lane Switching

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3 Test Setup and Procedure

A PCI Express 4.0 CBB, AIC compliance test is required for any device to be listed on the PCI-SIG integrators list. This section presents the test setup and test procedure of PCI Express 4.0 CBB, AIC compliance test. The configuration of the HSDC092 evaluation board featuring the TMUXHS4412 is also discussed.

3.1 Test Board Configuration

The HSDC092 evaluation module is used for the PCI Express 4.0 compliance test. The module features two DS160PR412 and two DS160PR421 linear redrivers that can extend the transmission distance of a PCIe Gen 4 8 × bus. The EVM can be directly plugged into a PCIe slot on a server or PC motherboard using the PCIe edge connector on the board and paired with a PCIe add-in card using one of the two PCIe connectors on the EVM.

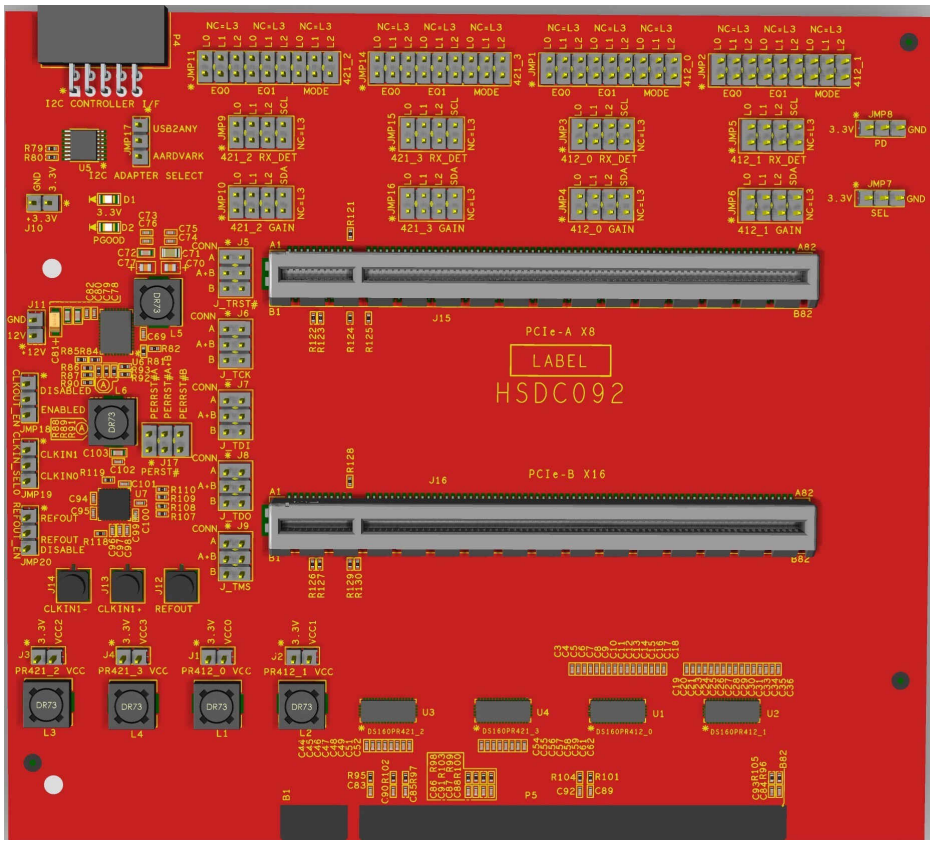

Figure 3-1. HSDC092 Evaluation Module

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Table 3-1 lists the board configuration for PCI Express 4.0 CBB, AIC compliance test.

Table 3-1. PCI Express 4.0 Compliance Test Configuration

SHNT#	Header	MUX SHNT#	412 or 421 SHNT#
1	JMP7	1–2	1-2
2	JMP8	2–3	2-3
3	JMP1	float	1-2,7-8,13-14
4	JMP2	float	1-2,7-8,13-14
5	JMP3	float	float
6	JMP4	float	float
7	JMP5	float	float
8	JMP18	float	2-3
9	JMP19	float	2-3
10	JMP20	float	2-3
11	JMP11	float	1-2,7-8,13-14
12	JMP14	float	1-2,7-8,13-14
13	JMP17	float	1-2,3-4,5-6

3.2 Test Setup

Figure 3-2 is the setup for PCI Express TX CBB, AIC compliance test. The required hardware includes:

- HSDC092 evaluation board
- PCI-SIG CBB4 board
- CPI-SIG ISI board
- TekTronic DPO77002SX scope

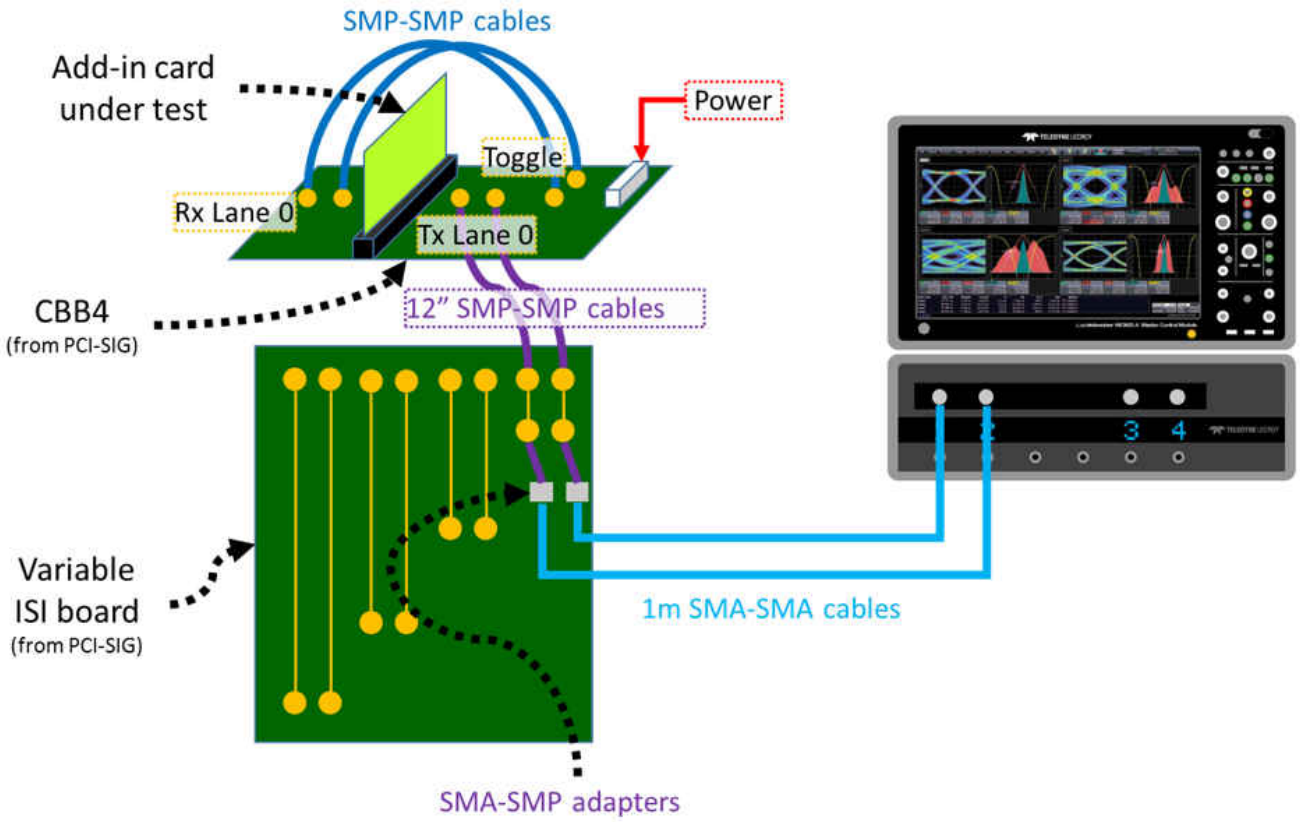

Figure 3-2. PCI Express 4.0 TX CBB, AIC Test Setup

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3.3 Test Procedure

The following steps show the test procedure:

1. Configure the HSDC092 evaluation board as detailed in PCI Express 4.0 Compliance Test Configuration.
2. Plug the EVM into a PCIe 16 × server motherboard slot. Make sure the motherboard is powered down before installing the EVM or configured for hot-plug operation.
3. Install a compatible PCIe endpoint card into one of the PCIe connectors (J16) on the EVM based on configuration of the SEL pin.
4. Power-up the motherboard.
5. Run PCIe CBB, AIC compatibility compliance test suite on the scope to check P0–P10 presets.
6. Attach PCIe SIG compliance board media (ISI board) and the output of this transmission line goes to the Tek scope.
7. Checked Broadcom end point by itself only and ran CBB test.
8. Attached the same end point into J16 and performed CBB test again.

3.4 Test Report

3.4.1 Test Summary

TX presets: BRCM, J16 meets the PCI Express 4.0 requirement.

ISI eye openings:

- BRCM meets all preset requirements
- J16 is able to pass P06, P07, P08, and P09 only. Technically, at least one preset needs to pass to claim compatibility

Figure 3-3 and Figure 3-4 illustrate the test reports for preset and ISI eye opening tests.

TekExpress PCI Express

Add-In-Card Test Report

Setup Information			
DUT ID	DUT001	DPOJET Version	10.0.7.9
Date/Time	2020-11-18 16:51:50	Scope Model	DPO77002SX
Device Type	CEM	Scope Serial Number	B000001
TekExpress Version	PCI Express:10.5.0.73 (Alpha)	SPC, FactoryCalibration	PASS;PASS
TekExpress Framework Version	4.15.0.2	Scope F/W Version	10.8.6 Build 29
Test Mode	SigTest Compliance	Probe1 Model	TCA292D
Spec Version	Gen4 - 4.0	Probe1 Serial Number	N/A
SigTest Version	3.2.0.3(Gen1,2,3) 4.0.51 (Gen4)-Signal Tests 4.0.51 (Gen4)-Preset Tests	Probe2 Model	none
		Probe2 Serial Number	N/A
Embed Filter File	Gen4 refpkg_rootcomplex_5db_thru.flt	Probe3 Model	TCA292D
Slot Number	01	Probe3 Serial Number	N/A
Overall Test Result	Pass	Probe4 Model	none
Overall Execution Time	0:08:18	Probe4 Serial Number	N/A
		Sigtest Template	Gen4: PCIe_4_16G_CEM.dat
		SSC Status	Off

PRESET RESULTS

Preset Name	Lane Name	PreShoot	De-Emphasis	Vb	Result
P0 Gen4	Lane0	0.000 dB	-6.085 dB	491.560 mV	Pass
P10 Gen4	Lane0	0.000 dB	-8.676 dB	364.773 mV	Pass
P01 Gen4	Lane0	0.000 dB	-3.540 dB	658.937 mV	Pass
P02 Gen4	Lane0	0.000 dB	-4.677 dB	578.047 mV	Pass
P03 Gen4	Lane0	0.000 dB	-2.522 dB	740.875 mV	Pass
P04 Gen4	Lane0	0.000 dB	0.000 dB	990.426 mV	Pass
P05 Gen4	Lane0	2.082 dB	0.000 dB	779.376 mV	Pass
P06 Gen4	Lane0	2.502 dB	0.000 dB	742.529 mV	Pass
P07 Gen4	Lane0	4.024 dB	-6.620 dB	363.705 mV	Pass
P08 Gen4	Lane0	3.600 dB	-3.619 dB	489.499 mV	Pass
P09 Gen4	Lane0	3.547 dB	0.000 dB	658.358 mV	Pass

Figure 3-3. Test Report of Presets - 1

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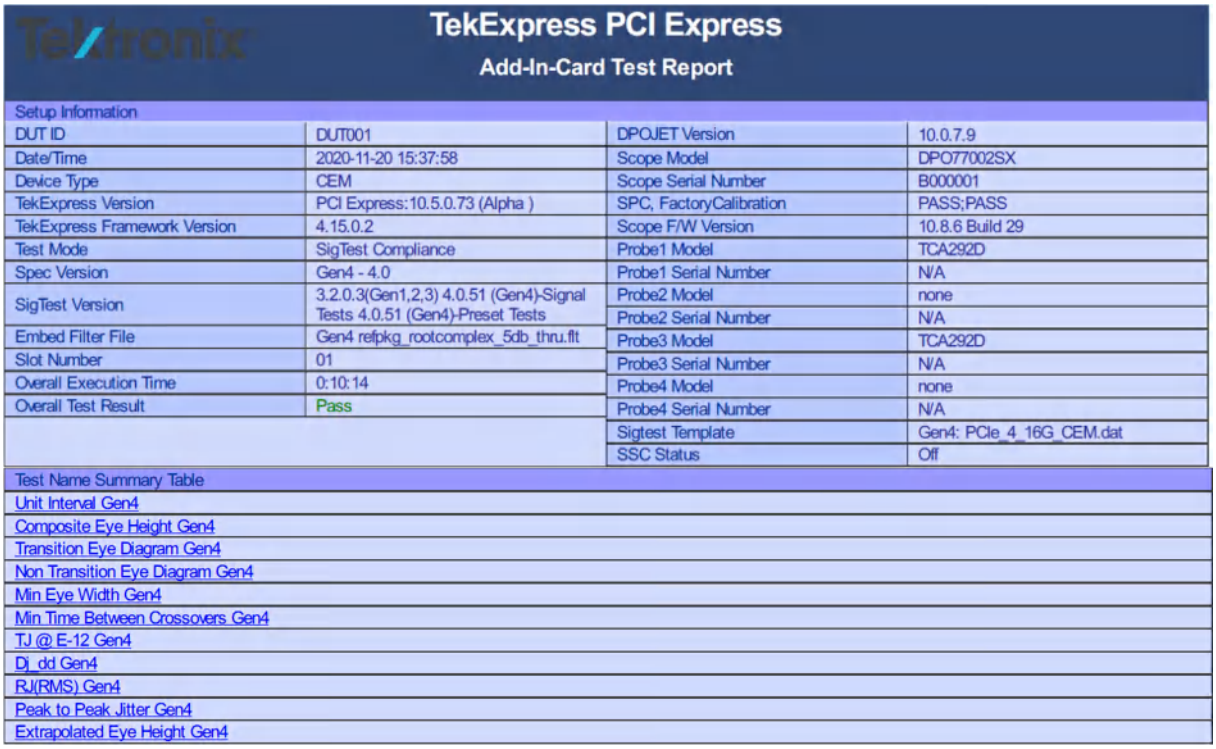

TekExpress PCI Express

Add-In-Card Test Report

Setup Information			
DUT ID	DUT001	DPOJET Version	10.0.7.9
Date/Time	2020-11-20 15:37:58	Scope Model	DPO77002SX
Device Type	CEM	Scope Serial Number	B000001
TekExpress Version	PCI Express:10.5.0.73 (Alpha)	SPC, FactoryCalibration	PASS;PASS
TekExpress Framework Version	4.15.0.2	Scope F/W Version	10.8.6 Build 29
Test Mode	SigTest Compliance	Probe1 Model	TCA292D
Spec Version	Gen4 - 4.0	Probe1 Serial Number	N/A
SigTest Version	3.2.0.3(Gen1,2,3) 4.0.51 (Gen4)-Signal Tests 4.0.51 (Gen4)-Preset Tests	Probe2 Model	none
		Probe2 Serial Number	N/A
Embed Filter File	Gen4 refpkg_rootcomplex_5db_thru.flt	Probe3 Model	TCA292D
Slot Number	01	Probe3 Serial Number	N/A
Overall Execution Time	0:10:14	Probe4 Model	none
Overall Test Result	Pass	Probe4 Serial Number	N/A
		Sigtest Template	Gen4: PCIe_4_16G_CEM.dat
		SSC Status	Off

Test Name Summary Table
Unit Interval Gen4
Composite Eye Height Gen4
Transition Eye Diagram Gen4
Non Transition Eye Diagram Gen4
Min Eye Width Gen4
Min Time Between Crossovers Gen4
TJ @ E-12 Gen4
Dj_dd Gen4
RJ(RMS) Gen4
Peak to Peak Jitter Gen4
Extrapolated Eye Height Gen4

Figure 3-4. ISI Test Report

4 Summary

This application note covered when a redriver or high-speed MUX device is needed for PCIe Gen4 applications. Additionally, a description of the test setup and procedures of PCI Express 4.0 CBB, AIC compliance test using the TMUXHS4412 device or DS160PR412 or DS160PR421 redriver was provided. The test report was also presented.

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