Application Note

Analog Time Gain Control (ATGC) Solutions for TI's Ultrasound AFE

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ABSTRACT

TI's low-noise analog front ends (AFE) have a time gain control (TGC) feature that helps achieve the best possible signal-to-noise ratio (SNR) for ultrasound applications. This application note describes the specifications and design considerations of a circuit used for generating a time-varying V_{CNTL} to drive multiple AFE receiver chips. The document discusses three different proposals to achieve noise performance. Also included is a detailed description of the circuits and how PSPICE simulations can be used for noise analysis.

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Trademarks

1 Introduction

Ultrasound imaging is based on the pulse-echo method, by sending ultrasound waves to the objects being imaged and receiving echo signals. It is also known that the emitted ultrasound wave amplitude gets smaller as the wave penetrates tissue, a phenomenon called attenuation. Signals that are reflected immediately after transmission are very strong because the signals are from reflections close to the surface; reflections that occur long after the transmit pulse are very weak because these signals are reflecting from deep in the body. If the ultrasound image was formed directly by the raw returned echoes, the image appears lighter in the superficial layers and darker in deep layers. A way to overcome ultrasound attenuation is time gain control or compensation (TGC), in which signal gain is increased as time passes from the emitted wave pulse. This correction makes equally echogenic tissues look the same even if the tissue is located in different depths. TI's low-noise analog front ends (AFEs) have a TGC feature that supports ultrasound applications because the AFEs can alter the gain of the receiver as a function of time. The ultrasound signal incident on the receiver decreases in amplitude as a function of the time elapsed since transmission, and the TGC helps achieve the best possible signal-to-noise ratio (SNR), even with the decreasing signal amplitude.

This application note describes the specifications and design considerations of three proposal circuits used for generating a time-varying control voltage to drive multiple AFE receiver chips. Figure 1-1 shows the signal chain of the AFE58JD48 analog front end. The TGC function is integrated and is implemented using an attenuator that can be controlled with a control voltage, V_{CNTL}. External circuitry comprised of a digital-to-analog converter (DAC) and operational amplifier (op amp) generates the control signal. The input signal for the DAC is a time-varying digital control from a field programmable gate array (FPGA) that can also handle the beamforming operation required in an ultrasound application.

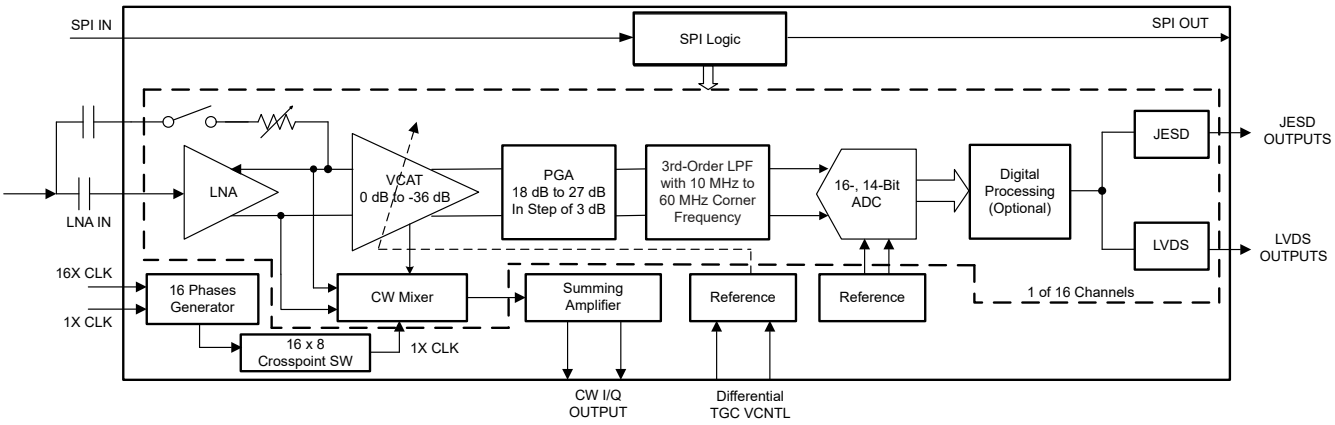

Figure 1-1. Signal Chain of the AFE58JD48 and Analog Control for TGC Operation

V_{CNTL} attributes from the point of view of the AFE are provided in the following list.

- **Signal levels on the control pins of AFE:** In the case of the AFE58JD48, V_{CNTL} (= V_{CNTLP} – V_{CNTLM}) is a differential input for controlling the voltage attenuation, ranging from –0.4 V to 0.4 V. The common-mode voltage for V_{CNTLP}, V_{CNTLM} is 1.3 V typically. This control voltage varies the attenuation of the attenuator based on the linear-in-dB characteristic. For single-ended operation, V_{CNTLM} can be fixed to 1.3 V and V_{CNTLP} can be swept from 0.9 V to 1.7 V. For fully-differential operation, (V_{CNTLP}, V_{CNTLM}) goes from (1.1 V, 1.5 V) to (1.5 V, 1.1 V). Figure 1-2 shows the relationship between V_{CNTL} voltage and VCAT attenuation. When the differential voltage level (V_{CNTLP} – V_{CNTLM}) exceeds the range of (–0.4 V to 0.4 V), the attenuator continues to operate at the maximum or minimum attenuation level.

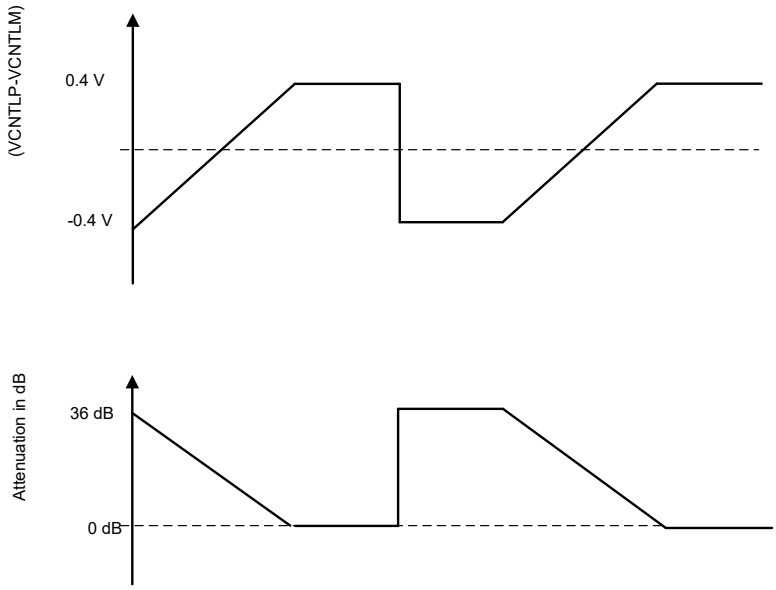

Figure 1-2. Relationship Between V_{CNTL} Voltage and Attenuation

- **Input referred noise:** As the received ultrasound signal decreases as a function of elapsed time, V_{CNTL} also decreases to reduce the attenuation and increase the channel gain. Figure 1-3 shows the benefit of the TGC circuit. As V_{CNTL} increases and the channel gain increases, the input-referred noise of the receiver also continues to decrease. The reduced noise helps arrest the SNR fall related to the declining amplitude of the receiver signal.

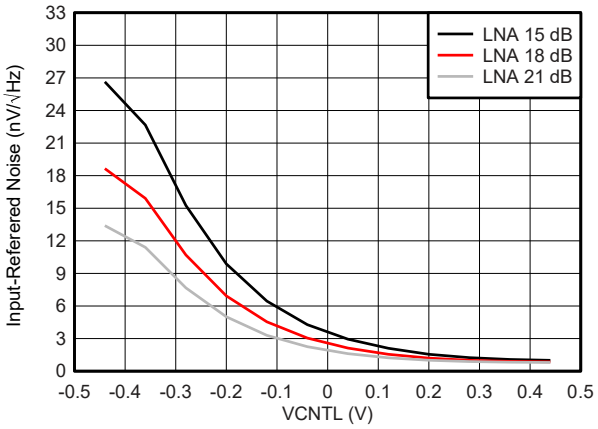

Figure 1-3. Input-Referred Noise vs V_{CNTL} and LNA Gains for Low-Noise Mode

- **Noise requirement for multiple channels:** One key consideration in the design of the V_{CNTL} drive circuit is the noise specification on V_{CNTL}. Since V_{CNTL} is a common control voltage across multiple channels of the AFE (and possibly shared with the channels of other AFE chips), any noise on V_{CNTL} shows up as a source of noise that is correlated across the multiple AFE channels that share that same V_{CNTL}. Noise at the V_{CNTL} pins must be low enough to obtain good system performance because this noise is correlated across channels. Figure 1-4 shows the allowed noise on V_{CNTL} as a function of the number of channels sharing the same V_{CNTL} drive.

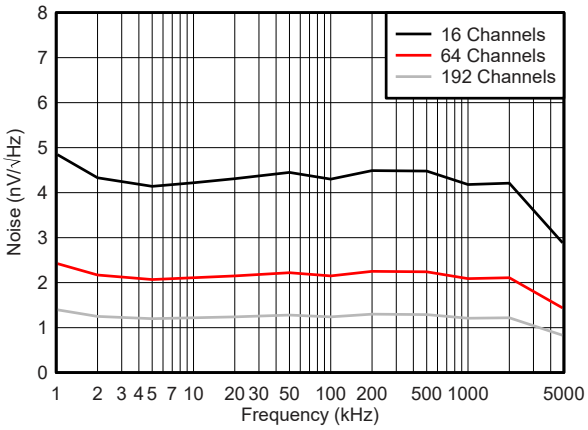

Figure 1-4. Allowed Noise on the V_{CNTL} Signal Across Frequency and Different Channels

2 Proposed Topologies

As previously mentioned, analog TGC (ATGC) circuits need to be designed to meet a variety of requirements, such as noise performance, level requirements, control accuracy requirements, and so forth. Thus, to meet different needs of customers and help them to complete the design, TI offers three different TGC designs that engineers can comprehensively evaluate based on the number of channels, noise performance requirements, and cost of their own products, and then choose the appropriate ATGC driver circuit for their needs. There are multiple approaches for a TGC control circuit that are based on the type of DAC.

2.1 Proposal 1: Using R-2R DAC (DAC8830)

2.1.1 Highlighted Products

2.1.1.1 DAC8830

The DAC8830 is a single, 16-bit, voltage-output DAC designed to operate from a single 2.7-V to 5.5-V supply. The device provides excellent linearity (1 LSB INL), low glitch, low noise, and fast settling (1.0 µs to 1/2 LSB of full-scale output) over the specified temperature range of –40°C to +85°C. The output is unbuffered, which reduces the power consumption and the error introduced by the buffer. The output is 0 V to V_{REF}. The DAC has a 1-µs settling time and output spot noise of 10 nV/$\sqrt{Hz}$.

2.1.1.2 OPA2210

The OPA2210 precision operational amplifier (op amp) is built on TI's precision, super-beta, complementary bipolar semiconductor process, which achieves very low-voltage noise density (2.2 nV/$\sqrt{Hz}$ at 1 kHz) with rail-to-rail output swing to maximize the dynamic range. This op amp is specified over a wide dual power-supply range of ±2.25 V to ±18 V.

2.1.1.3 THS4130

The THS4130 is a fully-differential amplifier providing very low noise (1.25 nV/$\sqrt{Hz}$) to provide maximum SNR and dynamic range. With a slew rate of 51 V/µs and gain bandwidth product of 215 MHz, the device is able to operate with a ±2.5- to ±15-V supply.

2.1.1.4 REF5040

The REF5040 is a low-noise, low-drift, very high-precision voltage reference. This reference is capable of both sinking and sourcing current and have excellent line and load regulation. The REF5040 has excellent temperature drift (3 ppm/°C) and high accuracy (0.05%). The noise is 3 μV_{PP}/V.

2.1.2 Design Circuit

Figure 2-1 shows a high-level block diagram for the topology using a R-2R-DAC to generate the drive for V_{CNTL}. This method uses the REF5040 as the reference voltage source and the VOCM (1.3 V) is obtained by the resistor divider, the output voltage has a typical requirement of low noise and fast settling.

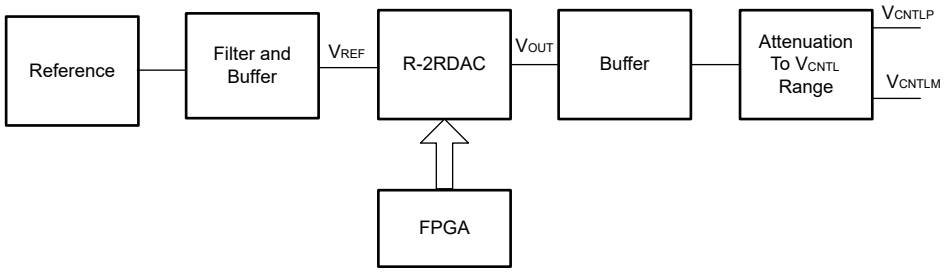

Figure 2-1. A R-2R DAC Used in Generating a TGC Signal

The output of the DAC is buffered first and then followed by attenuation, helps attenuate noise contributions from the reference circuit and the DAC. Figure 2-2 shows the entire drive circuit for the control voltage.

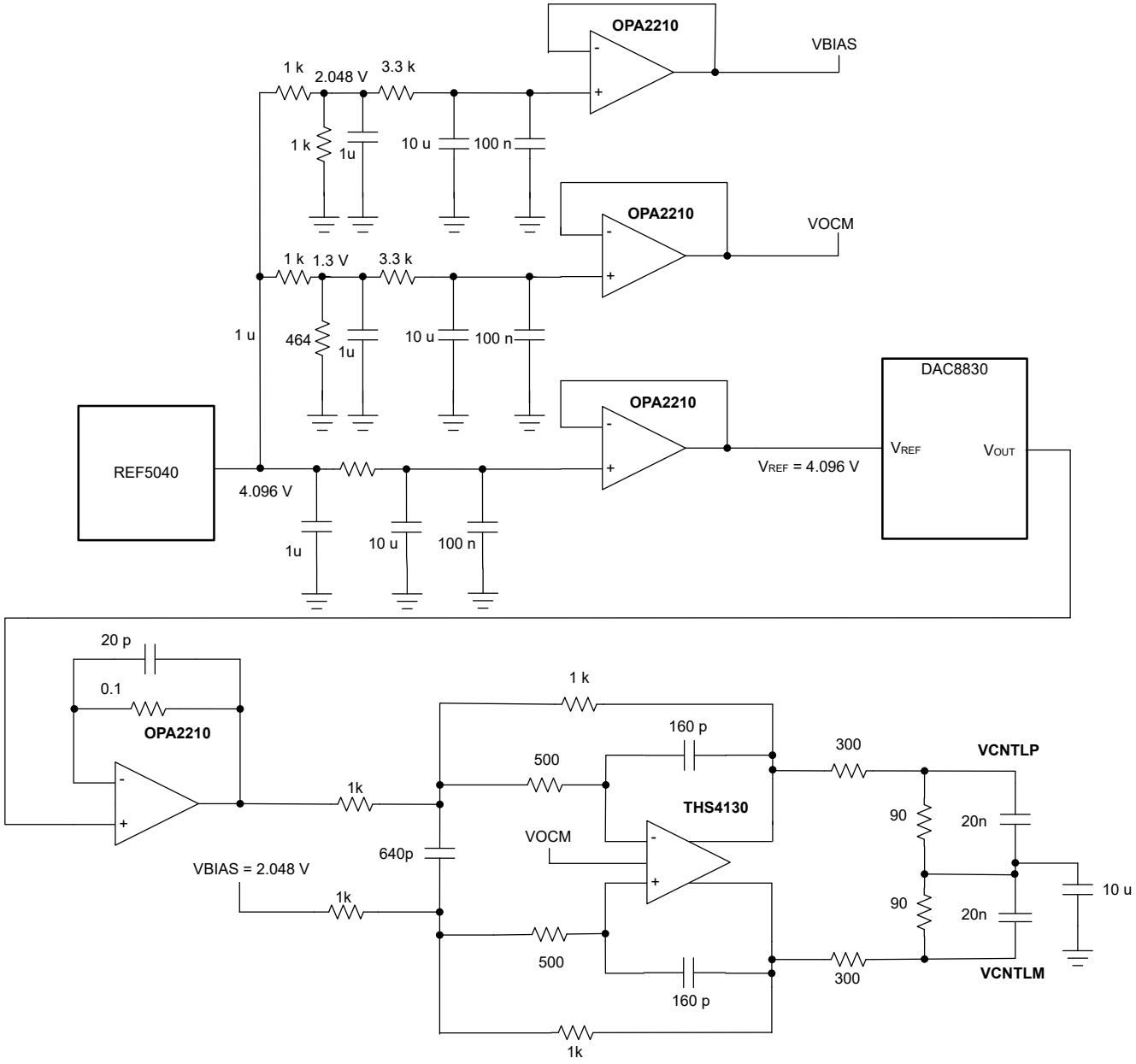

Figure 2-2. Proposal 1-V_{CNTL} Drive Circuit

2.1.3 PSpice-TI Simulation

Download the PSpice-TI simulation models for the relevant components from https://www.ti.com. Figure 2-3 shows the PSpice -TI simulation for the entire proposal 1 circuit.

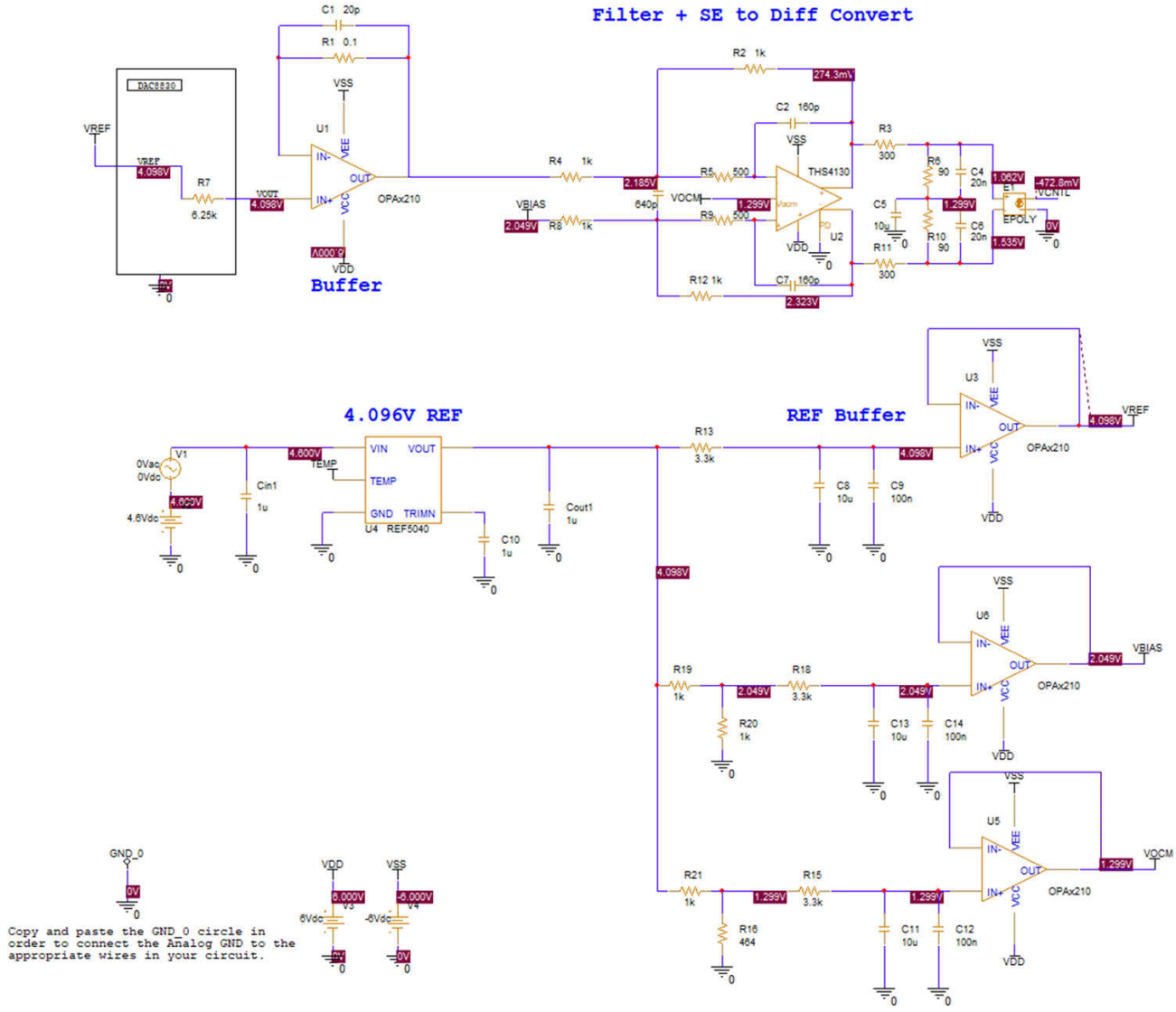

Figure 2-3. PSpice-TI Simulation of the Proposal 1 V_{CNTL} Drive Circuit

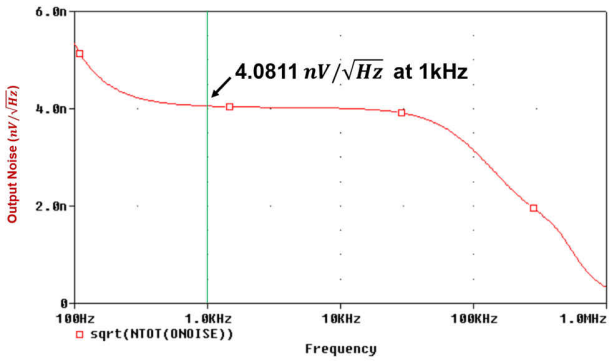

Figure 2-4. Noise Contribution of the Proposal 1 Circuit

Figure 2-4 shows the noise contribution of the proposal 1 circuit, the output noise of 4.0811 nV/√Hz at 1 kHz indicates that such a drive circuit can drive at least 16 channels simultaneously.

2.2 Proposal 2: Using M-DAC (DAC8801)

2.2.1 Highlighted Products

2.2.1.1 DAC8801

The DAC8801 multiplying digital-to-analog converter is designed to operate from a single 2.7-V to 5.5-V supply. The applied external reference input voltage V_{REF} determines the full-scale output current. An internal feedback resistor (RFB) provides temperature tracking for the full-scale output when combined with an external I-to-V precision amplifier. The DAC has a 0.5-µs settling time and output spot noise of 12 nV/√Hz.

2.2.1.2 OPA2210

The OPA2210 precision operational amplifier (op amp) is built on TI's precision, super-beta, complementary bipolar semiconductor process, which achieves very low-voltage noise density (2.2 nV/√Hz at 1 kHz) with rail-to-rail output swing to maximize the dynamic range. This op amp is specified over a wide dual power-supply range of ±2.25 V to ±18 V.

2.2.1.3 THS4130

The THS4130 is a fully-differential amplifier providing very low noise (1.25 nV/√Hz) to provide maximum SNR and dynamic range. With a slew rate of 51 V/µs and gain bandwidth product of 215 MHz, the device is able to operate with a ±2.5- to ±15-V supply.

2.2.1.4 REF5010

The REF5010 is a low-noise, low-drift, very high-precision 10-V voltage reference. This reference is capable of both sinking and sourcing current and have excellent line and load regulation. The REF5010 has excellent temperature drift (3 ppm/°C) and high accuracy (0.05%). The noise is 3 μV_{PP}/V.

2.2.2 Design Circuit

This section recommends another approach for a TGC control circuit with a multiplying DAC (MDAC) to generate the drive for V_{CNTL}. Figure 2-5 shows a high-level block diagram of this topology. Even though the V_{CNTL} range is from –0.4 V to 0.4 V, a much higher reference voltage, V_{REF} = 10 V, is used for the DAC. Filtering the reference voltage removes high-frequency noise and the DAC generates an output range of 0 to V_{REF}. The output of the DAC is buffered using an op amp to a level of –VREF to 0. Additional signal conditioning can involve low-pass filtering to reduce the noise bandwidth. Finally, an attenuation circuit reduces the range to the desired VCNTL range using a R-2R-DAC to generate the drive for V_{CNTL}.

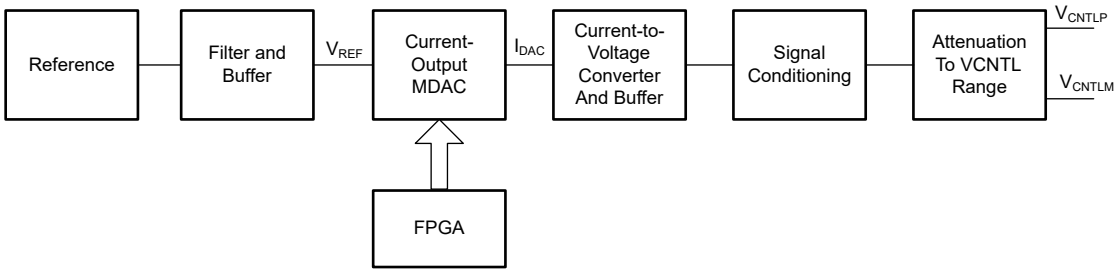

Figure 2-5. A Current-Output MDAC is Used in Generating a TGC Signal

The previous approach that starts off with a high-reference voltage and high DAC full-scale range, followed by attenuation, helps attenuate noise contributions from the reference circuit and the DAC, as well as other op amps used for signal conditioning. Using this topology, Figure 2-6 shows the drive circuit for the control voltage.

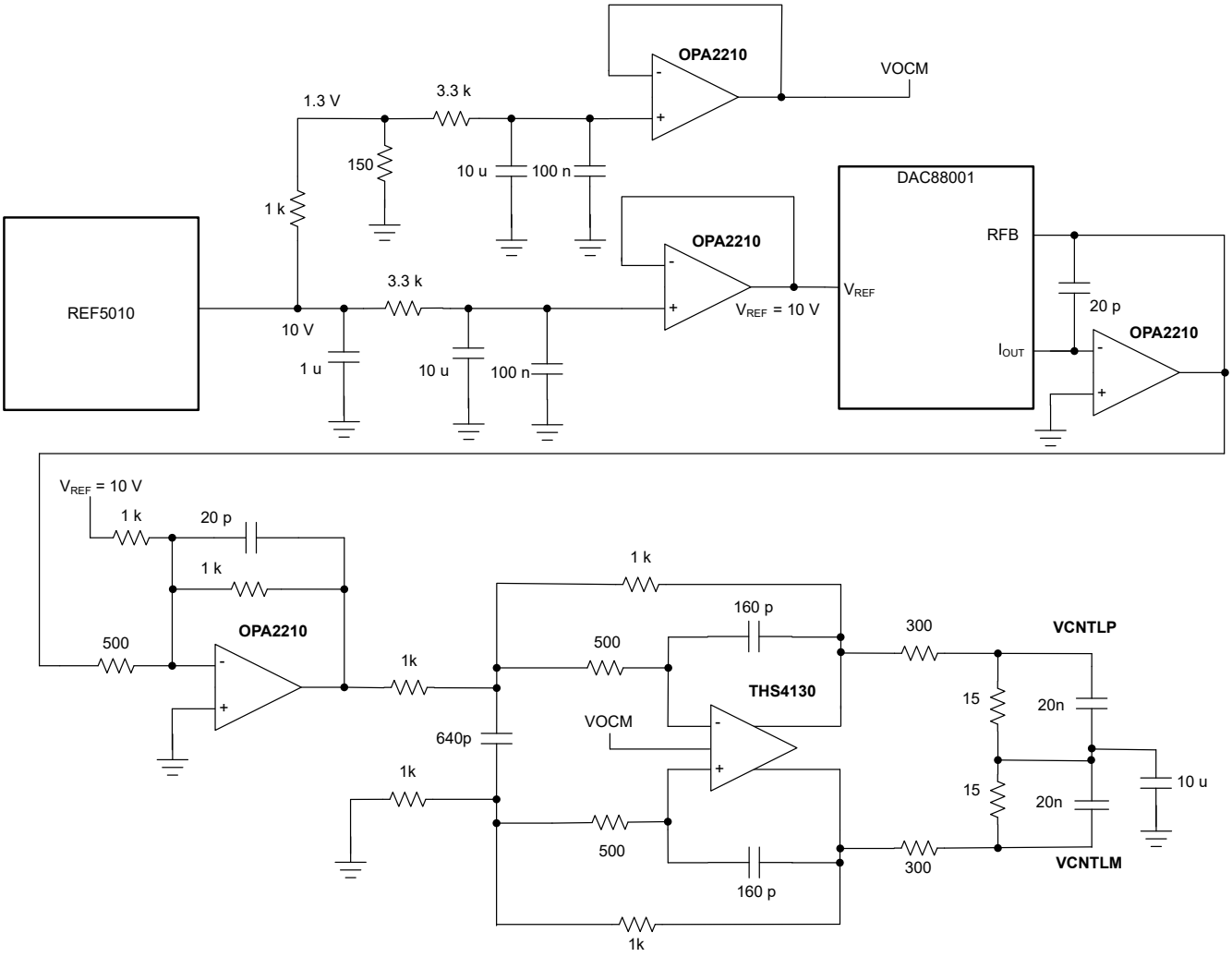

Figure 2-6. Proposal 2 V_{CNTL} Drive Circuit

The REF5010 generates a 10-V reference voltage that is filtered and buffered to generate VREF_10V. This serves as the reference voltage for the DAC8801, which generates a current output on I_{OUT} corresponding to the digital input code. The I_{OUT} pin of the DAC8801 is connected to the virtual ground (negative terminal) of the OPA2210; the feedback resistor (RFB is internal to the DAC8801) is connected to the output of the OPA2210, resulting in a current-to-voltage conversion. The output of the OPA2210 has a range of –10 V to 0 V and it is input to the THS4130, which is configured as a Sallen-Key filter. Finally, the 10-V range is attenuated down to a –0.4-V to 0.4-V range, with a common mode of 1.3 V using a resistive attenuator.

2.2.3 PSpice-TI Simulation

Download the PSpice-TI simulation models for the relevant components from https://www.ti.com. The reference section of the circuit shown in Figure 2-6 can be simulated in PSpice-TI (shown in Figure 2-7) and noise analysis can be performed.

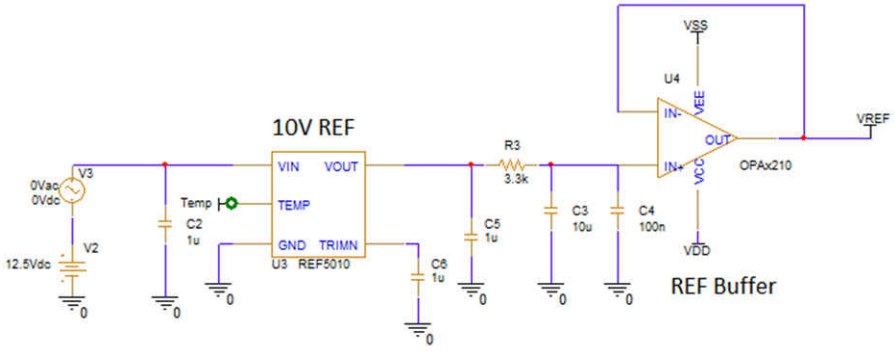

Figure 2-7. PSpice-TI Simulation for Reference Circuit (in previous image)

This noise is bandwidth-limited using the resistor-capacitor (R-C) filter at the output. Figure 2-8 shows the simulated results for the noise contribution from REF5010. Figure 2-9 shows the modeled noise contribution of the DAC8801 at the maximum output current.

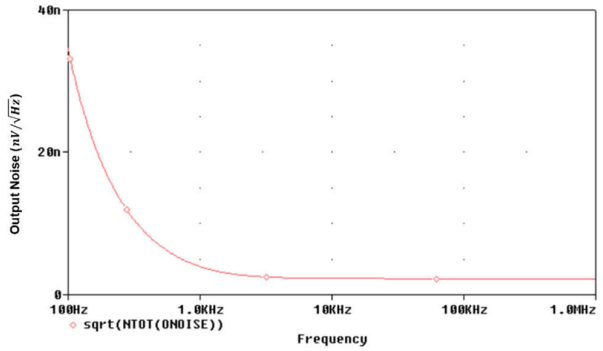

Figure 2-8. Noise Contribution From the Reference Circuit

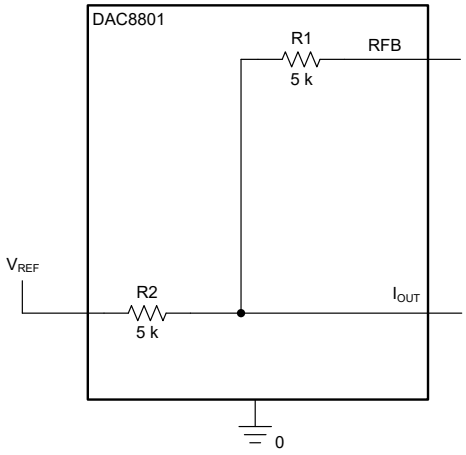

Figure 2-9. Noise Model for the DAC8801

Figure 2-10 shows the PSpice -TI simulation for the entire circuit.

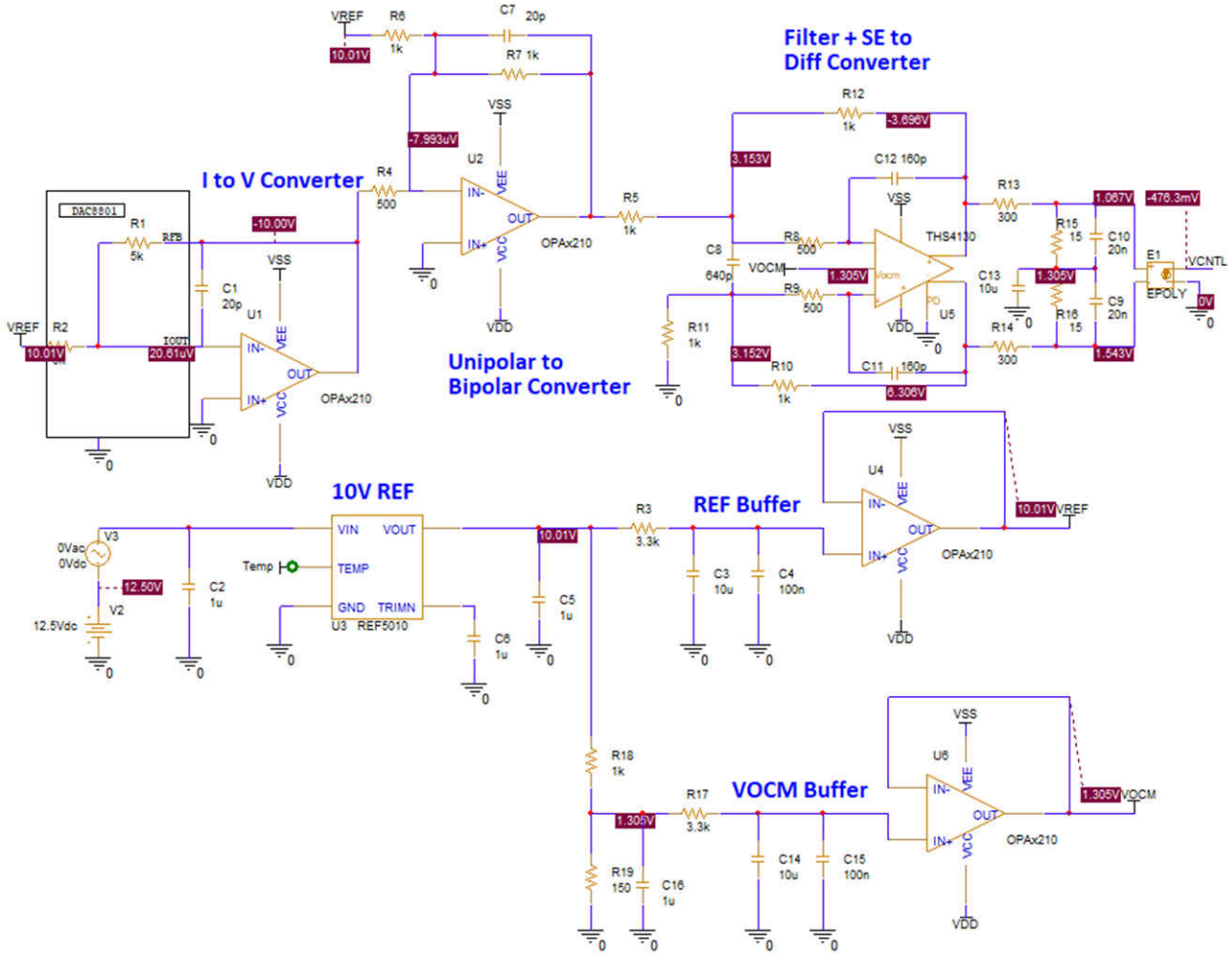

Figure 2-10. PSpice-TI Simulation of the Proposal 2 V_{CNTL} Drive Circuit

Figure 2-11 shows the noise contribution of the proposal 2 circuit, the output noise of 1.703 nV/√Hz at 1 kHz indicates that such a drive circuit can drive about 64 to 128 channels simultaneously.

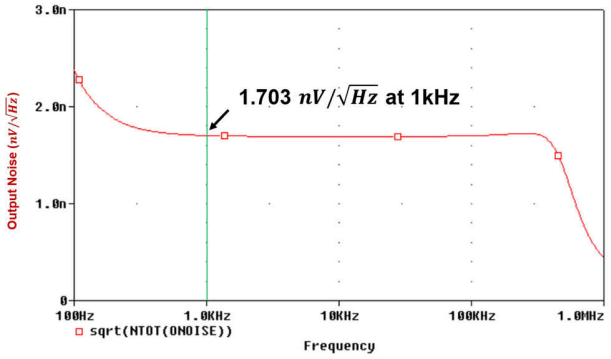

Figure 2-11. Noise Contribution of the Proposal 2 Circuit

2.3 Proposal 3: Using Low-Noise R-2R DAC (DAC81001)

2.3.1 Highlighted Products

2.3.1.1 DAC81001

The DAC81001 is a single-channel, 16-bit, voltage-output DAC. The device is specified monotonic by design, and offers excellent linearity of less than 4 LSB (max) across all ranges. The unbuffered voltage output offers low noise performance (7 nV/$\sqrt{\text{Hz}}$) in combination with a fast settling time (1 µs), making this device an excellent choice for low-noise, fast control-loop, and waveform generation applications.

2.3.1.2 OPA2210

The OPA2210 precision operational amplifier (op amp) is built on TI's precision, super-beta, complementary bipolar semiconductor process, which achieves very low-voltage noise density (2.2 nV/$\sqrt{\text{Hz}}$ at 1 kHz) with rail-to-rail output swing to maximize the dynamic range. This op amp is specified over a wide dual power-supply range of ±2.25 V to ±18 V.

2.3.1.3 THS4130

The THS4130 is a fully-differential amplifier providing very low noise (1.25 nV/$\sqrt{\text{Hz}}$) to provide maximum SNR and dynamic range. With a slew rate of 51 V/µs and gain bandwidth product of 215 MHz, the device is able to operate with a ±2.5- to ±15-V supply.

2.3.1.4 REF5010

The REF5010 is a low-noise, low-drift, very high-precision 10-V voltage reference. This reference is capable of both sinking and sourcing current and have excellent line and load regulation. The REF5010 has excellent temperature drift (3 ppm/°C) and high accuracy (0.05%). The noise is 3 μV_{PP}/V.

2.3.2 Design Circuit

This method uses a low-noise R-2R-DAC for the TGC control circuit. Figure 2-12 shows a high-level block diagram for the topology. There are two reference voltages for the DAC, V_{REF+} = 10 V, V_{REF-} = –10 V. The DAC81001 outputs are unbuffered, in such scenario, a low-noise external buffer must be used. Figure 2-13 shows the drive circuit for the control voltage.

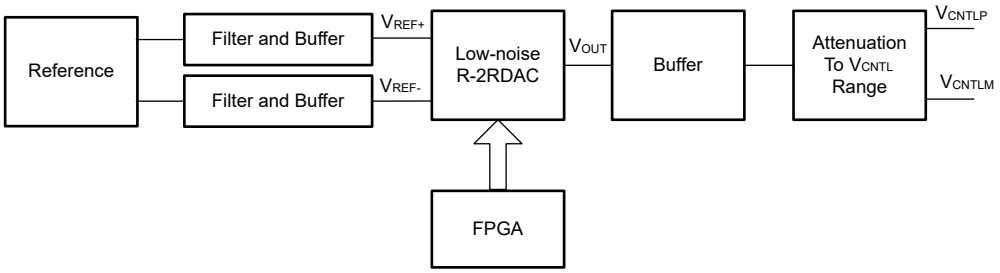

Figure 2-12. A Low-Noise R-2R DAC Used in Generating a TGC Signal

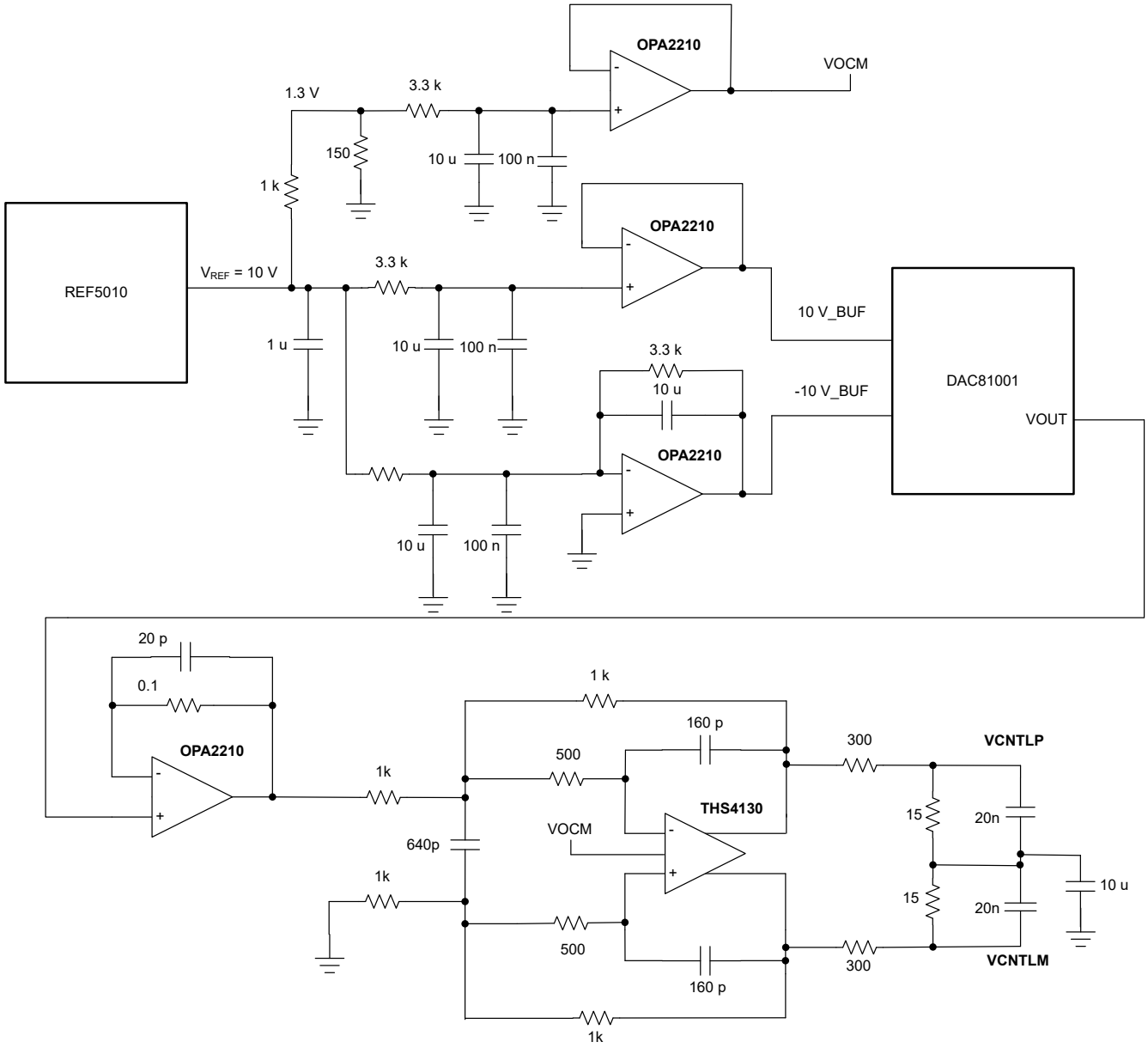

Figure 2-13. Proposal 3-V_{CNTL} Drive Circuit

2.3.3 PSpice-TI Simulation

Download the PSpice-TI simulation models for the relevant components from https://www.ti.com. Figure 2-14 shows the PSpice -TI simulation for the entire circuit.

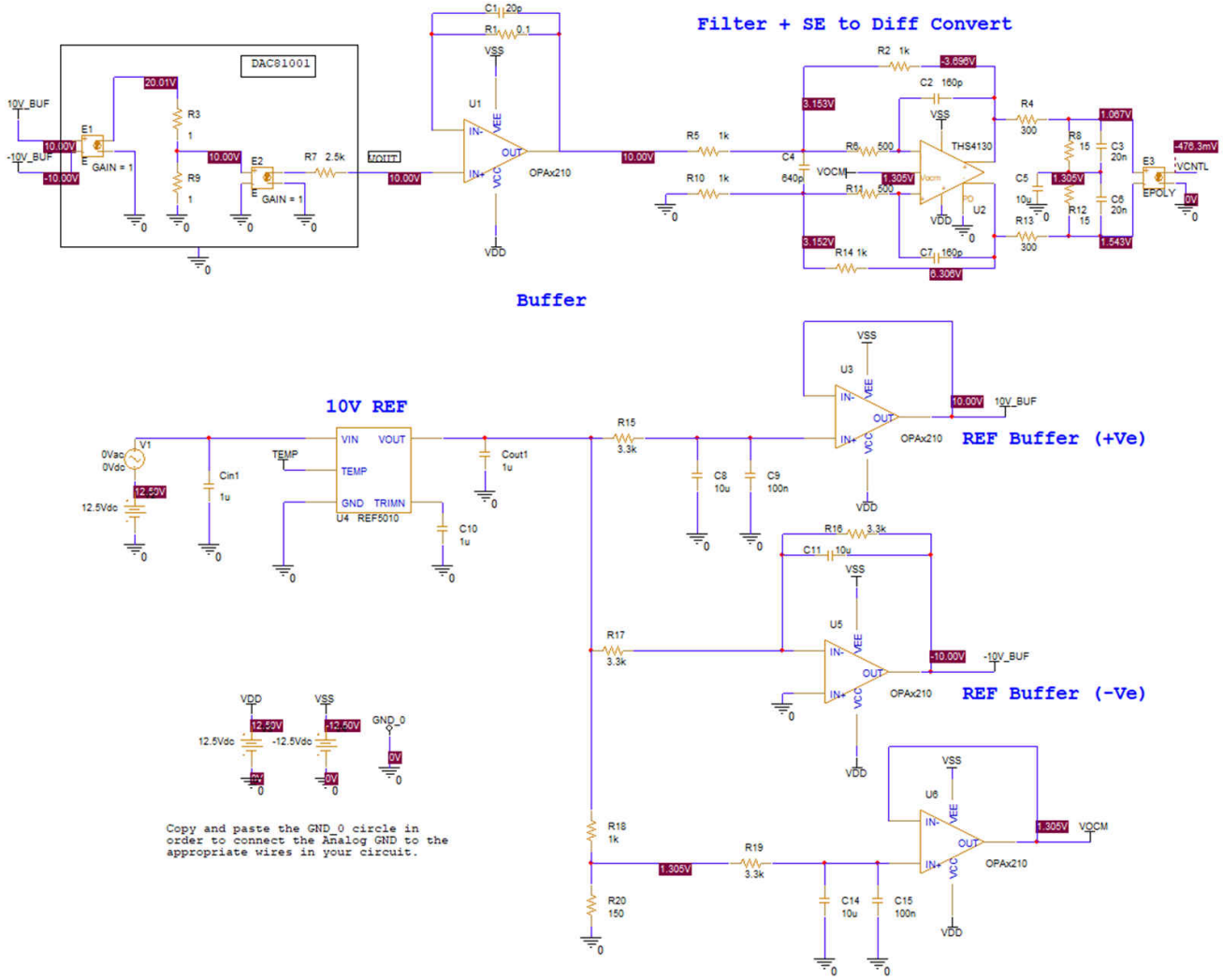

Figure 2-14. PSpice-TI Simulation of the Proposal 3-V_{CNTL} Drive Circuit

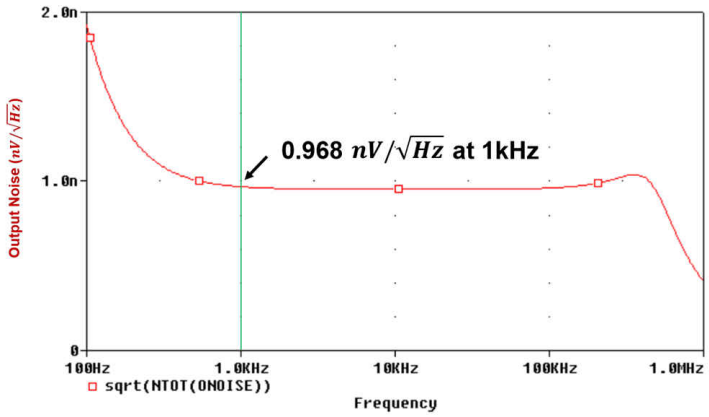

Figure 2-15. Noise Contribution of the Proposal 3 Circuit

Figure 2-15 shows the noise contribution of the circuit. The output noise of 0.968 nV/√Hz at 1 kHz indicates that such a drive circuit can drive less than 192 channels simultaneously.

3 Conclusion

This article described three approaches to design a low-noise drive circuit for the control voltage in TGC applications. For any ultrasound application, TGC is an important phenomenon. The ultrasound receive AFE includes a voltage-controlled attenuator for implementing TGC functionality that operates using a control voltage generated using external circuitry. The control voltage characteristics are used for defining the external DAC and amplifier specifications. This application notes explained the details of each approach. Table 3-1 compares each approach.

Table 3-1. Comparison of Different Approaches for TGC Circuit

Scheme	Proposal 1 (R-2R DAC)	Proposal 2 (M-DAC)	Proposal 3 (Low-noise R-2R DAC)
DAC device	DAC8830	DAC8801	DAC81001
DAC Resolution and Type	16-bit (R-2R-DAC with Unbuffered Voltage)	14-bit (M-DAC with Unbuffered Current)	16-bit (R-2R-DAC with Unbuffered Current)
DAC noise (nV/)	10	12	7
Number of op-amps	2 (OPA2210)	2 (OPA2210)	2 (OPA2210)
Number of FDAs	1 (THS4130)	1 (THS4130)	1 (THS4130)
Reference Voltage	4.096 V (REF5040)	10 V (REF5010)	10 V (REF5010)
Simulated total output noise (nV/) at 1 kHz	4.08	1.70	0.97
Power Supplies Required	• ±6 V for op-amp supplies and REF • 5 V for DAC VDD	• ±12.5 V for op-amp supplies and REF • 5 V for DAC VDD	• ±12.5V for op-amp supplies and REF • 5 V for DAC VDD
Drive channel	16	32–64	≤ 192

4 References

1. Texas Instruments, *Design and analysis of a time-gain-control (TGC) circuit to drive the control voltage for TI's ultrasound AFE* analog applications journal
2. Texas Instruments, *2.3-nV/√Hz, Differential, Time Gain Control DAC Reference Design for Ultrasound* design guide
3. Texas Instruments, *AFE58JD48 16-Channel Ultrasound AFE with 140-mW/Channel Power, 0.8-nV/√Hz Noise, 16-Bit, 125-MSPS ADC with JESD or LVDS Interface, Digital Demodulator, and Passive CW Mixer* data sheet
4. Pithadia, S., and Prakash, R., (December 2016). *Time Gain Control (Compensation) in Ultrasound Applications*. Retrieved from https://www.ti.com/lit/pdf/SLAA724

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