

Temperature Compensation of Power Amplifier FET Bias Voltages



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ABSTRACT

This application report details the basic functions and benefits of the AFE10004 in temperature-compensated voltage biasing for FETs in power amplifier (PA) applications. The report reviews the fundamentals of PA FET biasing and the need for temperature compensation. While this report focuses on the AFE10004, it is not the only device for which this principals can be applied.

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1 LDMOS and GaN Power Amplifier FET Basics

Most RF antenna systems feature power amplifiers (PA) for their transmitter design. These antenna systems include:

- Active Antenna System mMIMO (AAS)
- Macro Remote Radio Unit (RRU)
- Small Cell Base Stations
- Radar

Power amplifier biasing circuits are implemented in these systems to ensure two things: first, that the power output of the amplifier is known and controlled, and second, that the system is powered on and off safely to reduce the risk of damaging the PA. Power amplifiers are commonly created with either gallium nitride (GaN) or laterally diffused MOSFET (LDMOS) transistors. Power output in both GaN and LDMOS FETs (field-effect transistors) is dependent on the current that flows through the device from the drain to the source (I_{DS}).

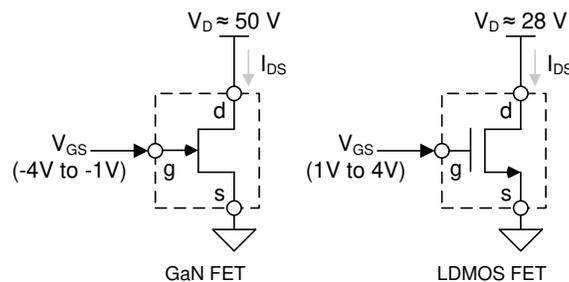


Figure 1-1. GaN and LDMOS FETs

The I_{DS} current is determined by a few variables: the drain voltage (V_D), the gate voltage (commonly called V_{GS}), and temperature. Figure 1-2 shows an example of I_{DS} values against the drain voltage for a selection of V_{GS} voltages for a GaN FET. The higher V_{GS} voltages result in a higher I_{DS} , or more power from the amplifier. When the V_{GS} voltage is sufficiently low, the FET allows virtually zero I_{DS} current. This V_{GS} voltage is called the *pinch-off* voltage. I_{DS} is also dependent on the drain voltage, but most designers do not vary the V_D . Instead, designers use optimized V_D voltages for the desired power levels. The V_D values are usually about 50 V for GaN FETs and 28 V for LDMOS FETs.

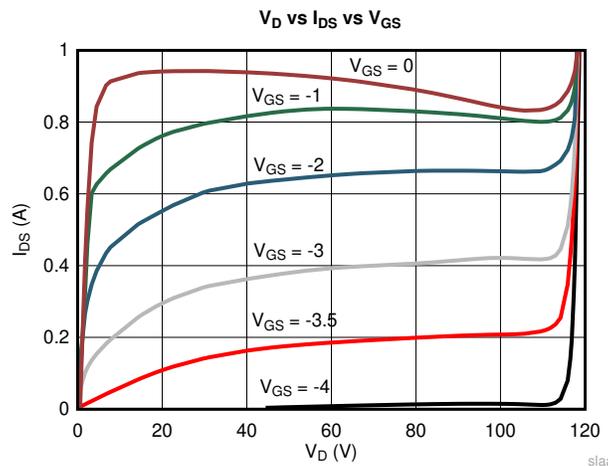


Figure 1-2. FET V_D , I_{DS} , and V_{GS} Behavior

2 V_{GS} Compensation

The I_{DS} also depends on the temperature of the FET. The I_{DS} variations due to thermal drift create the need to compensate by adjusting one of the other two variables in the system: V_D or V_{GS}. It is easier to adjust V_{GS}, as only small voltage changes are required. Conversely, V_D needs to change significantly if the device is operating in the flat areas of [Figure 1-2](#), making it infeasible to compensate for the thermal drift by adjusting V_D.

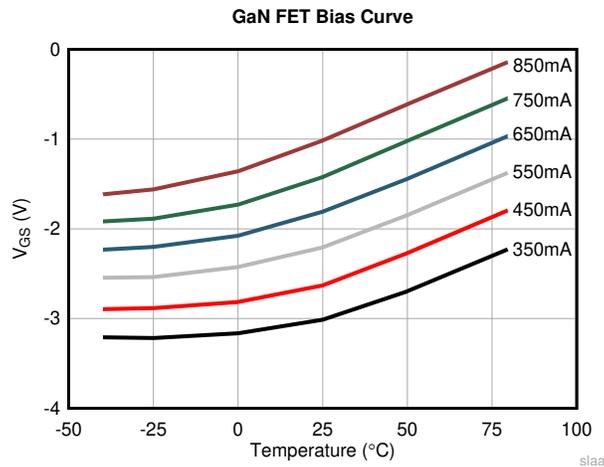


Figure 2-1. FET V_{GS} Bias Voltages

[Figure 2-1](#) shows V_{GS} needs to be adjusted to ensure a static I_{DS}. Applications utilizing these FETs require this kind of compensation to ensure that the power of the antenna system is tightly controlled. V_{GS} compensation can be implemented by either measuring the temperature of the FET, or measuring the I_{DS} using a current shunt and adjusting the V_{GS} accordingly.

3 Sequencing

Powering the FET on and off in a controlled routine is necessary to prevent the V_{GS} voltage from being too high when the V_D is applied. Such a state causes the FET to operate in saturation mode, and thermal damage the FET or board that it is mounted on. Powering on a FET requires the following steps:

1. The first signal to be applied to the FET must be V_{GS} . The V_{GS} voltage must transition to the V_{GS} pinch-off voltage or lower. This ensures that when the V_D voltage is applied, the gate is already low.
2. Next, the drain voltage supply can be enabled, allowing the V_D to be powered to the nominal value (50 V, for example). Remember that as the V_{GS} is at the pinch-off voltage, I_{DS} must be minimal.
3. Now that the V_D is applied, the V_{GS} bias voltage can be increased to set the desired power output of the PA.
4. Finally, the RF signal can be enabled. This allows the FET to transmit a signal.

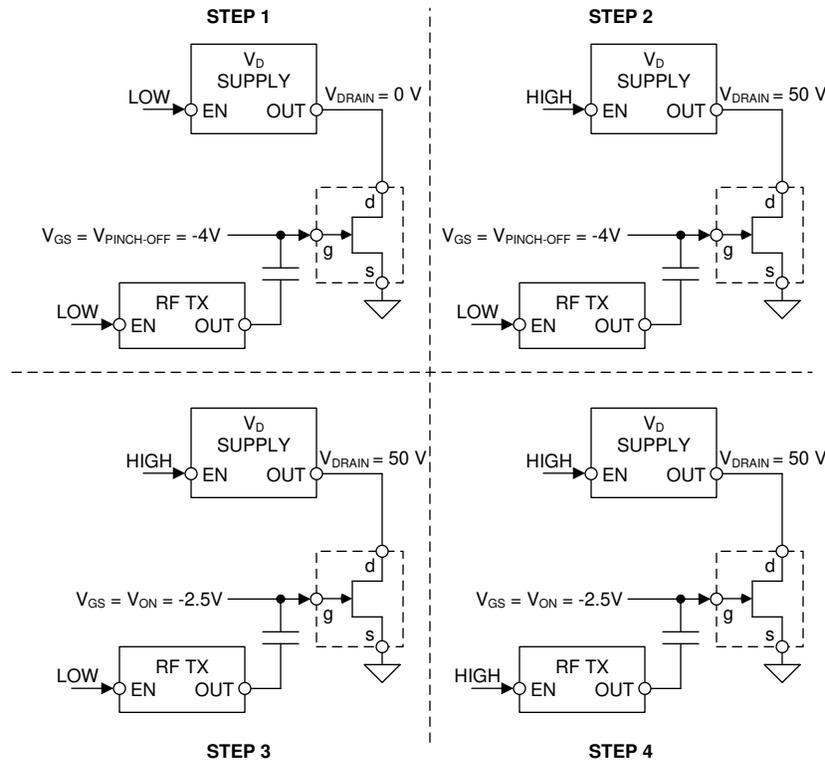


Figure 3-1. GaN Power Sequencing

The PA can be safely shut down by reversing the power-on steps.

1. Disable the RF signal from the FET.
2. Reduce the V_{GS} voltage to the pinch-off value, eliminating the power output of the FET.
3. Disable the V_D voltage by sending a disable signal to the drain supply.
4. Finally, the V_{GS} voltage can be allowed to collapse to ground as the PA is fully disabled.

4 An Integrated PA Biasing Solution

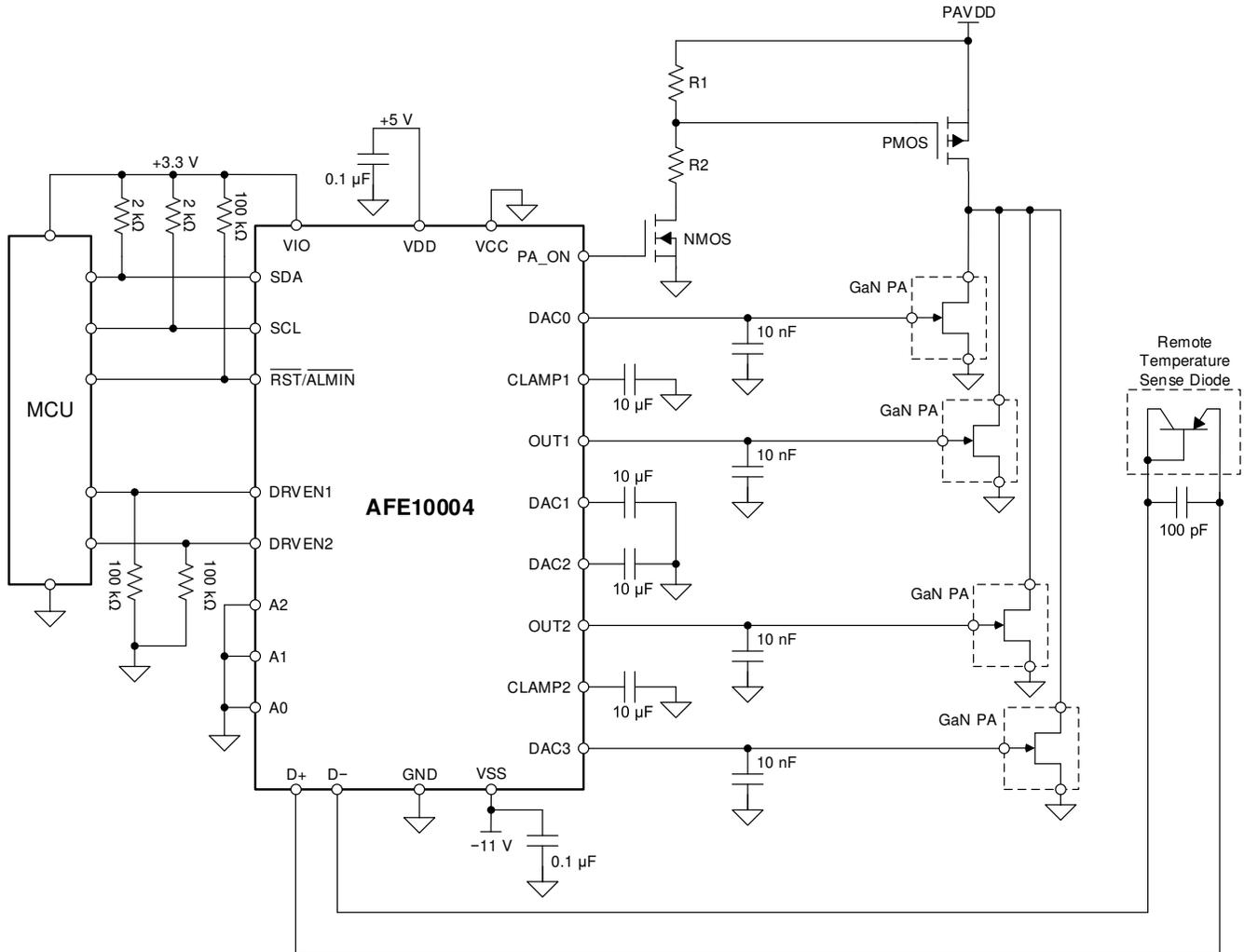


Figure 4-1. AFE10004 Typical Application

The AFE10004 is an integrated power amplifier biasing solution that integrates precision DACs with a temperature sensor to allow for closed-loop temperature compensation of four individual GaN or LDMOS FETs. The device features start-up and shutdown logic to control the input sequencing of the PA for safe power-up and power-down control. Also, it integrates low on-resistance (R_{ON}) switches to allow for fast switching between the V_{GS} -on voltage and the pinch-off voltage.

5 Temperature Compensation

The AFE10004 features non-volatile memory (NVM) that can be programmed with the V_{GS} compensation curve look-up table (LUT) for the application-specific PA. The device automatically enters a closed-loop operation, in which it monitors the operating temperature using local or remote temperature sensors and adjust V_{GS} to maintain a constant power level. Each of the four output channels has independent LUTs, allowing for different FETs to be used in with a single AFE10004.

6 Fast Output Switching

The AFE10004 uses two separate DAC channels to create the two critical bias voltages for the FET: the temperature compensated V_{GS-ON} voltage and the programmable, yet static, V_{GS} pinch-off voltage. These are the DAC output and the CLAMP output, respectively. The gate of the FET is connected to a common node (OUT) that can be connected to either of the outputs through low R_{ON} switches. The outputs use external capacitors to quickly charge the common node to the desired voltage, rather than be limited to the current output and slew-rate of precision DACs, to switch the output voltage directly. The fast switching between the two voltages allows the PA to be turned on and off quickly, enabling burst transmission of the RF signal while reducing total power consumption.

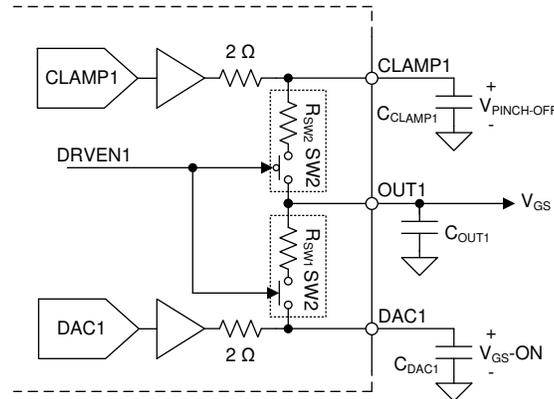


Figure 6-1. AFE10004 Output Switches

7 Controlled Sequencing With the AFE10004

The power sequencing requirements of the PA are maintained by the AFE10004 at start-up. Consider [Figure 7-1](#): as the AFE10004 supplies ramp to normal operating value, the V_{GS} bias (OUT) is connected to the CLAMP output, which tracks the negative supply, VSS. After the supplies are established, the CLAMP and DAC output load the initial values from the LUT. The OUT pin is still connected to the CLAMP value, which has now assumed the pinch-off voltage (step 1 in [Figure 3-1](#)). Once the device has loaded the LUT for the outputs from memory, the AFE10004 releases the PA enable signal, which is used to enable the V_D supply (step 2). Next, the externally generated drive enable (DRVEN) input switches the OUT pin from the CLAMP output to the DAC output, which is now the temperature compensated V_{GS} voltage (step 3). The RF signal can now be applied to the FET (step 4).

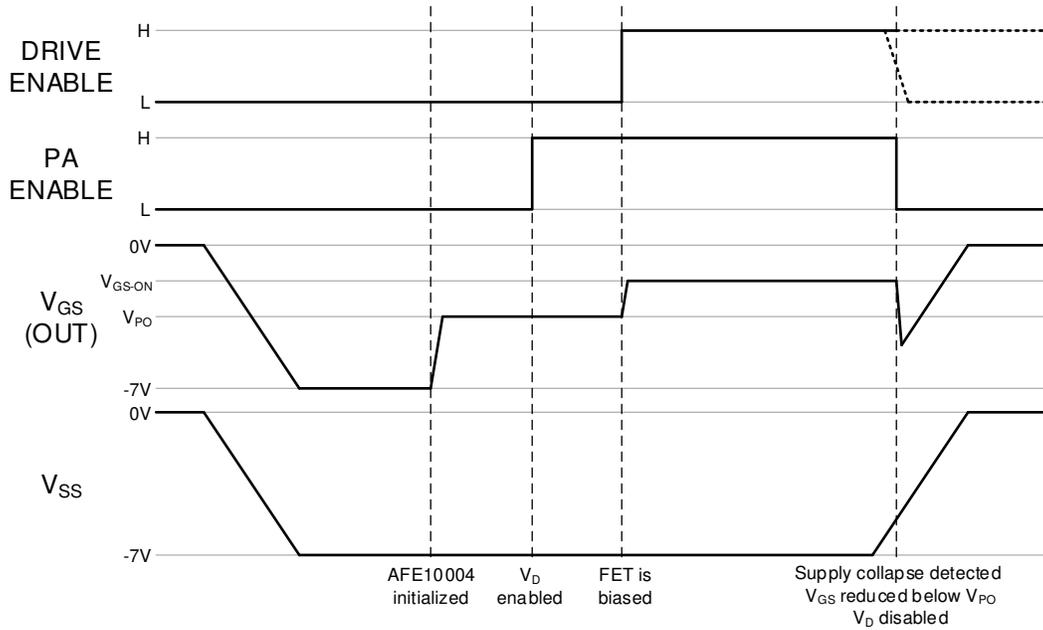


Figure 7-1. AFE10004 Power Sequence Control

The AFE10004 controls the sequence during power down. When the device receives an alarm input or detects a supply collapse, it connects the OUT pin to the CLAMP output, which brings the V_{GS} to the pinch-off voltage (power down step 2; note that step 1 is controlled by the RF source). Next, the PA enable signal becomes low, which disables the V_D supply. Finally, the OUT value tracks the VSS supply until it collapses to ground.

8 Conclusion

Power amplifier behavioral nuances make discrete V_{GS} compensation solutions complex and costly. The AFE10004 simplifies the solution while adding beneficial features, such as fast output switching, to make the device an excellent value. The device is offered in a compact 4 mm × 4 mm package, which reduces solution space considerably.

Table 8-1. Alternative Device Recommendations

Device	Optimized Parameters
LMP92066	Dual temperature-controlled DAC with EEPROM and output switching in 5-mm × 4.4-mm TSSOP package
AMC7836	16 bipolar 12-bit DACs with 21 12-bit ADC inputs, integrated temperature sensor in a 10-mm × 10-mm QFP package
AMC7834	4 bipolar 12-bit DACs, 4 12-bit ADC inputs, integrated temperature sensor and current shunt monitor in 8-mm × 8-mm QFN package

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