Application Report
SLAA893–April 2019

TMDS181 Schematic Checklist

ABSTRACT

This schematic checklist provides a brief explanation of each TMDS181 device pin and the recommended configuration of TMDS181 device pins for default operation. The TMDS181 is a digital video interface (DVI) or high-definition multimedia interface (HDMI) retimer. The TMDS181 supports four TMDS channels, audio return channel (SPDIF_IN/ARC_OUT), and digital display control (DDC) interfaces. The TMDS181 has the ability to be configured via pin strap or I2C. Use this information to check the connectivity for each TMDS181 device on a system schematic.

This document is intended to aid design at the system level for general applications but must not be the only resource used. In addition to this list, use the information from the TMDS181x 6 Gbps TMDS Retimer Data Sheet, TMDS181RGZ Evaluation Module User's Guide, and associated documents to gain a full understanding of device functionality.

Contents

List of Figures

List of Tables

Trademarks

1 TMDS181 Schematic Checklist

Table 1. TMDS181 Schematic Checklist for Default Operation

PIN NAME	PIN NUMBER(S)	PIN DESCRIPTION	RECOMMENDATION	ADDITIONAL COMMENT
MAIN LINK INPUT PINS				
IN_D[0:2]p/n	8, 9, 5, 6, 2, 3	Main link differential input	Direct connection from connector/GPU to TMDS181	
IN_CLKp/n	11, 12	Main link clock differential input	Direct connection from connector/GPU to TMDS181	

Table 1. TMDS181 Schematic Checklist for Default Operation (continued)

PIN NAME	PIN NUMBER(S)	PIN DESCRIPTION	RECOMMENDATION	ADDITIONAL COMMENT
MAIN LINK OUTPUT PINS				
OUT_D[0:2]p/n	28, 29, 31, 32, 34, 35	TMDS data differential output	Direct connection from TMDS181 to connector/receiver	Output can be AC-coupled, but require external termination network, see Figure 1. TMDS181 output amplitude needs to be increased to compensate for the double termination.
OUT_CLKp/n	26, 25	TMDS clock differential output	Direct connection from TMDS181 to connector/receiver	Output can be AC-coupled, but require external termination network, see Figure 1. TMDS181 output amplitude needs to be increased to compensate for the double termination.
DDC PINS				
SDA_SRC	47	Source side TMDS bidirectional DDC data line	Snoop mode, tie it to GND	
SCL_SRC	46	Source side TMDS bidirectional DDC clock line	Snoop mode, tie it to GND	
SDA_SNK	39	Sink side TMDS bidirectional DDC data line	SDA/SCL from the source is connected directly to theSDA/SCL sink. The TMDS181 will need its SDA_SNK and SCL_SNK pins connected to this link in order to correctly configure the TMDS_CLOCK_RATIO_STATUS bit.Sink application: 47k pull-ups to 5V Source application: 2k pull-ups to 5V	Consider adding an external I2C buffer for DDC capacitance isolation
SCL_SNK	38	Sink side TMDS bidirectional DDC clock line	SDA/SCL from the source is connected directly to theSDA/SCL sink. The TMDS181 will need its SDA_SNK and SCL_SNK pins connected to this link in order to correctly configure the TMDS_CLOCK_RATIO_STATUS bit.Sink application: 47k pull-ups to 5V Source application: 2k pull-ups to 5V	Consider adding an external I2C buffer for DDC capacitance isolation

Table 1. TMDS181 Schematic Checklist for Default Operation (continued)

PIN NAME	PIN NUMBER(S)	PIN DESCRIPTION	RECOMMENDATION	ADDITIONAL COMMENT
HOT PLUG DETECT PINS				
HPD_SNK	33	Hot plug detect input from sink side	Connect to HPD output for the display and connector. For snoop mode: Connect directly to Sink's/GPU's(Check GPU supported voltage) directly connected HPD line HPD_SNK has internal 190 k pull-down.	Consider adding an external switch to isolate potential leakage voltage from sink HPD when sink is off
HPD_SRC	4	Hot plug detect output to source side	If HPD_SRC goes to the source connector a level shifter from 3.3 V to 5 V is needed. If HPD_SRC goes to GPU, check supported GPU voltages. If HPD snoop mode is implemented, leave HPD_SRC floated.	
AUDIO RETURN CHANNEL PINS				
SPDIF_IN	45	SPDIF signal input	If not needed: 500 k pull-down. Implementation dependent, see Figure 2 SPDIF_IN -> HDMI sink SPDIF_IN_2 -> TMDS181	
ARC_OUT	44	Audio return channel output	if not needed: NC Implementation dependent,see Figure 2	
CONTROL PINS				
OE	42	Enable/reset pin	Start with 0.2uF, tune depending on the RC time constant delay (Tr) requirement in regard to power ramp up time	See Table 2 for different timing values based on capacitance.
Vsadj	22	TMDS-compliant voltage swing control resistor	Start with 7.06 k resistor to ground, resistor value tuning depends on compliance result	
SCL_CTL	15	I2C clock signal	2 k pull-ups to 3.3 V or value required by I2C master	
SDA_CTL	16	I2C data signal	2 k pull-ups to 3.3 V or value required by I2C maste	
I2C_EN/PIN	10	I2C control mode	65 k pull-down for pin strap mode 65 k pull-up for I2C mode	
EQ_SEL/A0	21	Input receive equalization	NC for adaptive EQ in pin strap mode	65 k pull-up or pull-down in I2C mode
A1	27	Input receive equalization	NC in pin strap mode	65 k pull-up or pull-down in I2C mode
SIG_EN	17	High address I2C bit for I2C programming	65 k pull-down or pullup to enable/disable signal detector	Recommend 65 k pull-down to disable signal detect circuit

Table 1. TMDS181 Schematic Checklist for Default Operation (continued)

PIN NAME	PIN NUMBER(S)	PIN DESCRIPTION	RECOMMENDATION	ADDITIONAL COMMENT
PRE_SEL	20	Signal detector circuit enable	PRE_SEL = L: -2dB PRE_SEL = NC: 0dB PRE_SEL = H: Reserved	Leave it floating when I2C_EN/PIN = high, control through I2C
TX_TERM_CTL	36	Transmit termination control	NC for automatic Tx termination	
SWAP/POL	1	Input lane SWAP and polarity control	Default NC, 65 k pull-up or pull-down if needed	
POWER PINS				
VCC	13, 43	3.3 V power supply	One 100 nF cap on each power pin. 4.7 pF and 10 pF on each power node. One bulky cap per power node	
VDD	12, 23, 24, 37, 48	1.1 V power supply	One 100nF cap on each power pin. 4.7pF and 10pF on each power node. One bulky cap per power node	
	7, 19 ,41, 30	Ground	Connect to board ground	
Thermal Pad	49	Ground	Connect to board ground	

Table 2. Enable (OE) Pin Timing Based on Capacitance

RISE TIME (T_r) (ms)	CAPACITOR VALUE (µF)
25	0.1
50	0.2
100	0.4
200	0.8
500	2

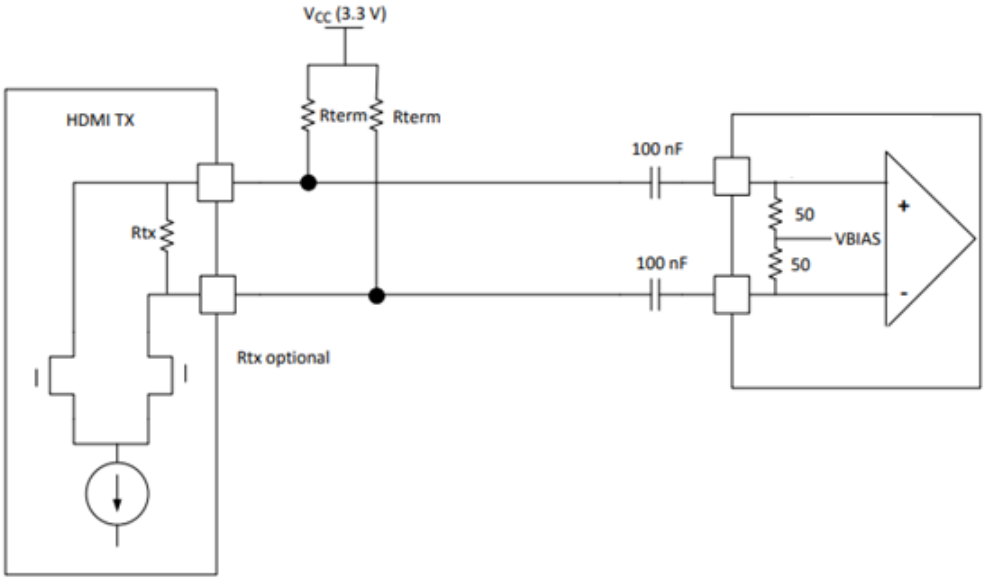

Figure 1. External Termination Network for AC-coupled Interface

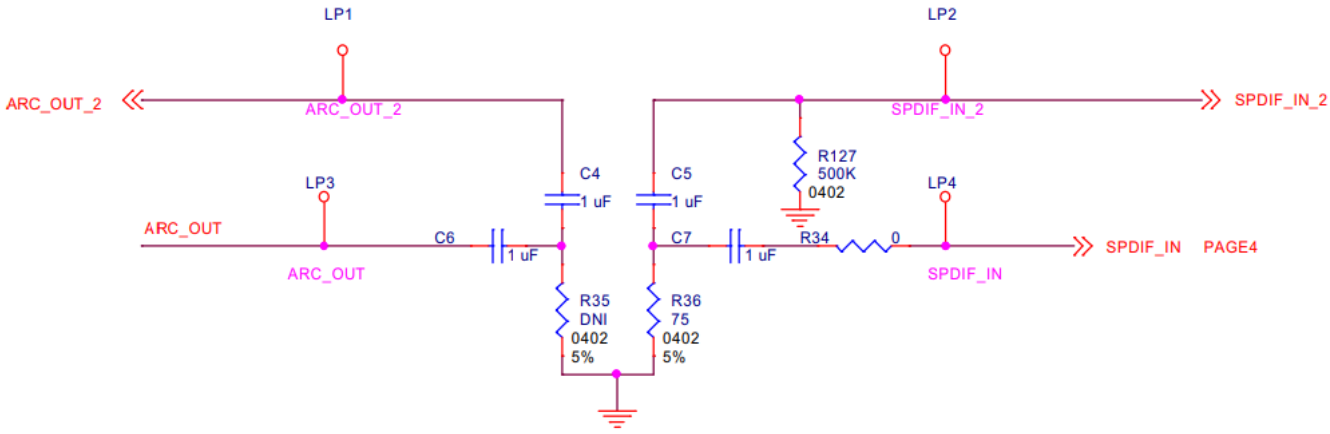

Figure 2. Audio Channel Implementation

2 References

- *TMDS181x 6 Gbps TMDS Retimer Data Sheet*
- *TMDS181RGZ Evaluation Module User's Guide*

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