Application Report

TAS2764 Schematic and Layout Guidelines

ABSTRACT

In audio applications, it is always important to minimize the noise effects that may be induced by external conditions or even by the same components of the PCB. All the audio amplifiers require a clean and stable power supply to get the best performance. Any noise issue at the power supplies may be the cause of a high THD+N and SNR levels. In addition, the analog inputs and outputs require good noise immunity against the digital activity from nearby devices.

This document describes an optimized layout for the TAS2764 device in mono and stereo configuration. The goal of utilizing these layout guidelines is to minimize the noise issues and ensure the best device performance. The TAS2764EVM was taken as reference for the suggested guidelines.

Table of Contents

Trademarks

1 Mono Version

1.1 TAS2764 Typical Application Circuit

TAS2764 Block Diagram shows the typical application block diagram for the mono TAS2764 device.

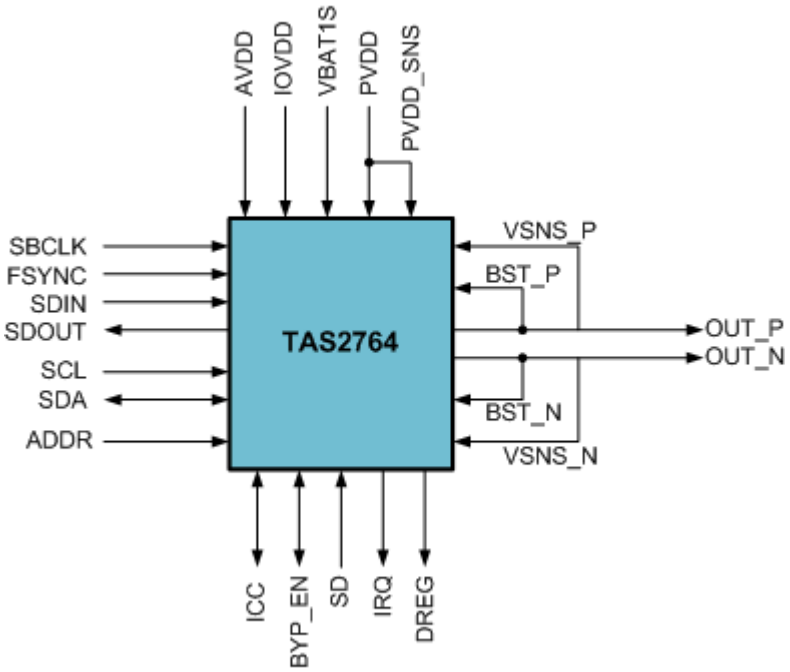

Figure 1-1. TAS2764 Block Diagram

TAS2764 Components Location and TAS2764 Components Location (3D View) show the components location of the PCBA reference layout.

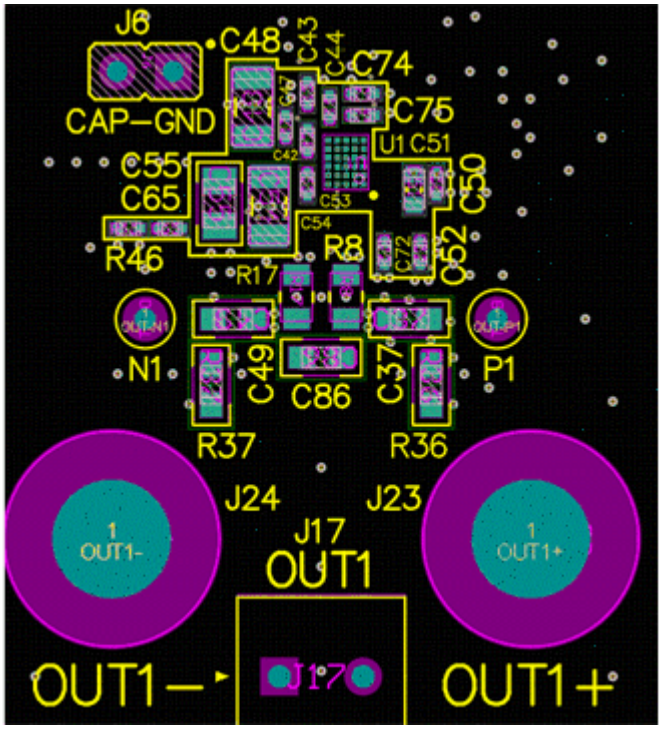

Figure 1-2. TAS2764 Components Location

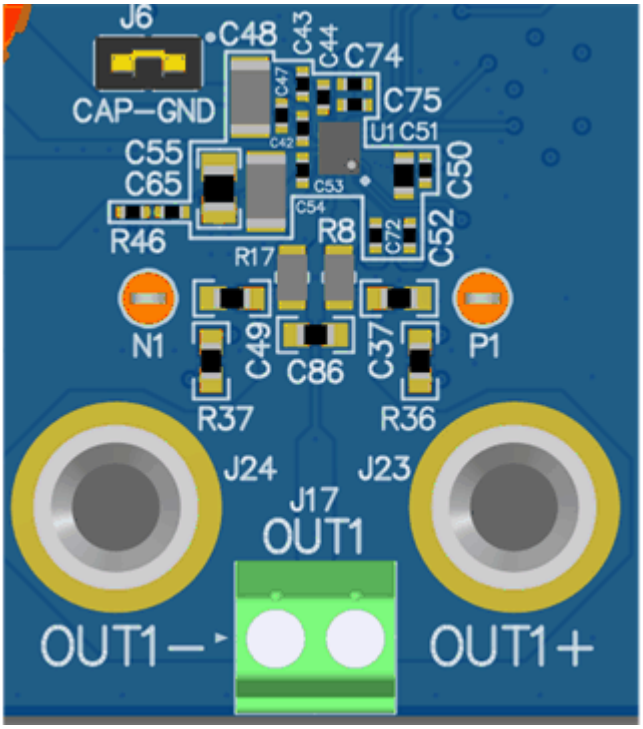

Figure 1-3. TAS2764 Components Location (3D View)

Layout Line Color Codes In This Document lustrates the colors used for all the layout lines in this document.

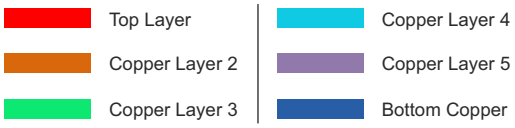

Figure 1-4. Layout Line Color Codes In This Document

1.2 VBAT1S

VBAT1S is the battery power supply input. Since it carries a considerable amount of current, a decoupling capacitor is required. At least a 0.1 uF capacitor must be used to bypass VBAT1S to GND. See Decoupling Capacitors section for details.

An additional 10 uF capacitor if VBAT1S is externally supplied or an additional 1uF capacitor if VBAT1S is internally generated.

It is important to consider the following recommendations for VBAT1S:

- Include the additional capacitors previously mentioned to reduce the overall THD+N at high power.
- Have the VBAT1S traces wide enough to handle the total output power.
- Do not use vias between device pins and related capacitors.

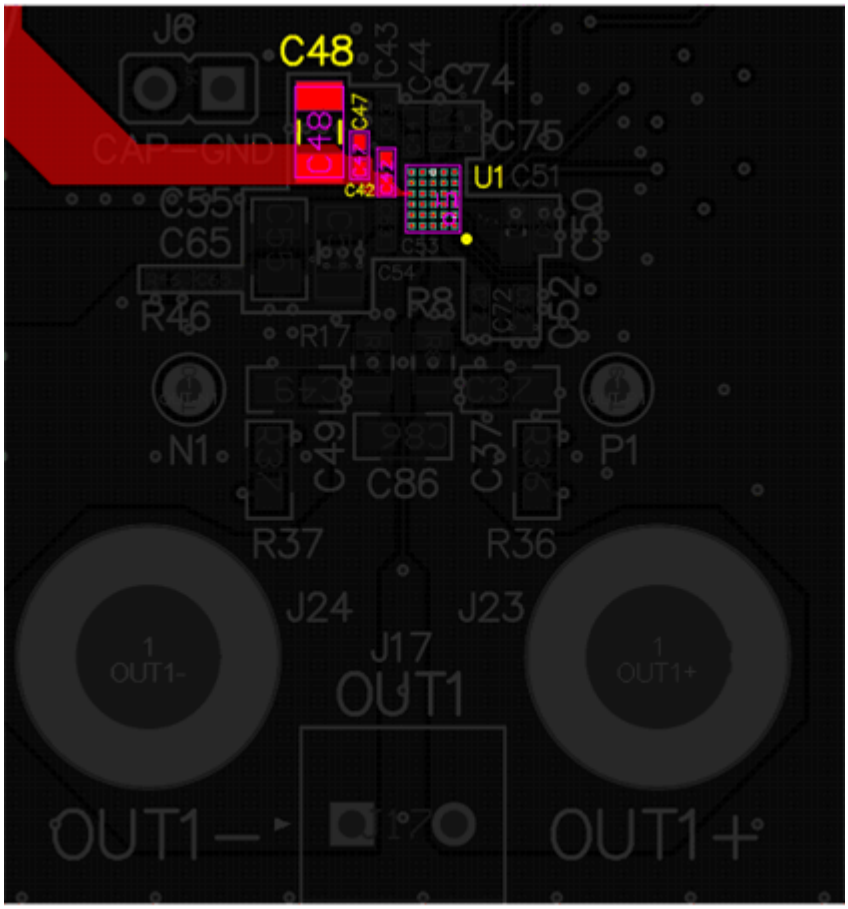

Figure 1-5. VBAT1S Pin Connection

1.3 DREG

DREG is the digital core voltage regulator output. This pin must be bypassed to GND with a 1 µF capacitor and it must not be connected to an external load. TI recommends ensuring that both decoupling capacitor ends see as low inductance as possible between this DREG pin and GND. Multiple vias are suggested to reduce the inductance.

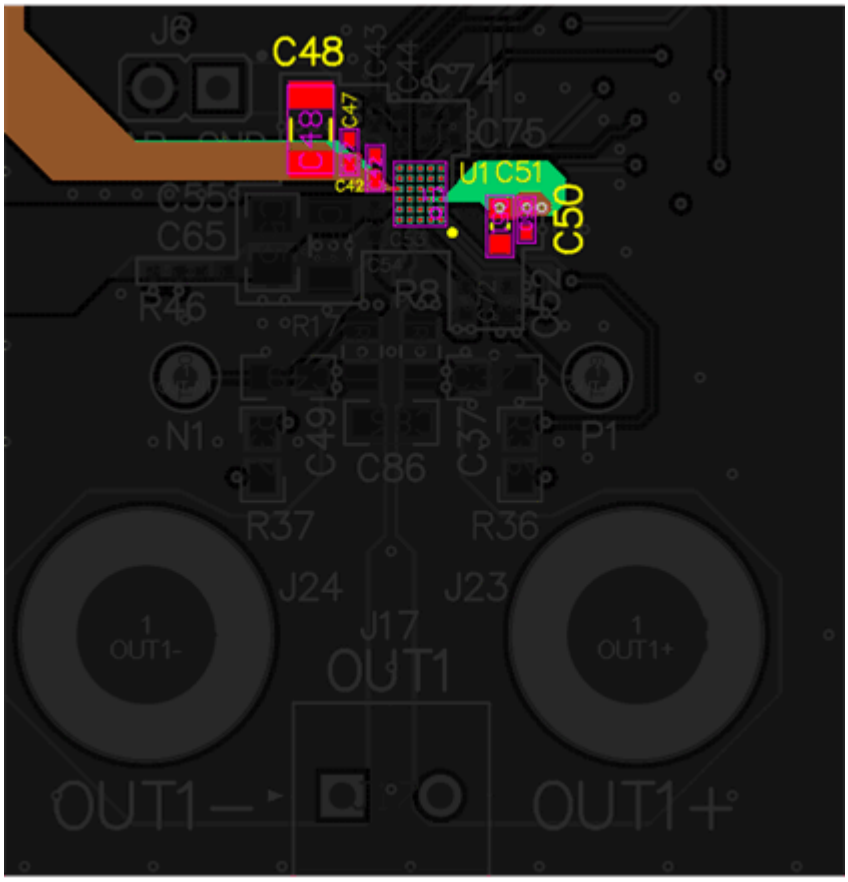

Figure 1-6. DREG Pin Connection

1.4 PVDD

PVDD is the power stage supply pin of the TAS2764. There are a few considerations that must be taken into account for the PVDD connection.

- PVDD traces carry a high amount of current. The traces should support currents up to the device overcurrent limit.
- The power supply should be connected to PVDD through a thick plane.
- PVDD pin must be bypassed to PGND with a decoupling capacitor. At least a 10 µF and a 0.1 uF decoupling capacitors must be connected to the PVDD pin.
- The decoupling capacitor ends should see as low an inductance as possible between the PVDD pin and the PGND pin. It is suggested to add multiple vias to reduce parasitic inductance.

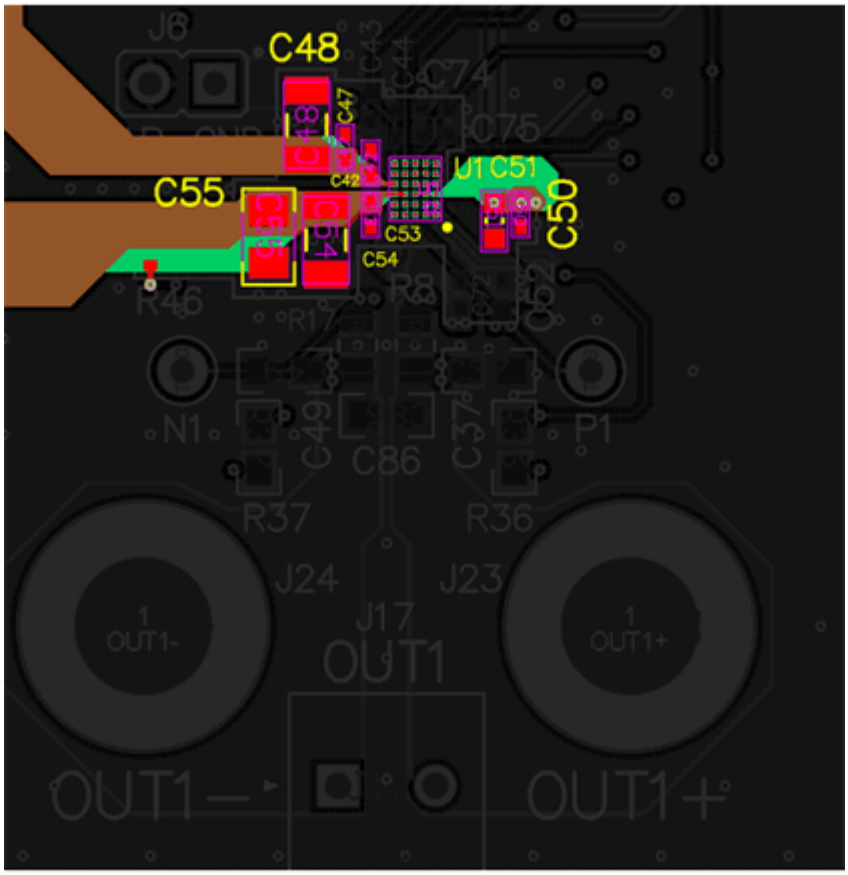

Figure 1-7. PVDD Pin Connection

1.5 AVDD

AVDD is the analog power input. Similar to VBAT1S and PVDD, this pin requires a decoupling capacitor. A minimum 4.7 µF capacitor is suggested to bypass AVDD to GND. See Decoupling Capacitors section for details.

Similar to the decoupling capacitors recommendations, it should be placed as close as possible to the AVDD pin.

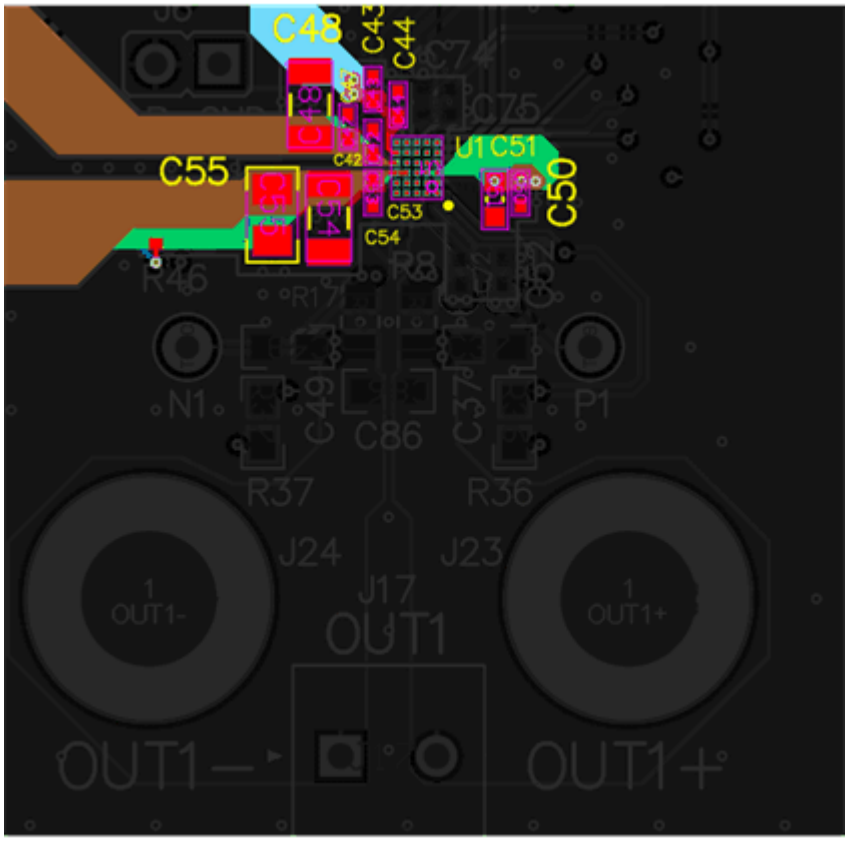

Figure 1-8. AVDD Pin Connection

1.6 IOVDD

IOVDD is the digital I/O supply. This power pin also requires of a decoupling capacitor. A minimum 1 µF is suggested to bypass IOVDD to GND. The capacitor should be placed as close as possible to the IOVDD pin.

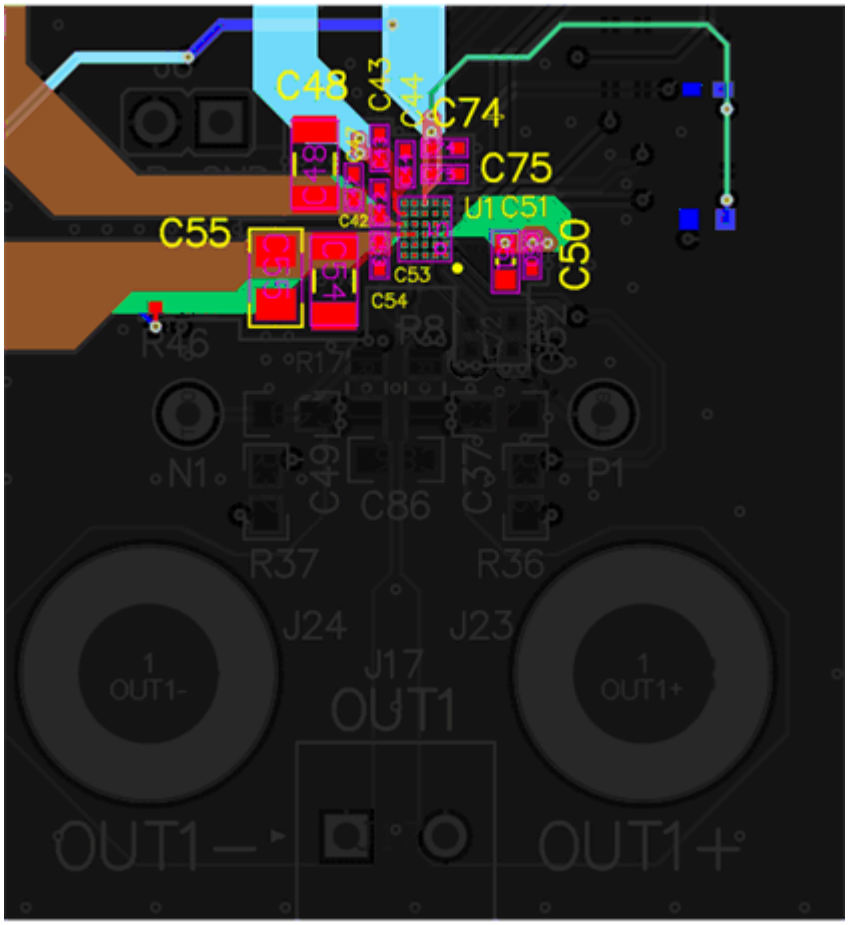

Figure 1-9. IOVDD Pin Connection

1.7 Output Pins

OUT_N and OUT_P are the Class-D receiver channel negative and positive output, respectively. Due to its switching nature, TI recommends keeping the routing short to limit the emissions.

For optimal current flow, the PCB traces must be widened near to the output pins. In addition, the outputs need to be routed on two layers using several vias to minimize parasitic impedance.

It is important to consider a few things when using an EMI filter (LC array):

- Inductance should be the first element in the filter.
- Capacitance to GND or other output will pull high-current spikes capable of triggering overcurrent protection.
- TI recommends fixing 1.5 MHz as the lower limit of the corner frequency to simplify the filter debug and noise issues.

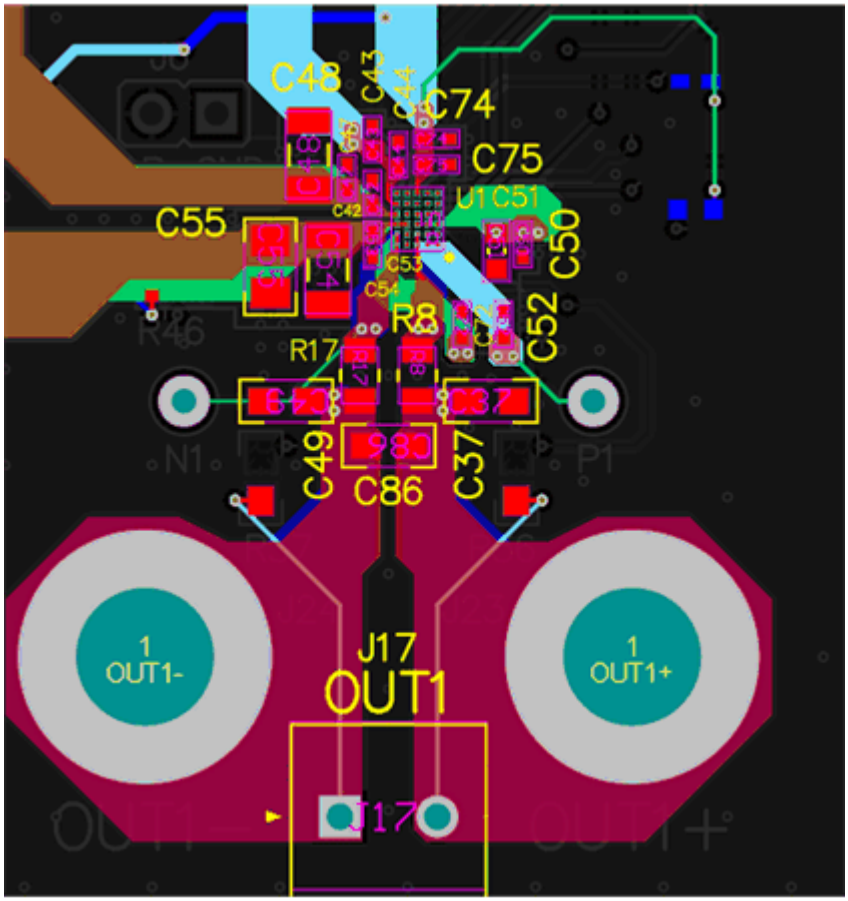

Figure 1-10. OUT_P, OUT_N, BST_P and BST_N Pins Connections

1.8 Sense Pins

VSNS_N and VSNS_P are the voltage sense negative and positive inputs, respectively. These inputs are connected to the Class-D outputs (VSNS_N to OUT_N and VSNS_P to OUT_P) after the ferrite bead filter.

When routing these pins to the ferrite bead filter, it is necessary to the make the connection to its respective output at the speaker terminal, not to a pin or trace. In addition, TI recommends adding a 1 kΩ resistor for each voltage sense path. This practice helps to reduce emissions and reduce ICN increments that result from the EMI filter.

PVDD_SNS pin is the PVDD voltage sense input pin. This input is connected to the PVDD source, not to a pin or trace.TI recommends adding a 1kΩ resistor for the PVDD sense path.

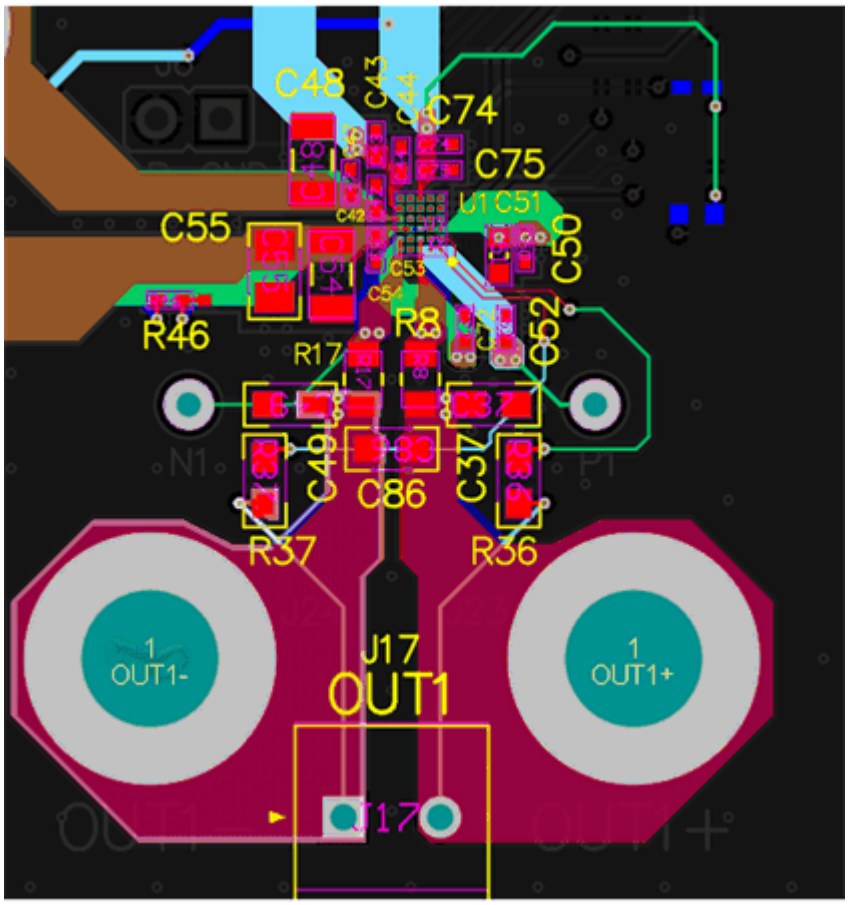

Figure 1-11. VSNS_P, VSNS_N and PVDD_SNS Pins Connections

1.9 Digital Portion

The TAS2764 device involves digital and analog activity. Care must be taken when routing the different signals since it may result in noise issues, especially from the digital lines to the analog portion.

The digital lines can reach frequencies up to 1 MHz for the I2C lines in Fast-Mode Plus and up to 50 MHz for the I2S lines. This high-frequency content can affect the performance of the analog signals. For measurement purposes, the digital noise level may affect the scope captures or a THD+N measurement.

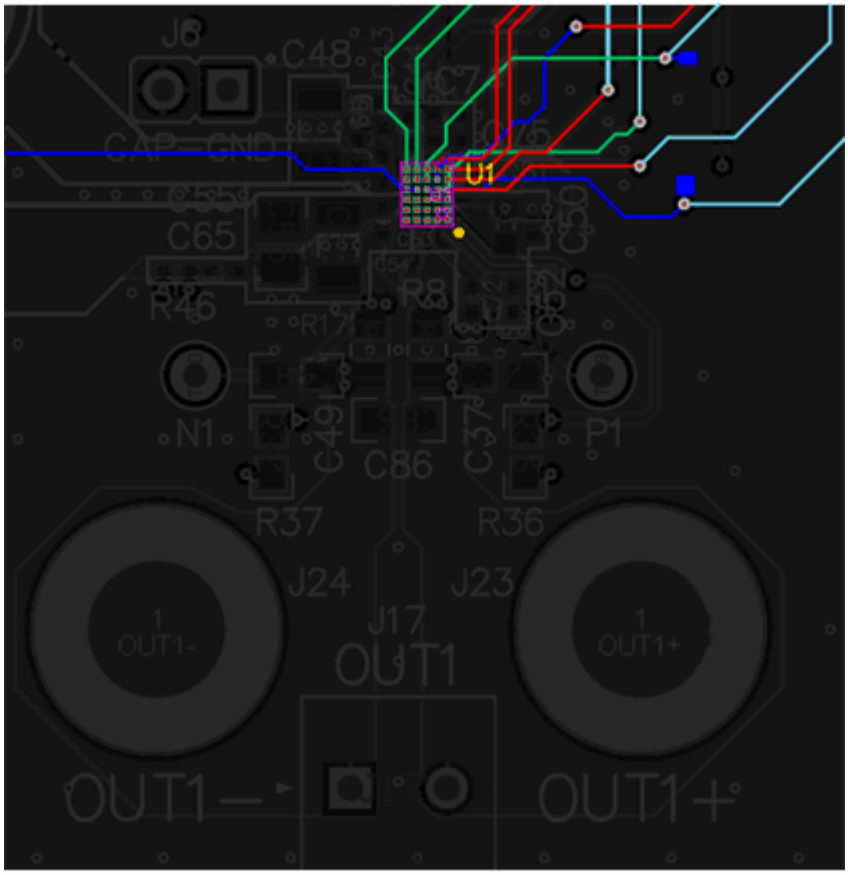

Figure 1-12. Digital Pins Connections

1.10 Ground Planes

The ground plane routing is important when designing the PCB layout. These planes must be designed to have a proper thermal dissipation and minimize the parasitic impedance as much as possible. Design tips for the different ground pins are listed here:

- All the ground pins must be shorted below the package and connected to the PCB ground plane through multiple vias.
- The vias are the best way to carry heat from the different sections in the board. Since the GND plane will need to quickly dissipate all the elevated temperatures, it is necessary to add multiple vias close to the ground pins.
- Having many vias reduces the additional parasitic impedance and provides good conduction in both electrical and thermal perspective.
- An entire layer immediately below the top layer must be dedicated to GND, as best practice.

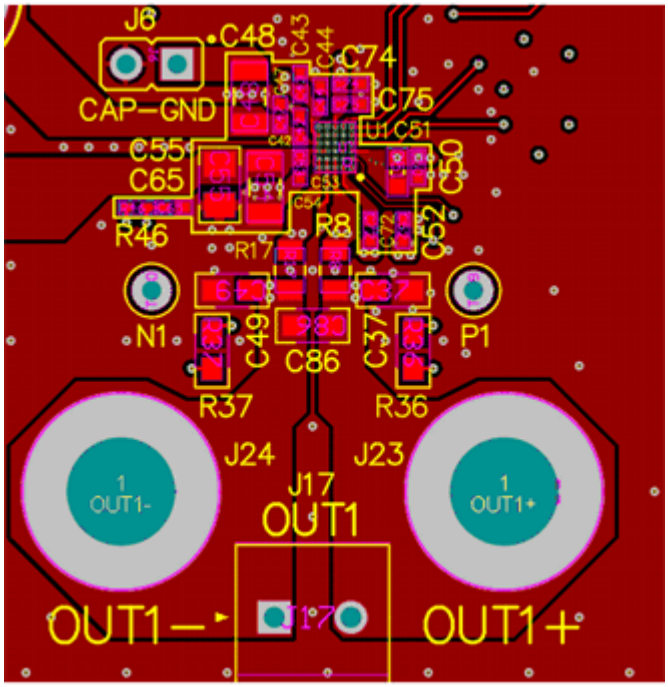

Figure 1-13. TAS2764 Top Layer

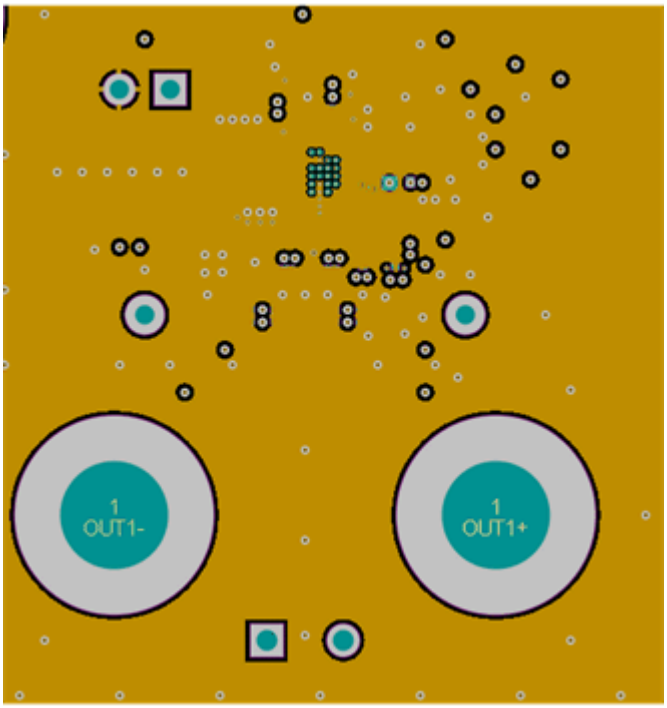

Figure 1-14. TAS2764 Signal Layer 2

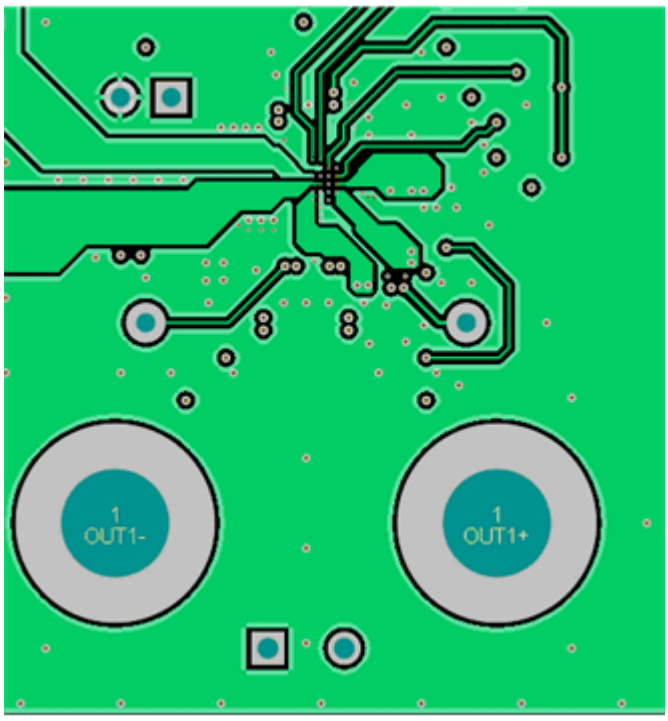

Figure 1-15. TAS2764 Signal Layer 3

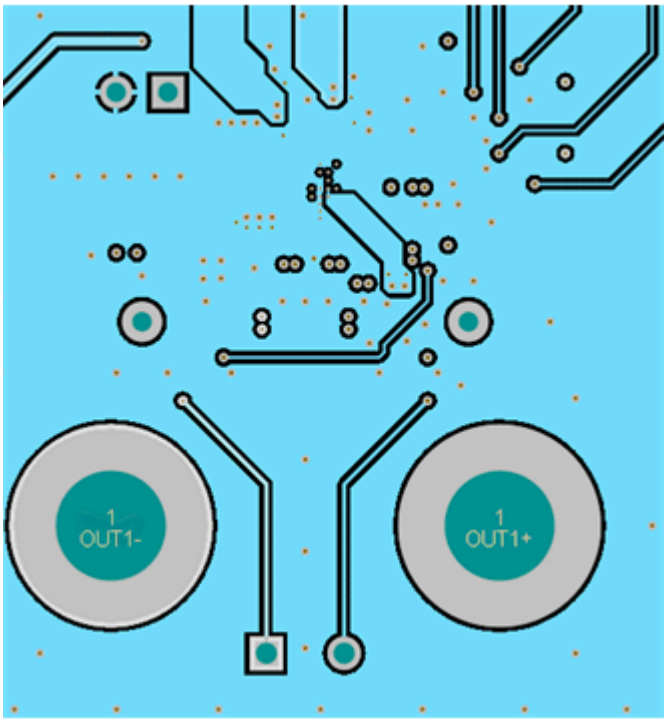

Figure 1-16. TAS2764 Signal Layer 4

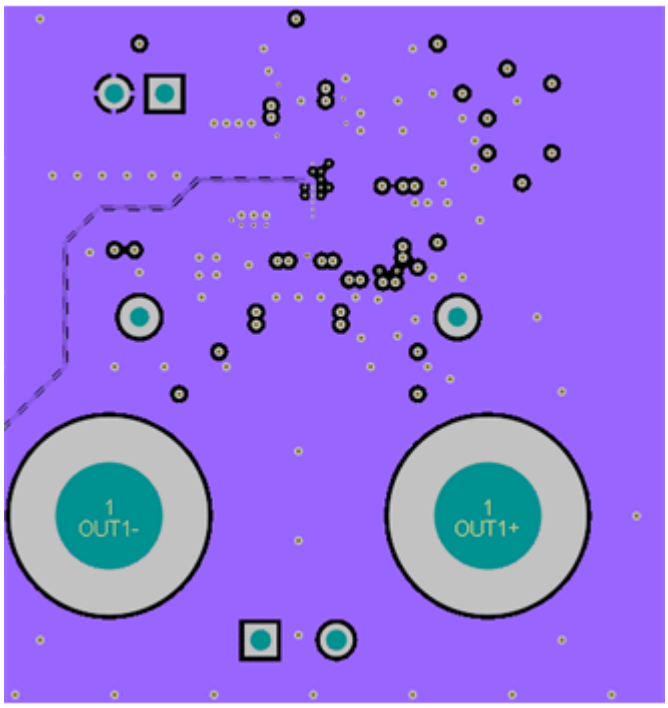

Figure 1-17. TAS2764 Signal Layer 5

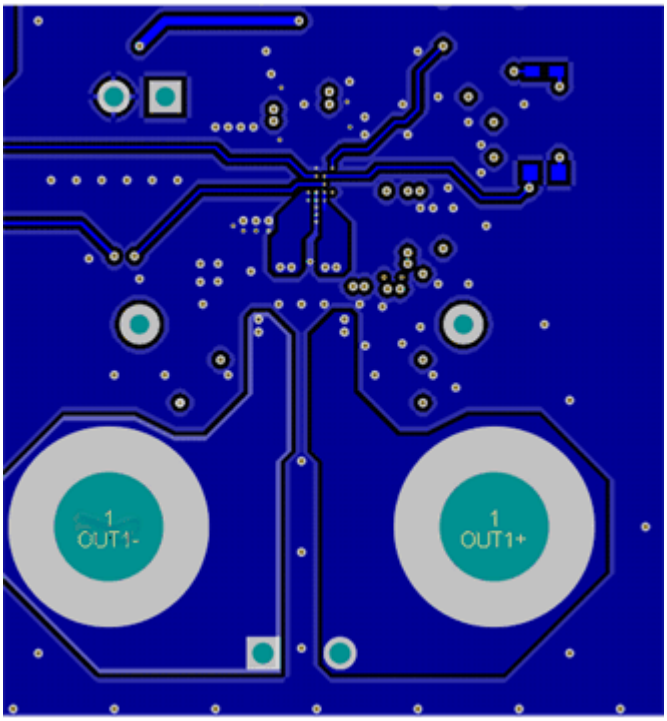

Figure 1-18. TAS2764 Bottom Layer

2 Stereo Version

2.1 TAS2764 Typical Application Circuit (Stereo)

TAS2764 Block Diagram (Stereo) shows the typical application block diagram for a stereo TAS2764 device. Notice the devices share some of the signals like digital interface 1 (ASI1) and I2C control. Optionally, both devices can share the power supplies, IRQ and SD if required. The designer must consider that each device has VSNS signals connected as close as possible to its respective speaker

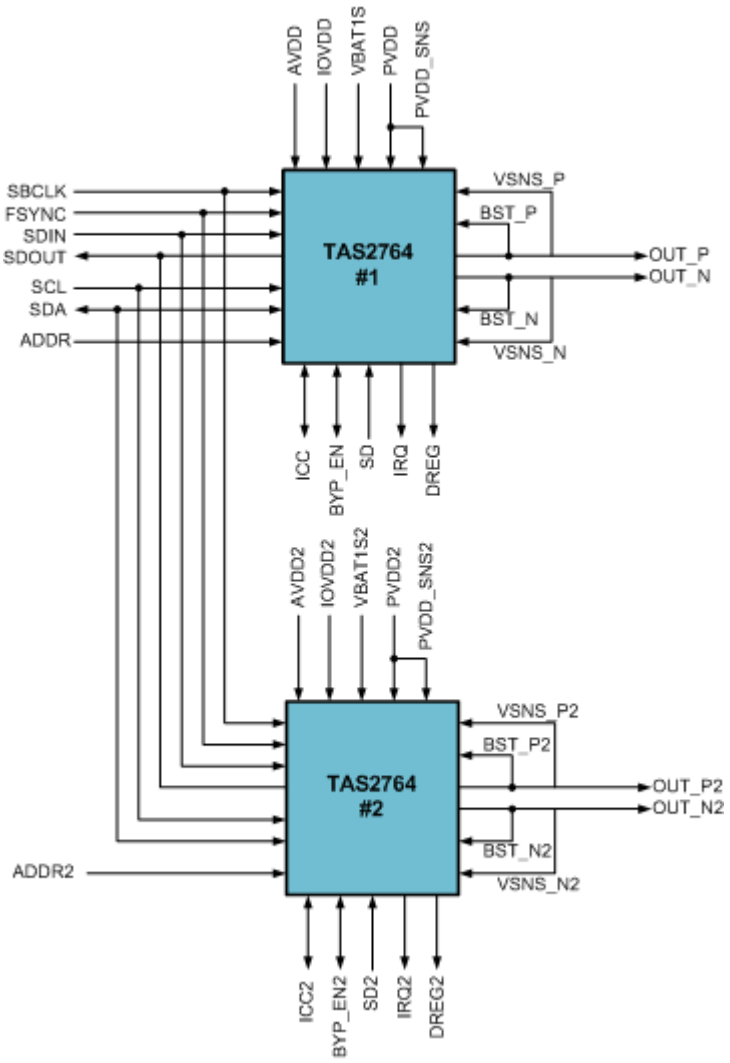

Figure 2-1. TAS2764 Block Diagram (Stereo)

2.2 Layout Guidelines

TAS2764 mono and stereo connections share the same design rules. Refer to Mono Version section for details about the PCB design recommendations.

3 Schematic

TAS2764 Schematic (Sheet 1 of 2) and TAS2764 Schematic (Sheet 2 of 2) show the typical application circuit for the TAS2764 with the components names used in this document. Refer to sheet 1 for mono version and sheet 1 and 2 for stereo verion.

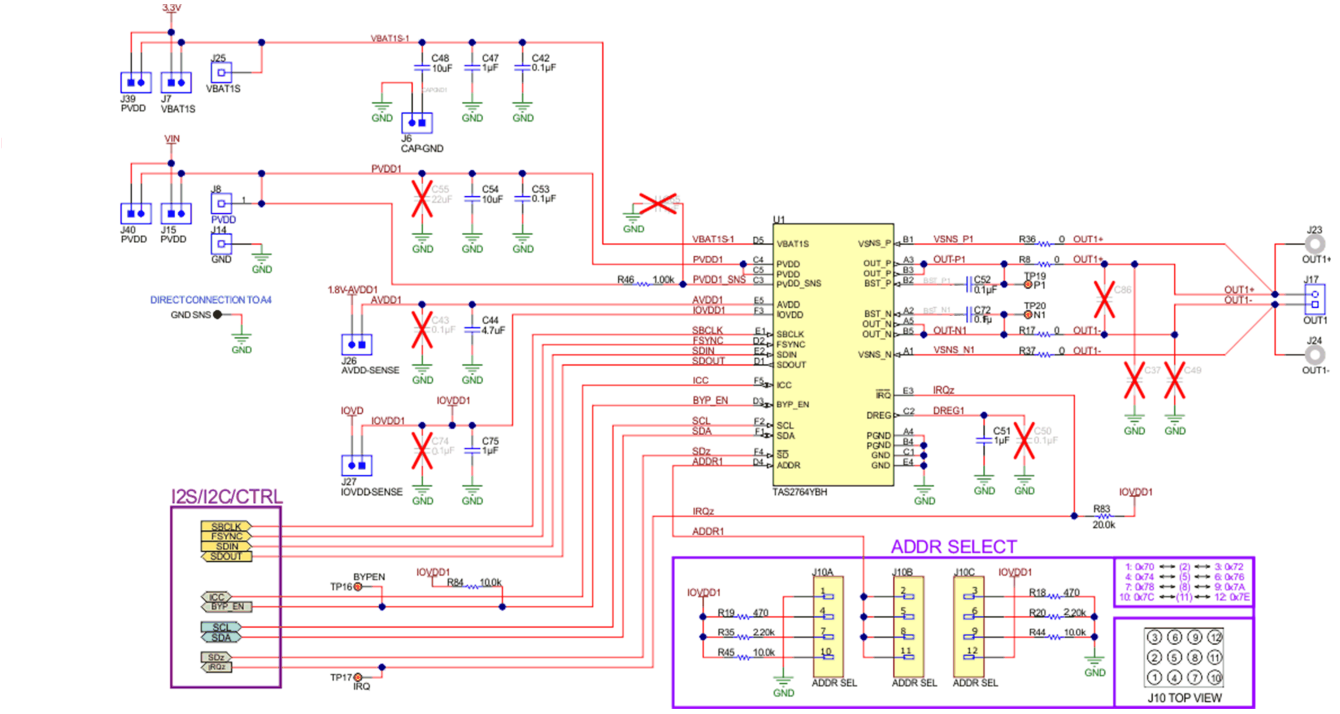

Figure 3-1. TAS2764 Schematic (Sheet 1 of 2)

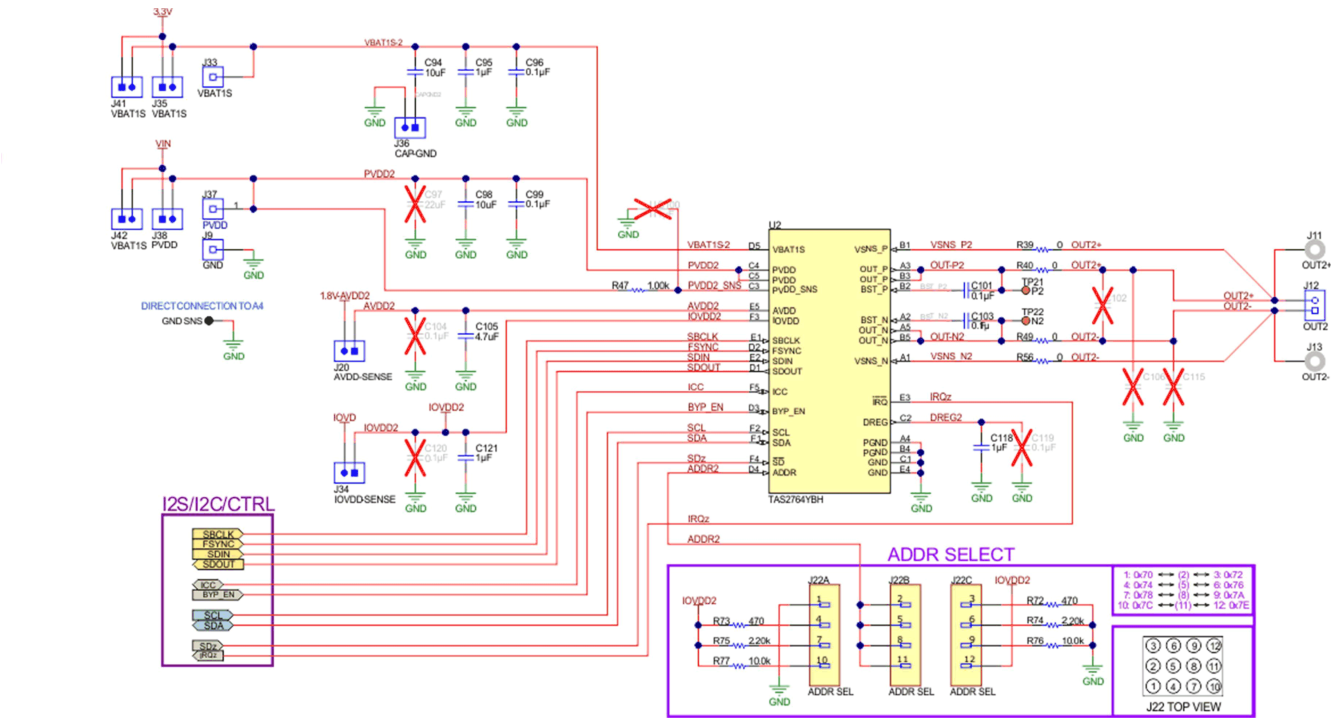

Figure 3-2. TAS2764 Schematic (Sheet 2 of 2)

3.1 Recommended External Components

Component	Description	Specification	MIN	TYP	MAX	UNIT
C48, C94	VBAT1S Decoupling Capacitor - VBAT1S External Supply	Type	X7R			
		Capacitance, 20% Tolerance	10			µF
		Rated Voltage	6			V
C47, C95	VBAT1S Decoupling Capacitor - VBAT1S Internally Generated	Type	X7R			
		Capacitance, 20% Tolerance	0.68	1	1.5	µF
		Rated Voltage	6			V
C42, C96	VBAT1S Decoupling Capacitor	Type	X7R			
		Capacitance, 20% Tolerance		0.1		µF
		Rated Voltage	6			V
C54, C98	PVDD Decoupling Capacitor	Type	X7R			
		Capacitance, 20%	10			µF
		Rated Voltage	20			V
C53, C99	PVDD Decoupling Capacitor	Type	X7R			
		Capacitance, 20%		0.1		µF
		Rated Voltage	20			V
C44, C105	AVDD Decoupling Capacitor	Type	X7R			
		Capacitance, 20% Tolerance	4.7			µF
		Rated Voltage	6			V
C51, C118	DREG Decoupling Capacitor	Type	X7R			
		Capacitance, 20% Tolerance	0.68	1	1.5	µF
		Rated Voltage	6			V
C75, C121	IOVDD Decoupling Capacitor	Type	X7R			
		Capacitance, 20% Tolerance	1			µF
		Rated Voltage	6			V
C52, C72, C101, C103	High-side Boost Capacitors	Type	X7R			
		Capacitance, 20% Tolerance	68	100	120	nF
		Rated Voltage	6			
Replace R8, R17, R40 and R49 by these inductors in case the EMI Filter is required	EMI Filter Inductors (optional). These are not recommended as it degrades THD +N performance. The device is a filter-less Class-D and does not require these bead inductors.	Impedance at 100MHz		120		Ω
		DC Resistance			0.095	Ω
		DC Current	5			A
C37, C49, C106, C115	EMI Filter Capacitors (optional, must use EMI inductors if C37, C49, C106, C115 used)	Capacitance		1		nF

4 Decoupling Capacitors

All the PCB routes have defined impedance that must be considered during all design stages. These signal paths will act as additional components in the board. In addition, the PCB lines have a parasitic inductance and capacitance that result in a different power distribution.

To reduce the negative effects of all these parasitic impedances, we recommend that the VBAT and VDD decoupling capacitor connections respect the following rules:

- **Place the decoupling capacitor close to the device pin in the same layer.** The decoupling capacitor stores local charge and supplies the large transient currents when it is required. The TAS2764 device has many switching activity and voltage fluctuations that demand large current transients in a short period of time. In addition, the parasitic effects caused by the vias, traces, and pads generate a voltage drop in the power supply. The proximity of the decoupling capacitors to the power pins compensates these effects and supplies the large transient currents when it is required.
  On a multi-layer board, the capacitors must be placed in the same layer where the TAS2764 device is located. Otherwise, the decoupling capacitor value may be reduced by the additional capacitance due to the vias connections.
- **Place the VDD and GND vias as close as possible to the decoupling capacitors.** If possible, place the vias directly or the closest as possible to the capacitor mounting pads. The vias have defined impedance determined by its length and diameter. This impedance may cause a voltage drop (in high-frequency applications the signal integrity is greatly influenced) and a current flow that must be reduced or avoided. For that reason, it is recommended to add many vias around the mounting pads. This practice reduces the parasitic impedance.

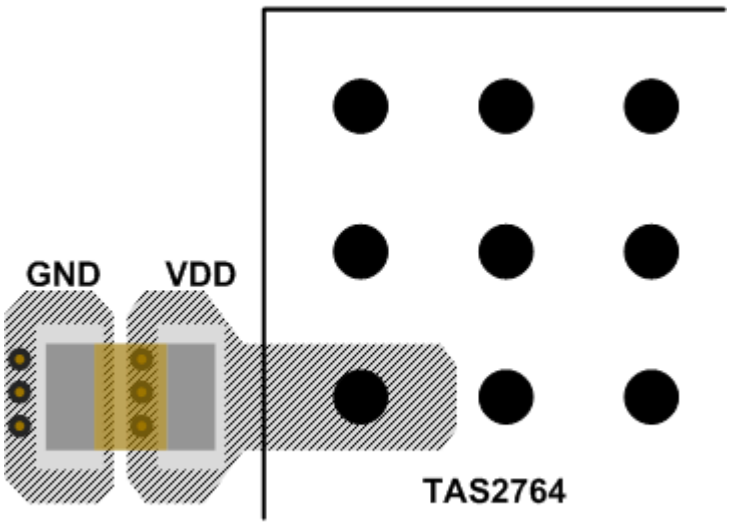

Figure 4-1. Decoupling Capacitor

Refer all the pins that require a decoupling capacitor to this section for detailed information.

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