EEPROM Emulation Using Low-Memory MSP430™ FRAM MCUs

Introduction

Electrically Erasable Programmable Read-Only Memory (EEPROM) devices are often used by end applications to store relatively small amounts of data which are retained when power is not supplied to the system. This type of data storage is valuable to applications requiring calibration data, unit identification, or backup information. Such an operation can be emulated by using ferroelectric random access memory (FRAM) available on select MSP430™ microcontrollers (MCUs). The ultra-low-power nature of FRAM makes it a great option for EEPROM emulation enabling nonvolatile writes for a fraction of the power used by conventional memories. Furthermore, FRAM offers practically unlimited write cycles and is not stressed from constantly logging data or saving system information. 48 bytes of FRAM are allocated to EEPROM functionality on the MSP430FR2000 MCU, a cost-effective FRAM device that has only 512 bytes of main memory, but larger devices can be substituted for more data storage or added functionality. To get started, download project files and a code example demonstrating this functionality.

Implementatiom

EEPROM emulation is configured to use SPI protocol in slave mode. A host processor acting as the master should be connected so that it can write or read data from the MSP430 MCU. Beyond the typical SPI bus (SCLK, MOSI, MISO, and CS) a write protect (WP) line is also used. Figure 1 shows the SPI block diagram interface.

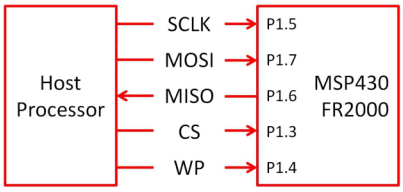

Figure 1. EEPROM SPI Block Diagram

The CS pin determines if the SPI is enabled and is active low by default. Communication is achieved by sending an op code followed by an 8-bit address, after which the EEPROM can be written to or read from until the memory space allocation has been exceeded or the CS line resets the SPI. The two op-code values are 0x02 (write) and 0x03 (read) but can be changed to the user's preference. Up to 256 bytes of EEPROM memory can be utilized on FRAM devices that exceed 512 bytes of total memory, but additional space will require changes to the code, because it accounts for only 8-bit addressing. The EEPROM page is protected from write commands until the WP line is driven low but read commands can be performed at any time. Figure 2 and Figure 3 show an interface example between a host device and MSP430 FRAM EEPROM emulator, in which a word is written starting at 0x0F and then read from 0x10.

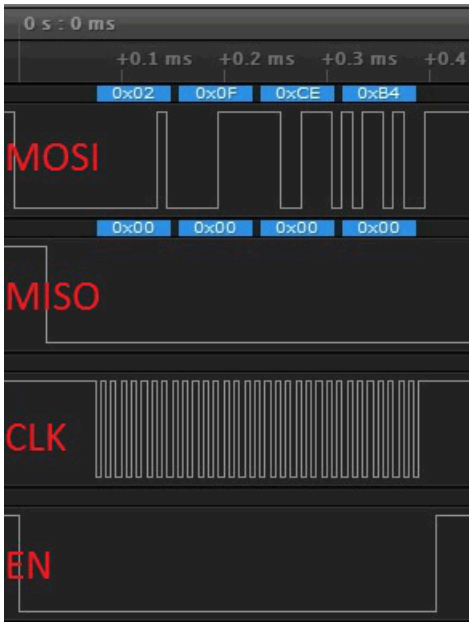

Figure 2. EEPROM Write Word Sequence

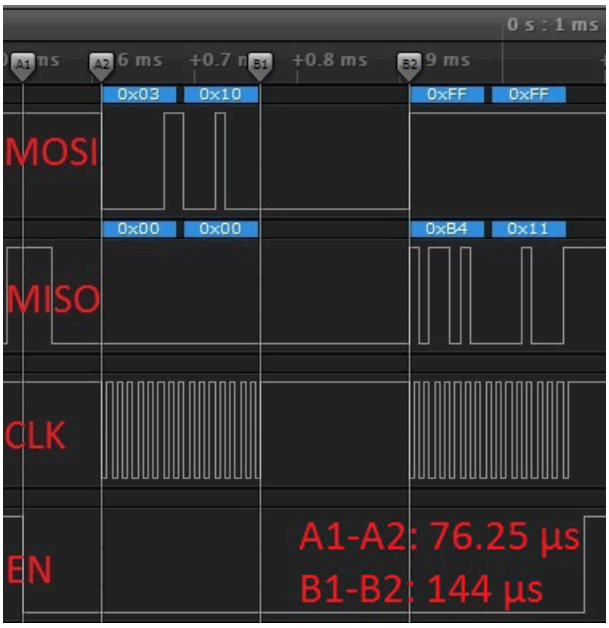

Figure 3. EEPROM Read Word Sequence

As seen in Figure 2, the "write" op-code (0x02) is followed by the desired address (0x0F), after which the word 0xCEB4 is supplied. A "read" op code (0x03) quickly follows with the address 0x10, and the MSP430 MCU responds with the 0xB4 value that was previously given as well as the preset value (0x11) stored at the memory address 0x11. Further investigation reveals that 0xCE has been properly written to address 0x0F as well. After the op code and address are given, writes or reads can continue repeatedly until the end of the memory page has been reached, at which point further instructions are ignored.

Performance

Using the MSP430FR2000 MCU has certain restrictions due to the 0.5KB of memory. For example, Figure 3 shows that a 75 µs delay is required between the high-to-low transition of the CS/EN pin and the start of the system clock (SCLK). 150 µs must also pass between the read address and reading from the EEPROM memory, and the CS/EN pin must remain high for at least 100 µs between SPI sequences.

Upgrading to one kilobyte of memory with the MSP430FR2100 MCU or reducing the necessary EEPROM page size allows enough additional memory space for increasing the operating frequency for faster response times. For a fuller featured and larger EEPROM memory, other MSP430 FRAM MCUs can be used with the TIDM-FRAM-EEPROM reference design, which uses the 256KB MSP430FR5994 device.

The firmware operates in low-power mode 3 (LPM3) when the SPI is not active but consumes 20 µA of current at 3 V, some of which is due to the internal pullup resistance on the CS pin. 15 µA is required to drive the internal trimmed low-frequency reference oscillator (REFO), but less than 2 µA is achievable by populating an external crystal and sourcing to the auxiliary clock (ACLK). Overall current consumption averages from active SPI communication depend on the number of bytes written to the FRAM during each transaction and the frequency to which the EEPROM is accessed. Use cases therefore need to be further evaluated by the user.

Device Recommendations

The device used in this example is part of the MSP430 Value Line Sensing portfolio of low-cost MCUs, designed for sensing and measurement applications. This example can be used with the devices shown in Table 1 with minimal code changes. For more information on the entire Value Line Sensing MCU portfolio, visit www.ti.com/MSP430ValueLine.

Table 1. Device Recommendations

Part Number	Key Features
MSP430FR2000	0.5KB FRAM, 0.5KB RAM, eComp
MSP430FR2100	1KB FRAM, 0.5KB RAM, 10-bit ADC, eComp
MSP430FR2110	2KB FRAM, 1KB of RAM, 10-bit ADC, eComp
MSP430FR2111	3.75KB FRAM, 1KB RAM, 10-bit ADC, eComp

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from September 16, 2017 to April 20, 2018	Page
• Corrected direction of MOSI and MISO in Figure 1, *EEPROM SPI Block Diagram*	1

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