Application Report
SLAA747–August 2017

Quick-Start Methods in Simulating the DAC38RF8x Input/Output Buffer Information Specification (IBIS) Model

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1 Introduction

Input/output Buffer Information Specification (IBIS) models are used to simulate digital electrical interfaces. These models can be categorized into two main categories: traditional and algorithmic modeling interface (AMI). AMI is typically used for SerDes channel simulation, and is different from the traditional IBIS model, which is the focus of this document. These models are simple ASCII text files that contain buffer voltage-current (V-I) characteristics and output voltage over-time (V-T) characteristics. In the model file, the individual digital pins and their respective signal type, model name, and parasitic RLC values are all listed. Notes and other information may be included as well.

Typical models include single-ended or differential input, output, I/O, and tristate among others. One advantage of IBIS models over simulation programs with integrated circuit emphasis (SPICE) models is that IBIS models do not model the actual silicon or transistor-level circuitry of the integrated circuit (IC), so proprietary information regarding the IC is not revealed. Simulation time is greatly reduced compared to SPICE simulation for this same reason.

IBIS models are used in Signal Integrity (SI) simulation. Single-ended input and output models are used to simulate one pin at a time, while differential models simulate a pair of complementary pins. Simulating circuits that employ IBIS models can be achieved using a number of programs, however Advanced System Design (ADS) and HyperLynx are used to explore a simplified example of an SI simulation.

2 Simulation Overview

2.1 Example Circuit

Figure 1 shows a circuit simulated in ADS and HyperLynx.

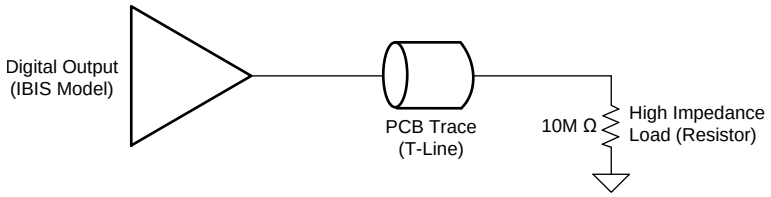

Figure 1. ADS and HyperLynk Simulated Circuit

In this example, the GPO0 pin of the DAC38RF80 device drives a high-impedance node. The length of the PCB trace between the pin and load is set to 3 inches. This trace is a stripline that is fully embedded in dielectric material. Also, the characteristic impedance of the trace is approximately 50 Ω. In a practical simulation, additional parasitic factors may also be modeled and the pin may drive a digital receiver, rather than a purely-resistive high-impedance load.

3 Simulation Description

3.1 ADS Simulation

ADS offers a wide range of simulation tools, including the ability to simulate IBIS models. The following steps describe the process to simulate the previous example.

1. After creating a new workspace and a new schematic, select Signal Integrity – IBIS from the palette drop-down menu and place an IBIS_O model on the schematic.
2. Connect the PC and PU nodes to each other with a wire.
3. Connect the GC and PD nodes to each other with a wire, and then to ground.
4. Select Sources-Time Domain from the palette drop-down menu.
5. Place a V_DC model on the schematic.
6. Place a Pulse model on the schematic and configure according to Figure 2.

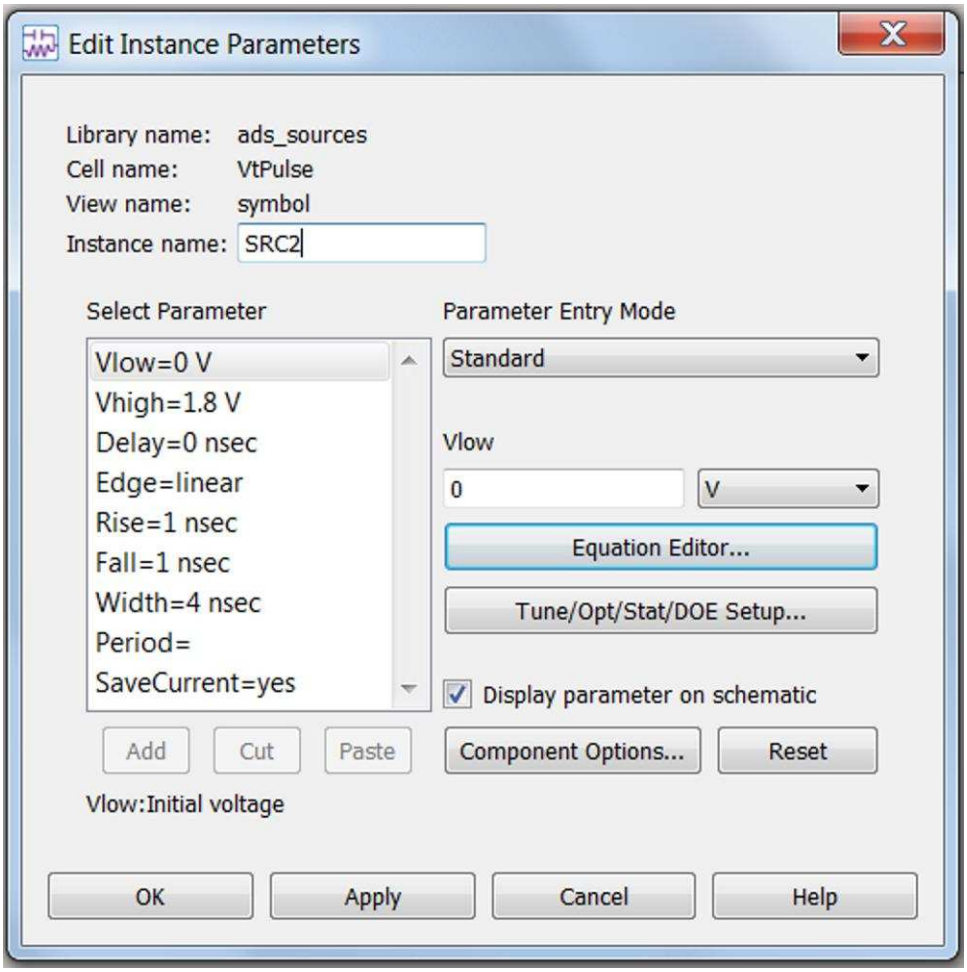

Figure 2. Pulse Source Configuration

7. Connect the positive node of the DC voltage source to the PU and PC nodes, and connect the negative node to ground.
8. Connect the positive node of the pulse source to the T node of the IBIS_O model, and connect the negative node to ground.
9. Select Lumped-Components and place a resistor on the schematic.
10. Set the resistor value to 10 MΩ.
11. Select TLines-Stripline from the palette drop-down menu.

12. Place a SSUB and SLIN model onto the schematic.
13. Set the width of the transmission line to 6 mil and its length to 3 in.
14. Connect the output of the IBIS_O model to one end of the transmission line and connect the other end to the 10 MΩ resistor.
15. Ground the other end of the resistor.
16. Configure the transmission line substrate according to Figure 3.

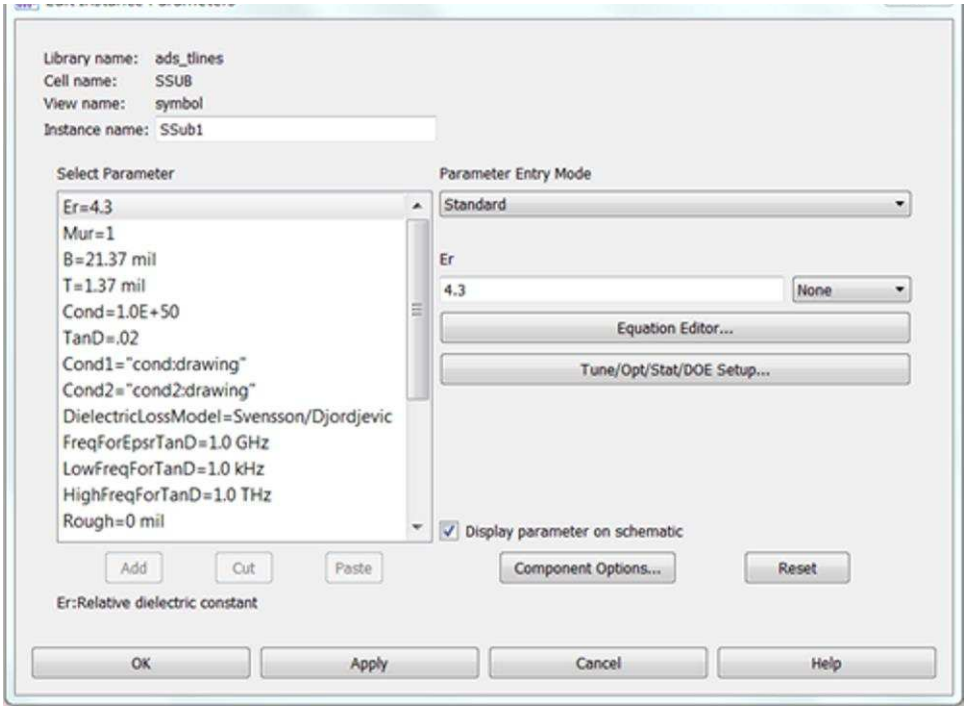

Figure 3. Stripline Substrate Configuration

17. Double-click on the IBIS model.
18. Click on the Select IBIS File button and then browse to the location on the PC containing the DAC38RF80 IBIS file. Select the file and click OK.
19. Navigate to the Pin tab, verify that GPO0 is highlighted, then click OK.

20. Select Simulation-Transient from the palette drop-down menu and configure it as shown in Figure 4.

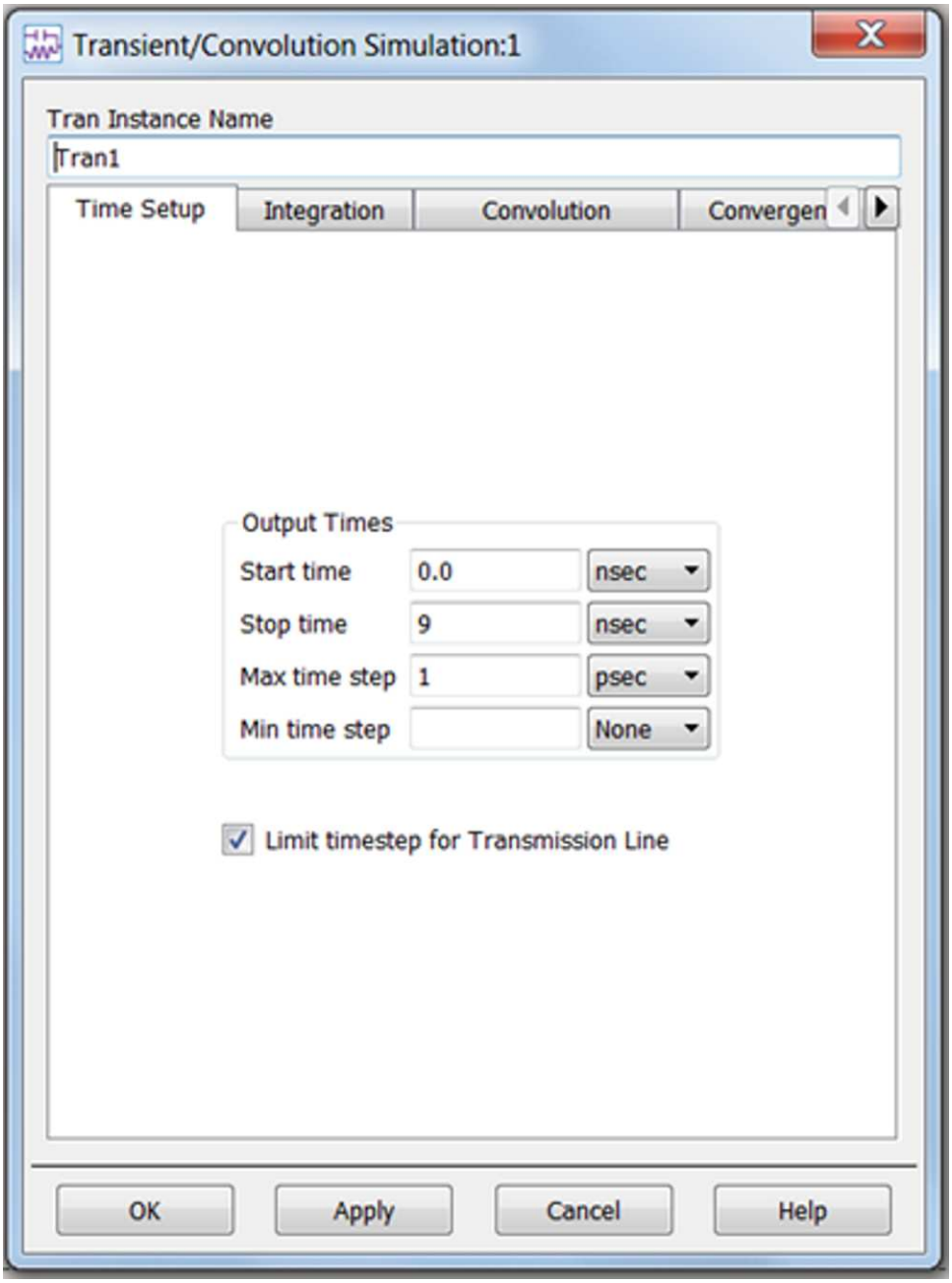

Figure 4. Transient Simulation Parameters

21. Name the net just before the transmission line, and name the net just after it as well.

22. Click on the Simulation icon. Figure 5 shows the complete circuit.

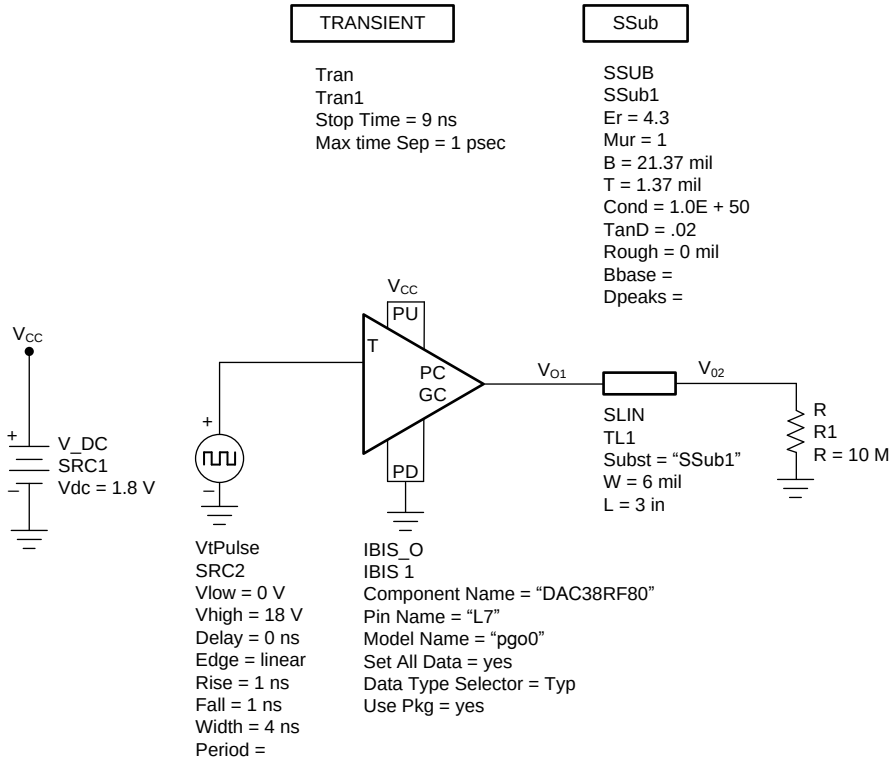

Figure 5. Signal Integrity Simulation Circuit – ADS

3.1.1 ADS Simulation – Results

Figure 6 and Figure 7 show the results of ADS simulation.

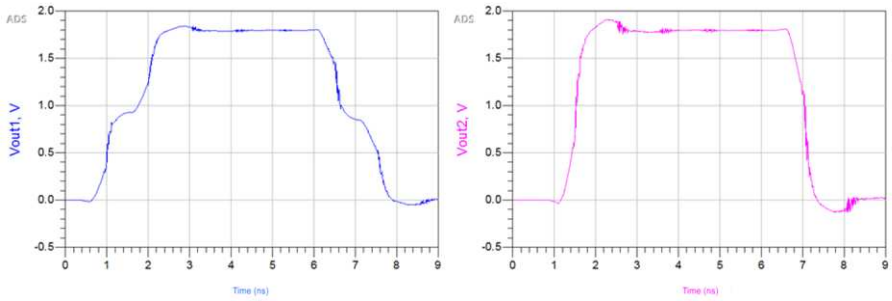

Figure 6. Signal at Driver Pin (Left) and Load (Right) – ADS

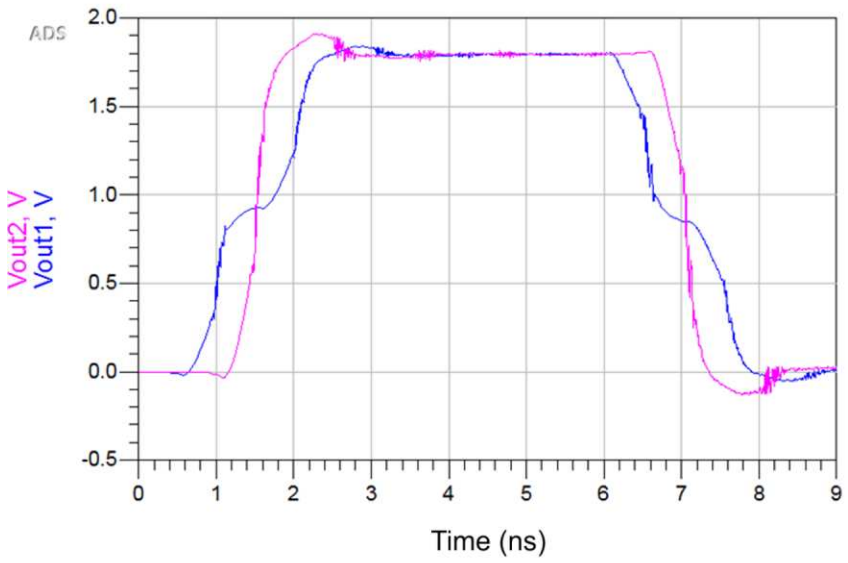

Figure 7. Overlay of Signal at Driver Pin (Blue) and Load (Magenta) – ADS

3.2 HyperLynx Simulation

HyperLynx is another tool used to simulate IBIS models. The following steps describe the process to simulate the previous example.

1. From the menu bar, select File → New Free Form Schematic → SI (or SI/PI).
2. Using the menu bar, navigate to Setup → Options → Directories.
3. In the Set Directories window that appears, click on the Edit button near the model-library file path section.
4. Browse to the directory in which the IBIS file is stored and then click on the Add button.
5. From the palette containing the schematic models, select the single-ended IC and place it on the schematic.
6. Place a single, horizontal, transmission line on the schematic.
7. Place a resistor on the schematic.
8. Connect the output of the IC to one end of the transmission line.
9. Connect the other end of the transmission line to the resistor.
10. Connect the other end of the resistor to ground.
11. Set the value of the resistor to 10 MΩ.
12. Double-click on the transmission line and in the Transmission Line Type section, and then select Stripline.
13. Navigate to the Values tab and configure the transmission line as shown in Figure 8, then click OK.

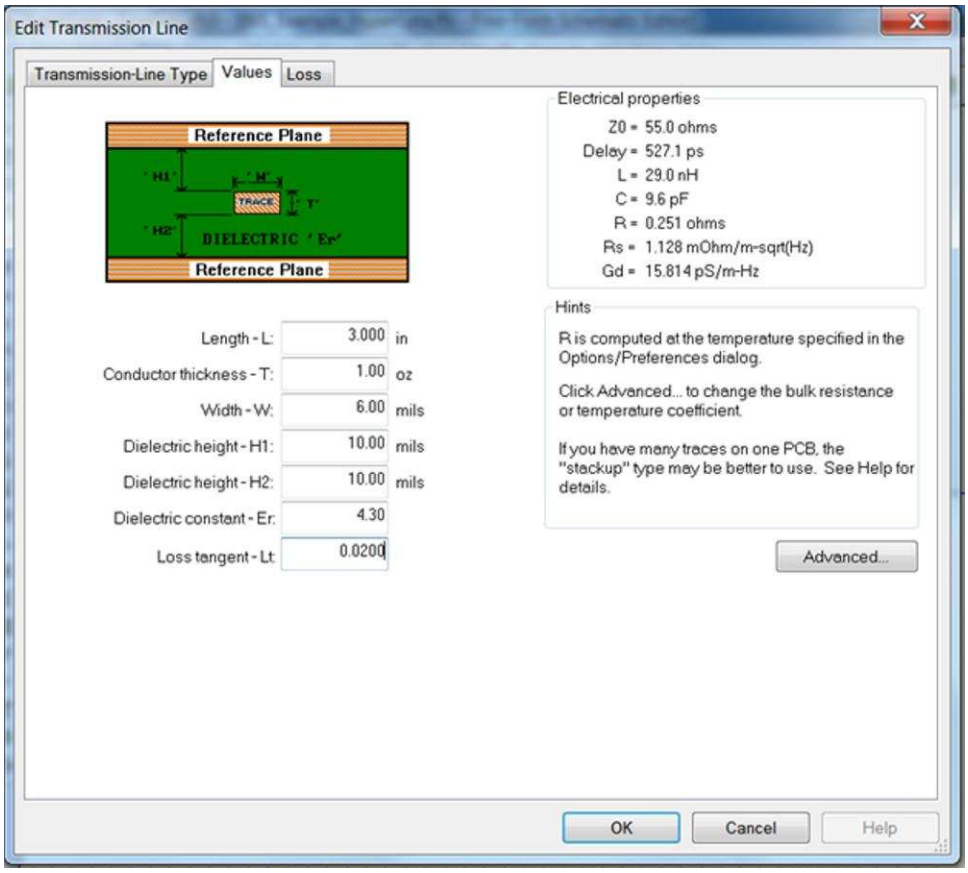

Figure 8. Stripline Configuration

14. Double-click on the IBIS model.
15. Click the Select button, then select the DAC38RF80 model, which should be selectable in the Libraries list.

NOTE: After the DAC38RF80 model is selected, the Devices list should only show DAC38RF80.

16. Select GPO0 from the Signal list, then click OK.

NOTE: If Steps 2 to 4 were not correctly completed, then the Libraries list will not show the DAC38RF80 file.

17. Verify that the Output option is selected in the Buffer Settings section and then click OK.
18. Click on the Interactive Simulation icon. Figure 9 shows the complete circuit.

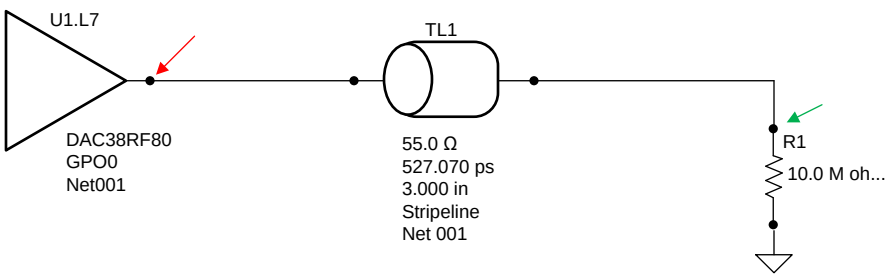

Figure 9. Signal Integrity Simulation Circuit – HyperLynx

19. In the Stimulus section, select Per Net/Pin and click on the Assign button.

20. When the Assign Stimulus window opens, click on Edit Stimulus.
21. Create a Pulse by configuring the stimulus, as shown in Figure 10.

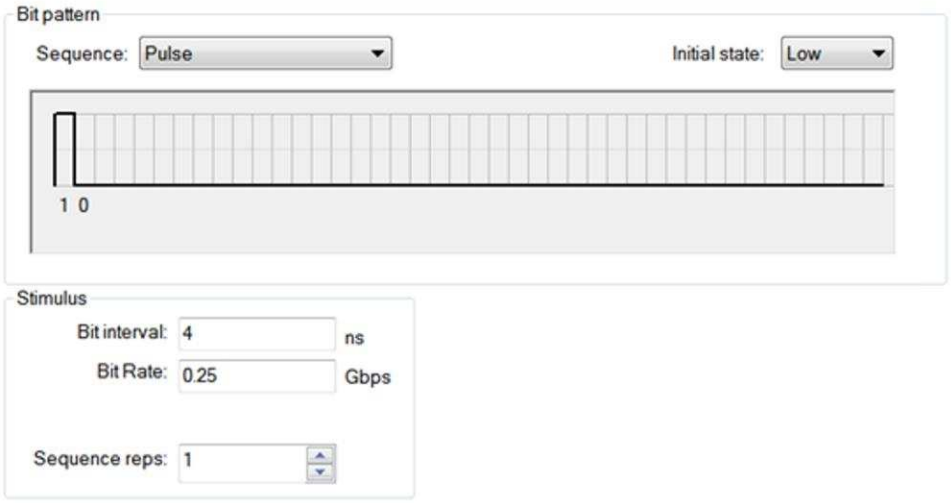

Figure 10. Stimulus Configuration

22. Before clicking OK, save the stimulus as a separate file, to a known directory, because the default stimulus cannot be edited.
23. Using the menu bar, navigate to Setup → Options → Directories.
24. In the Set Directories window that appears, click on the Edit button in the stimulus file path section.
25. Browse to the directory in which the IBIS file is stored and then click on the Add button.
26. After returning to the Assign Stimulus window, the newly created stimulus file may be selected from the Stimulus drop-down list.
27. Click OK and then click Start Simulation.

3.2.1 HyperLynx Simulation – Results

Figure 11, Figure 12, and Figure 13 show the results of HyperLynx simulation.

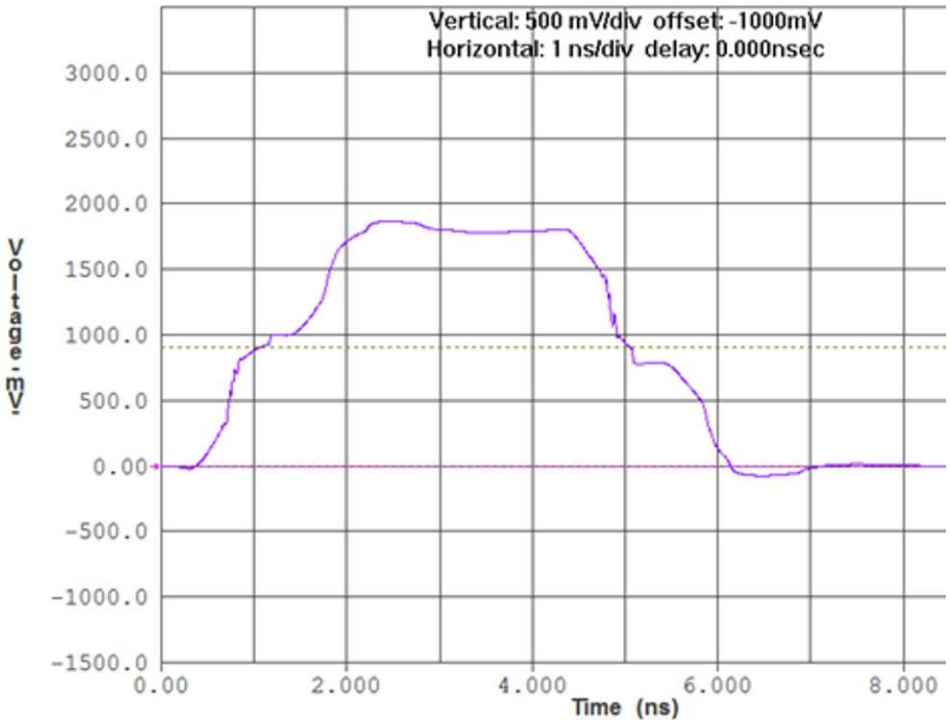

Figure 11. Signal at Driver Pin – HyperLynx

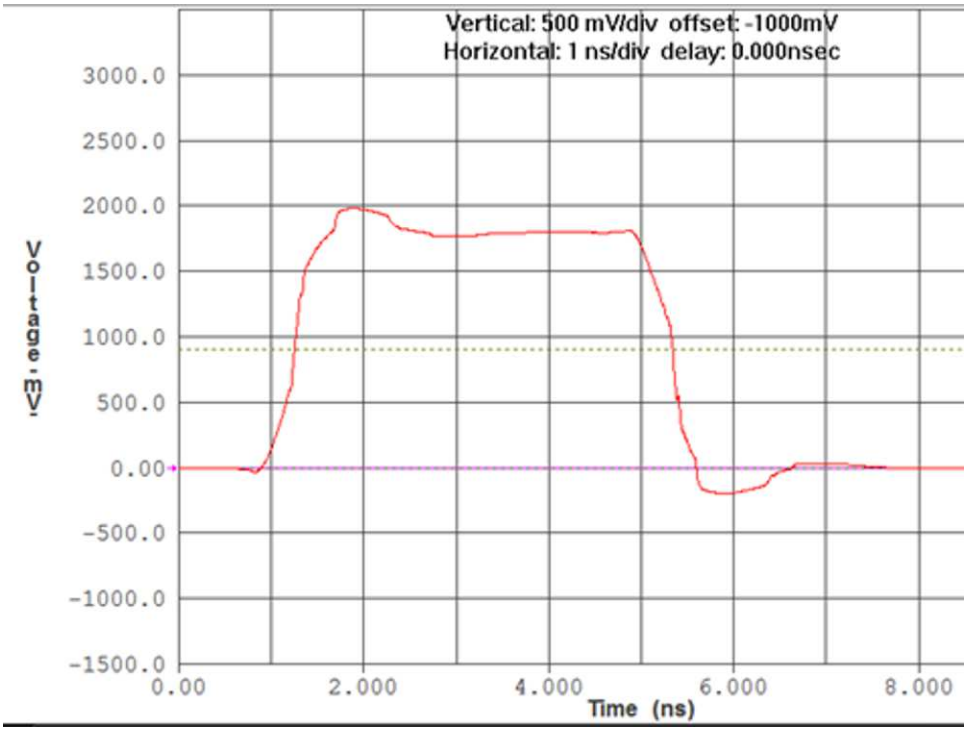

Figure 12. Signal at Driver Load – HyperLynx

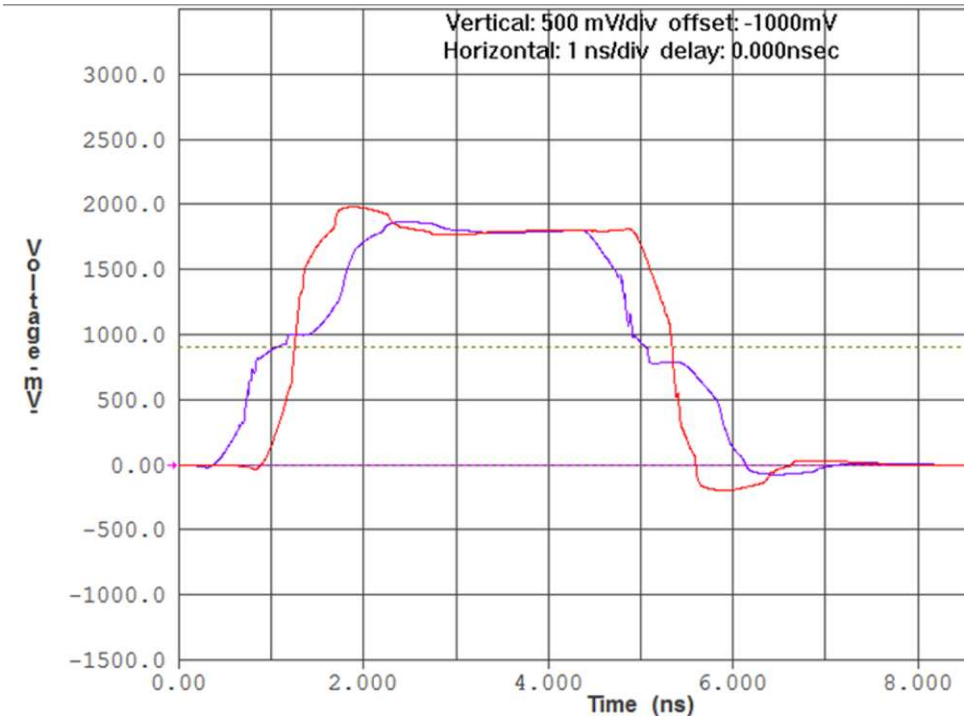

Figure 13. Overlay of Signal at Driver Pin (Purple) and Load (Red) – HyperLynx

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