RF Sampling DAC with 800 MHz of IBW LTE

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ABSTRACT

This document describes a candidate device, DAC38RF8x, for the next generation (5G) cellular systems that shows a total of 800 MHz of Instantaneous Bandwidth (IBW) using Long Term Evolution (LTE) patterns (40 of LTE 20 MHz) captured from spectrum analyzer.

Over the last decade, the wireless infrastructure industry has been investing large amounts of research and equipment in 3.5G (Mobile WiMAX), 3.9G (LTE), 4G (Advanced LTE) networks to provide higher data rates to end users by deploying advanced technologies such as multiple-input-multiple-output (MIMO) and carrier-aggregation (CA). 5G requires microwave and mmWave frequency bands (licensed and unlicensed) with wide bandwidth up to 2 GHz or wider. The standard body of 5G specifications such as the Third Generation Partnership Project (3GPP) envisions 28 GHz up to 40 GHz or higher of channel frequency with 1 GHz of instantaneous bandwidth (IBW).

DAC38RF8x is a dual-channel 14-bit digital to analog converter (DAC) and provides 9 Gsps of DAC sample rate. This device has an 8-lane JESD204B interface with a maximum input bit rate of 12.5 Gbps. DAC38RF8x supports subclass 1 for multi-chip synchronization. Up to x24 of interpolation enables users to transmit 375 MHz of baseband rate from FPGA, and 4 independent Numerically Controlled Oscillator (NCO) supports 4 different frequency bands from one DAC38RF8x device.

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1 Theory of Operation

The DAC38RF8x is a family of high performance dual channel 14-bit, 9 Gsps RF DACs, capable of synthesizing wideband signals from 0 to 4.5 GHz. A high dynamic range allows the DAC38RF8x to generate 4G/5G signals for wireless base stations with an output frequency up to 4 GHz.

The devices have a low power JESD204B interface with up to 8 lanes, with a maximum bit rate of 12.5 Gbps and input sample rate of 1.23 Gsps complex per channel. The DAC38RF8x has two digital up-converters per DAC, with multiple interpolation factors and digital quadrature modulator with independent, frequency flexible NCOs. An optional low jitter Phase Locked Loop (PLL)/Voltage Controlled Oscillator (VCO) simplifies the DAC clock generation by allowing users of a lower frequency reference clock.

In this document, 200 MHz (10xLTE20MHz) of IBW is transmitted from FPGA JESD204B Serializer/Deserializer (SerDes) lanes and combined to 800 MHz of IBW with 4 different NCOs from DAC38RF8x. Combined 800 MHz of IBW can be measured from spectrum analyzer.

1.1 Test Pattern Profile of 800 MHz

The 200 MHz of IBW LTE pattern was created by combining 10 of LTE TM3.1 20 MHz carriers and each of LTE 20 MHz carriers was generated with different Cell ID to avoid peak regrowth.

Figure 1 shows 10xLTE 20 MHz carriers that span an IBW of 200 MHz without gain equalization. Each carrier has different subcarrier information so each of carrier powers is different. From the view point of field operation, it is true that each of carrier power shows different level among multi carriers.
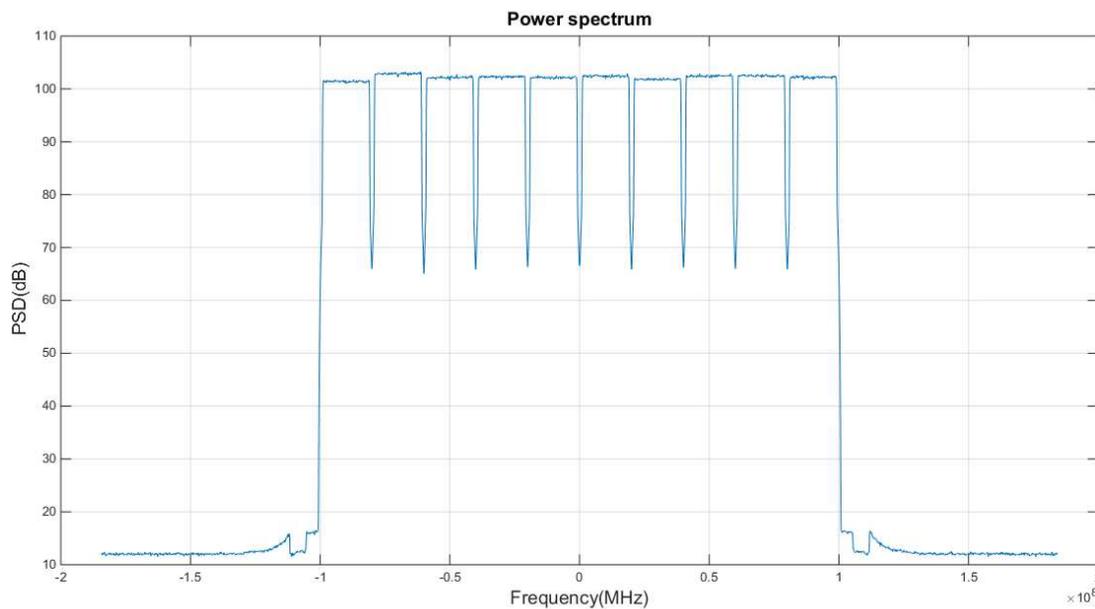
Figure 1. 200 MHz of IBW Without Gain Equalization From MATLAB

To achieve a flat multi-carrier over 200 MHz, gain equalization was applied to each of carriers from MATLAB shown as Figure 2.
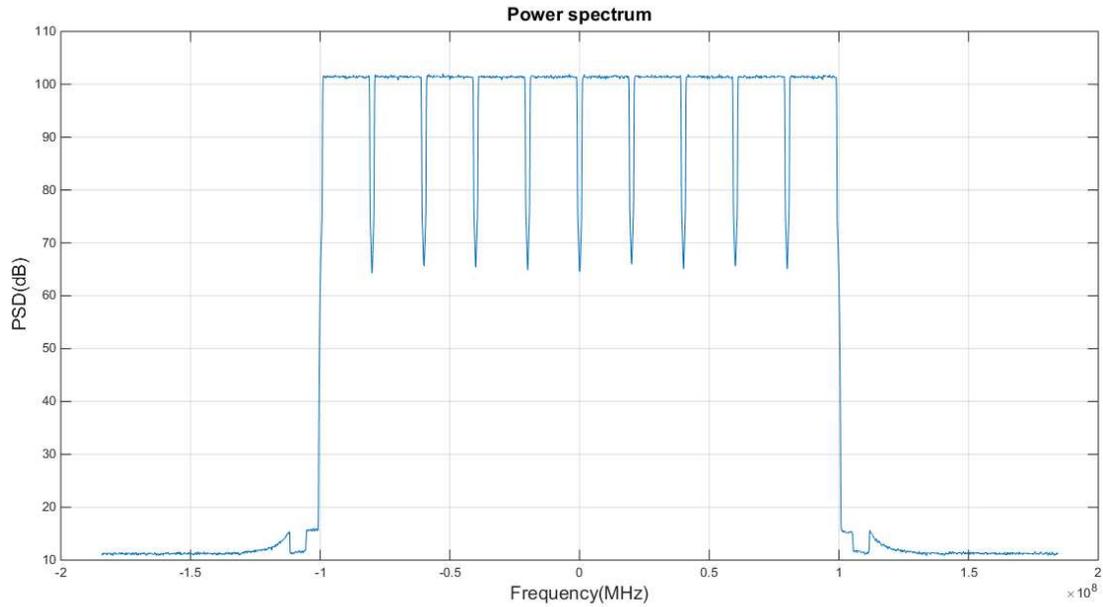

Figure 2. 200 MHz of IBW With Gain Equalization From MATLAB

Figure 3 shows 9.74 dB of peak-to-average ratio (PAR) of 200 MHz IBW at 0.01% from complementary cumulative distribution function (CCDF) curve. The measured PAR (9.74 dB) of 200 MHz shows the same PAR of single LTE carrier.
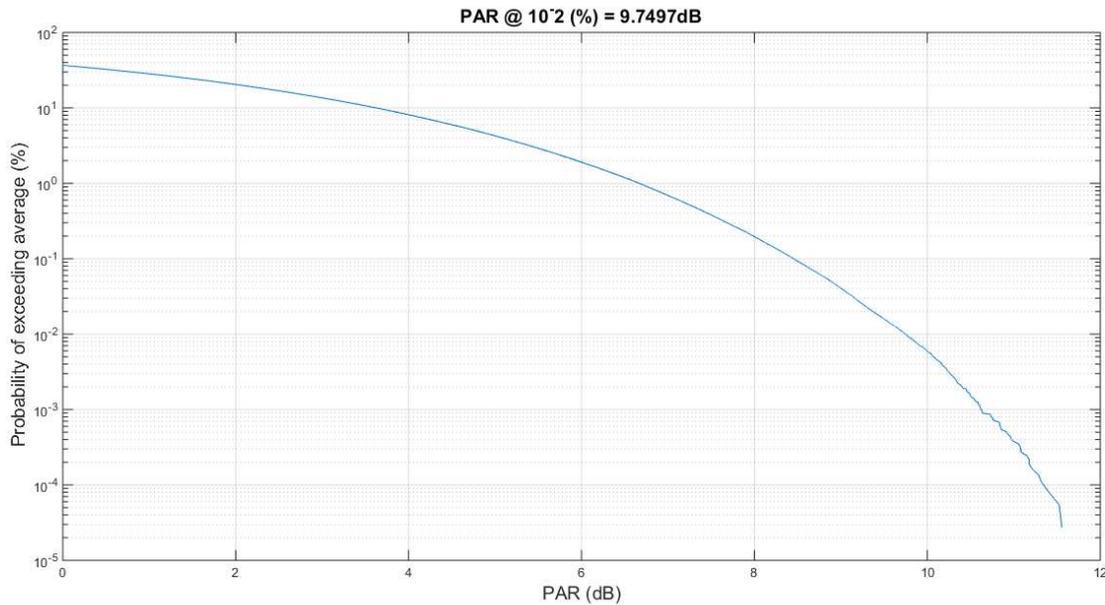

Figure 3. 9.74 dB of PAR at 0.01% from CCDF Curve

The 200 MHz of IBW LTE pattern consists of 16-bit of two's complementary and this pattern has approximately 0.5 dB of headroom from the peak threshold which is ±32768. Figure 4 shows the complex I/Q patterns in the time domain from MATLAB.
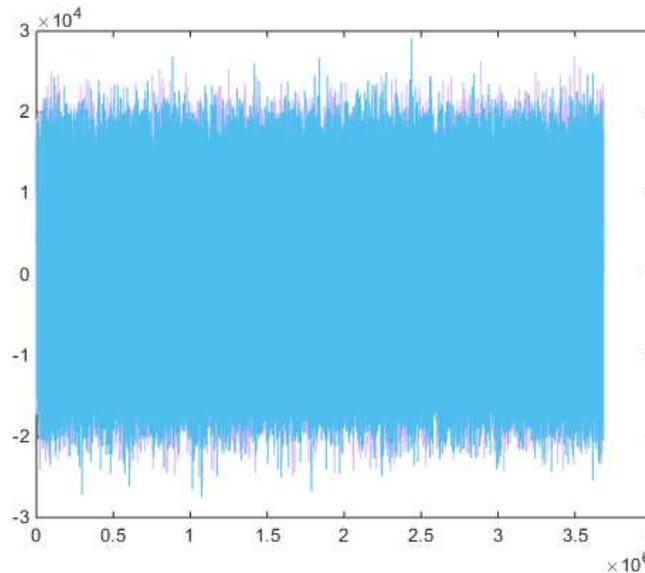
Figure 4. Baseband Complex I/Q Patterns in the Time Domain From MATLAB

1.2 *Operation of DAC38RF8x*

DAC38RF8x has four SerDes I/Q lane pairs per DAC channel, which is 8 configurable JESD204B serial lanes shown as below in Figure 5. The highest speed of each SerDes lane is 12.5 Gbps.
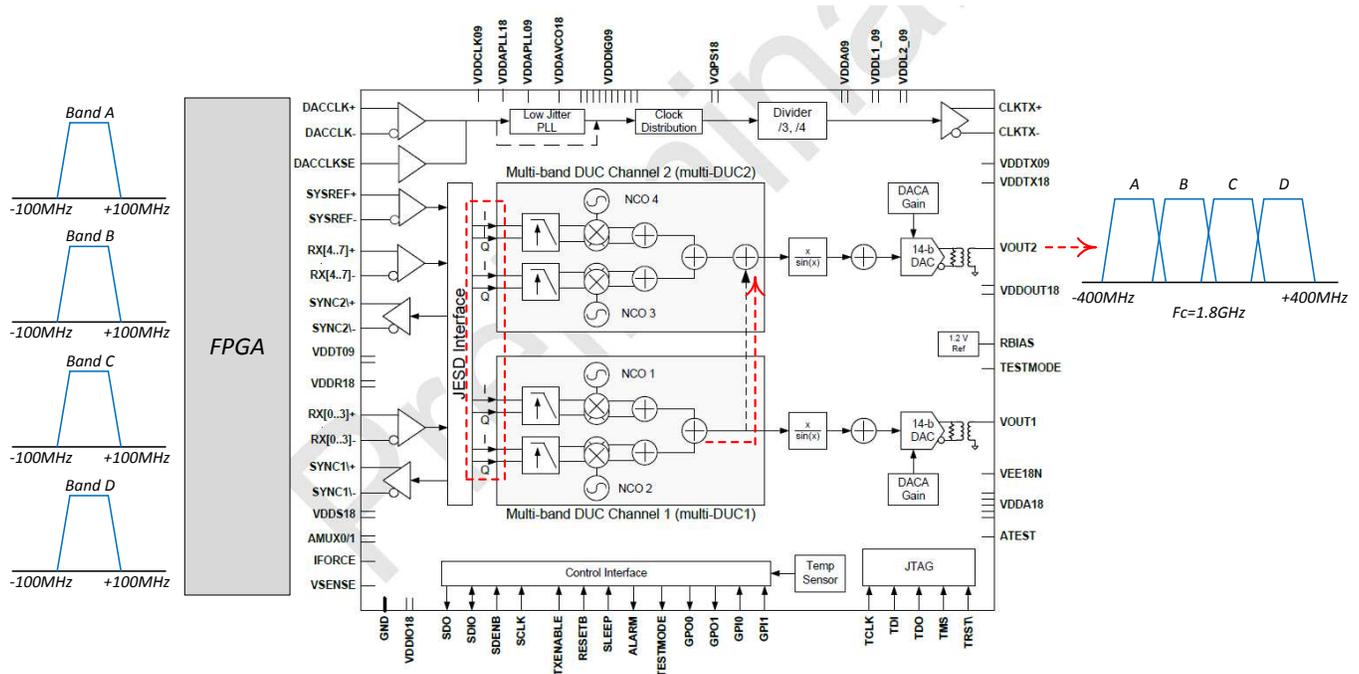
Figure 5. Block Diagram of Combined 800 MHz With Different NCOs

Table 1 is an example of DAC38RF8x configuration for commercial system operation. The baseband pattern has 368.64 MHz of data rate from each of SerDes interface from FPGA, and this pattern is interpolated by 24 in DAC38RF8x. The required DAC sampling clock frequency is 8847.36 MHz (= 368.64 MHz x 24) and the on-chip PLL provides this clock.

DAC38RF8x has 14-bit resolution of DAC interface but 16-bit is sent from FPGA in this configuration. The SerDes lane speed, F_{SerDes}, from FPGA can be calculated as shown in Equation 1.

F_{SerDes} = 1 (Non-interleaved I/Q) x 368.64 Msps x 16 bits x 10/8 = 7372.8 Mbps,

where

- 10/8 is for 8b/10b decoding   (1)

Table 1. Example of DAC38RF8x Configuration Parameters

PARAMETERS	VALUE	UNIT
DAC Clock Frequency	8847.36	MHz
Reference Frequency for On-chip PLL	368.64	MHz
Baseband Input Rate	368.64	MHz
# of DAC	Dual	DAC
# of I/Q Pairs per DAC	2	I/Q Pair
# of SerDes Lanes per DAC	4	Lane
Interpolation Factor	24	x
Target RF Frequency	1843.2	MHz
NCO Frequency Path AB for DACA	1543.2	MHz
NCO Frequency Path CD for DACA	1743.2	MHz
NCO Frequency Path AB for DACB	1943.2	MHz
NCO Frequency Path CD for DACB	2143.2	MHz
JESD204B Frame Format for "LMF"	882	

The DAC38RF8x has a total of 8 lanes for dual DAC, which each of DAC has 4 lane interfaces with FPGA. In this application, the maximum input rate is 375 Msps and 9 Gsps for maximum sampling rate with 24 of interpolation factor.

Table 2 describes JESD204B frame format of DAC38RF8x for this application. In-phase (I) and Quadrature-phase (Q) signals are formatted as interleaved and transmitted from FPGA in this mode, and 8b/10b coding is to ensure DC balancing of the digital data stream.

Table 2. JESD204B Frame Format for LMF = 882

# un bits	4	8	12	16
# en bits	5	10	15	20
Nibble	1	2	3	4
lane RX0	i0			
lane RX1	q0			
lane RX2	i1			
lane RX3	q1			
lane RX4	i2			
lane RX5	q2			
lane RX6	i3			
lane RX7	q3			

The following list provides the meaning of symbols and abbreviations from JEDEC (Joint Electron Device Engineering Council) standard.
- L: Number of lanes per converter device
- M: Number of converters per device
- F: Number of octets per frame

2   Performance Evaluated from DAC38RF8xEVM

From the configuration parameters shown in Table 1, Figure 6 shows –55.55 dBc of measured ACLR of the combined 800 MHz of IBW from spectrum analyzer. The noise reduction feature from PXA helps noise floor improved and consequently gives us a good ACLR at 1.8432 GHz of RF center frequency. In general, 20 MHz of signal LTE carrier shows around -70 dBc of ACLR and 40-carrier of LTE 20 MHz should be around -54 dBc of ACLR calculated by Equation 2.

$$-70 \text{ dBc} + 16 \text{ dB} \ (= 10 \times \log_{10}(40)) \tag{2}$$

To avoid droop occurred DAC sampling process, inverse sinc feature of DAC38RF8x was applied to each of Digital Up-Converter (DUC) blocks, and 6 dB of mixer gain was used for the maximum output power.
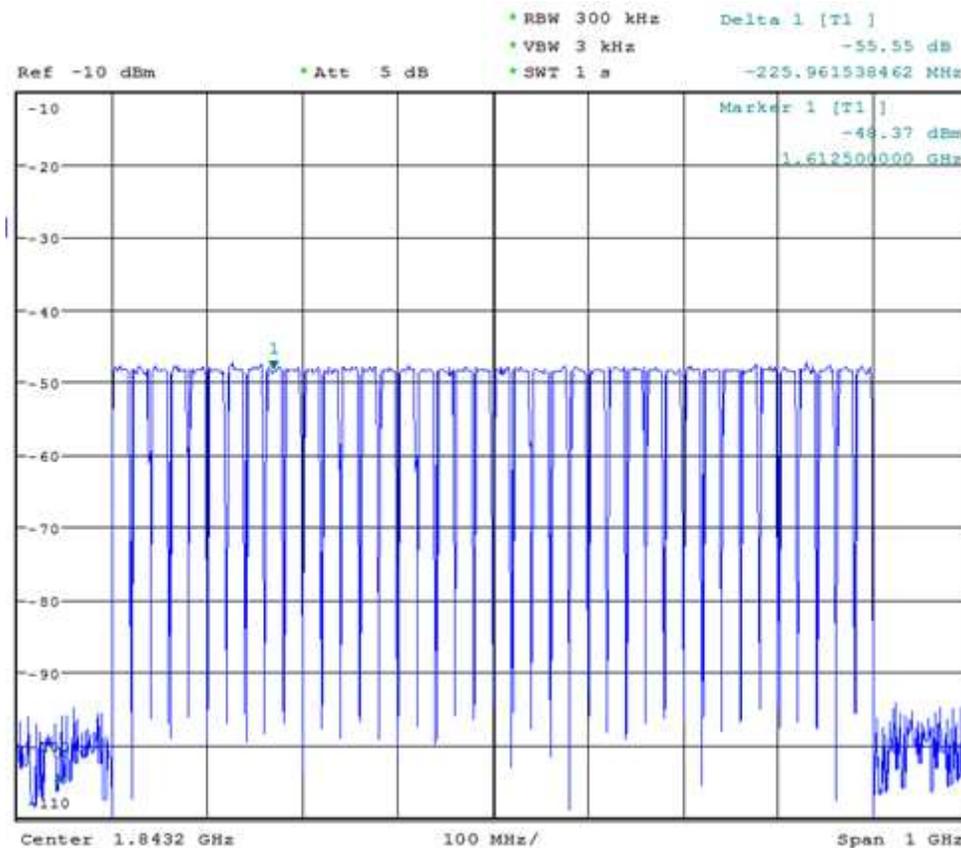
Figure 6. ACLR of 800 MHz IBW Measured (–55.55 dBc) From Spectrum Analyzer

Figure 7 shows measured Error Vector Magnitude (EVM) from the carrier located 1.4532 GHz, which is 0.45%. The baseband LTE pattern is directly up-converted to 1.5432 GHz by Numerically Controlled Oscillator (NCO) so there is no I/Q impairment during this process because it is achieved only in digital domain.

Spectral flatness wise, it looks quite good enough with modulated LTE carriers. Each of LTE carriers has different sub-carriers due to different cell ID. For the signal quality, Error Vector Magnitude (EVM) was measured from Vector Signal Analyzer (VSA). Figure 7 through Figure 10 shows measured EVM over 800 MHz of IBW.
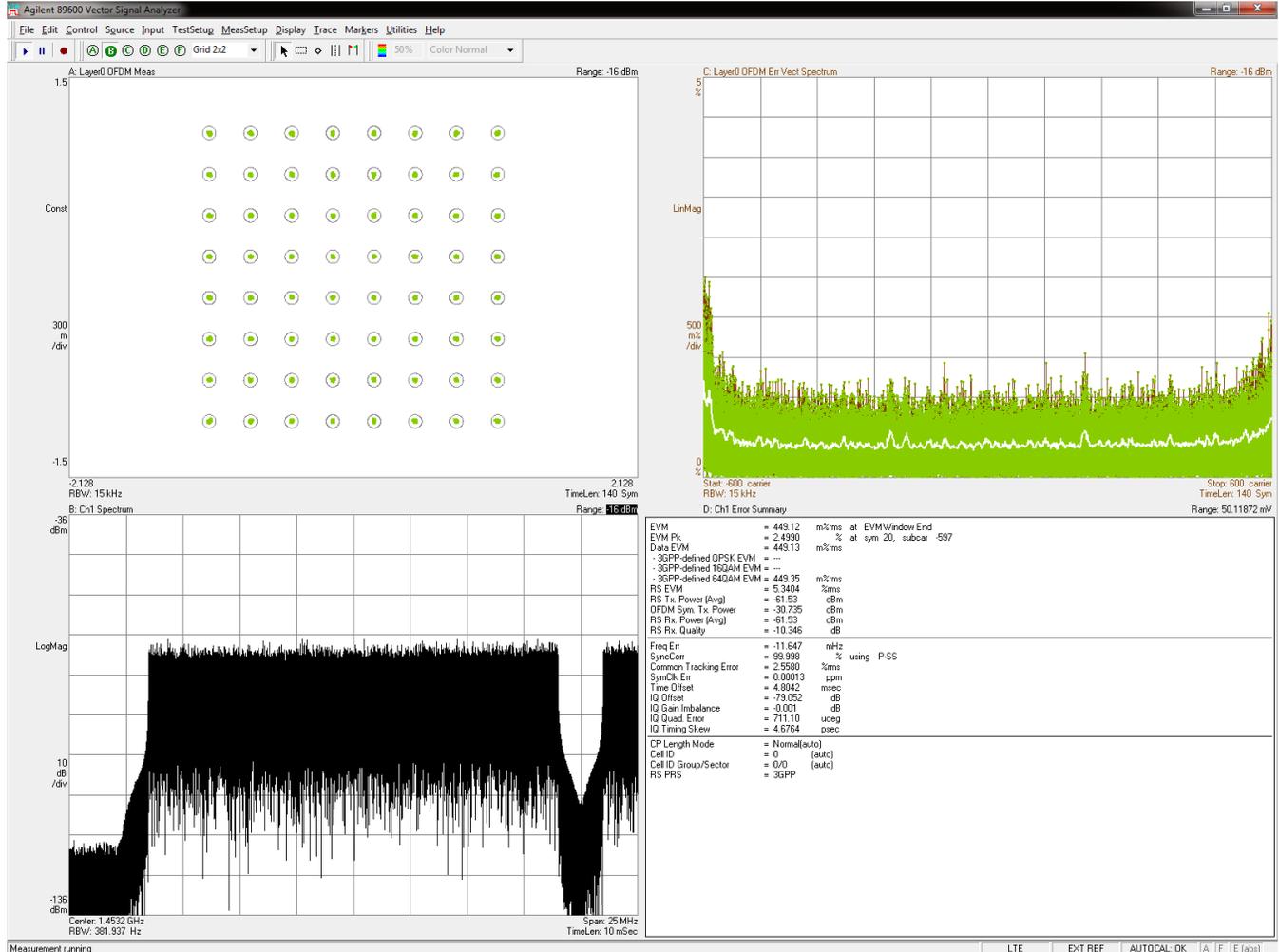
Figure 7. Measured EVM (0.45%) at 1.4532 GHz

Figure 8 shows measured Error Vector Magnitude (EVM) from the carrier located 1.6532 GHz, which is 0.47%. The baseband LTE pattern is directly up-converted to 1.7432 GHz by Numerically Controlled Oscillator (NCO) so there is no I/Q impairment during this process because it is achieved only in digital domain. .
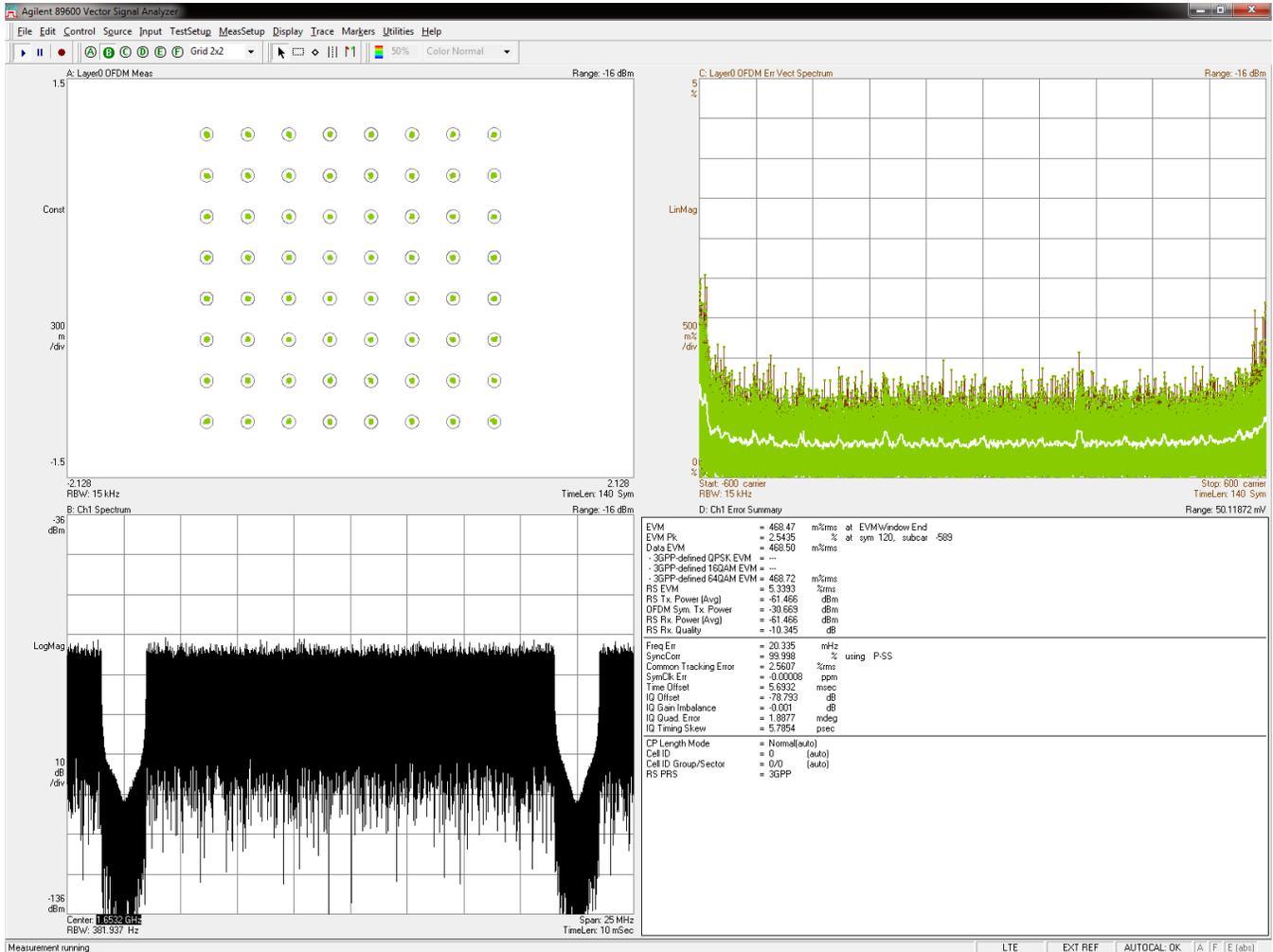
Figure 8. Measured EVM (0.47%) at 1.6532 GHz

Figure 9 shows measured Error Vector Magnitude (EVM) from the carrier located 1.8732 GHz, which is 0.49%. The baseband LTE pattern is directly up-converted to 1.9432 GHz by NCO.
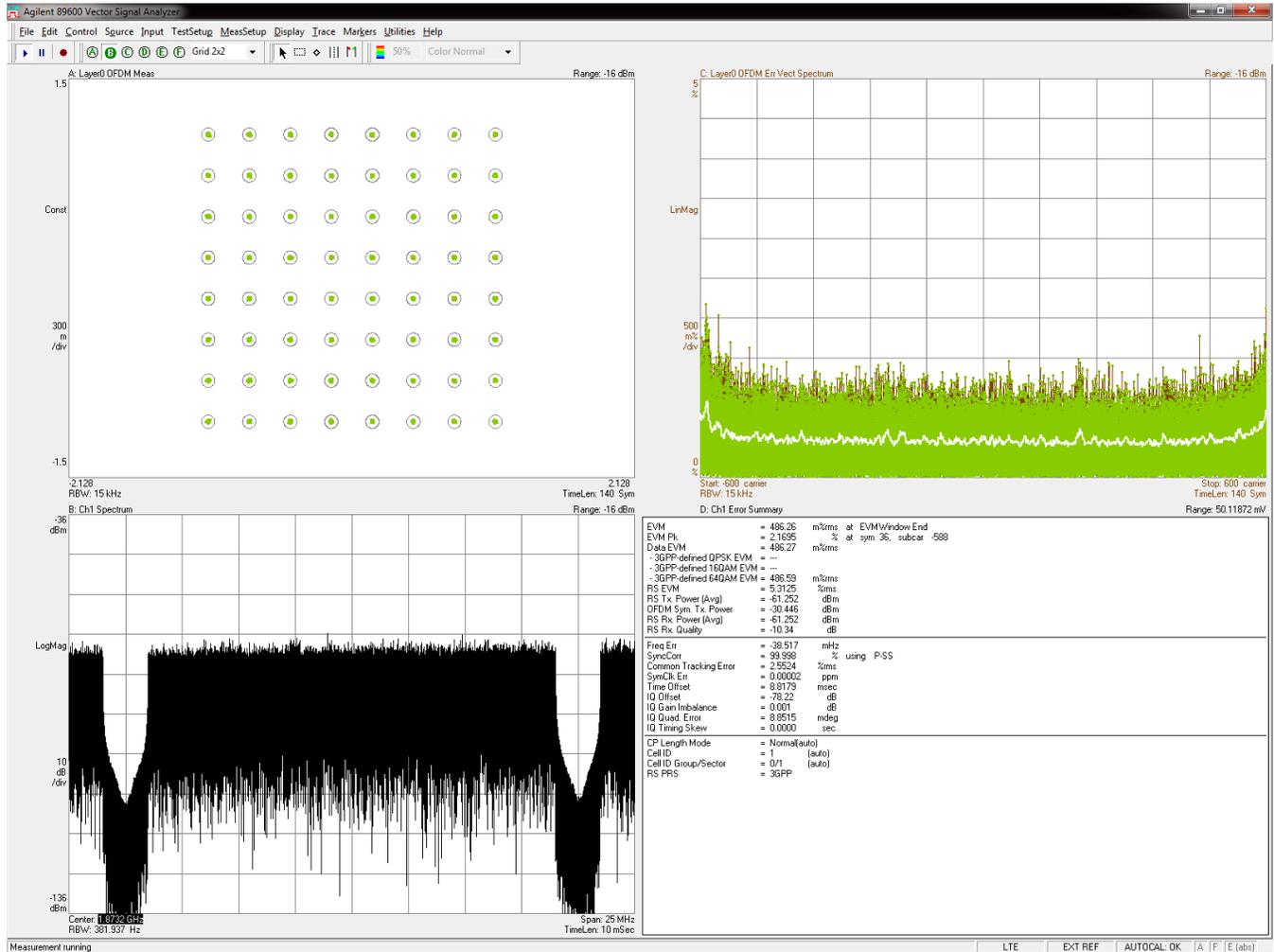
Figure 9. Measured EVM (0.49%) at 1.8732 GHz

Figure 10 shows measured Error Vector Magnitude (EVM) from the carrier located 2.2332 GHz, which is 0.52%. The baseband LTE pattern is directly up-converted to 2.1432 GHz by NCO.
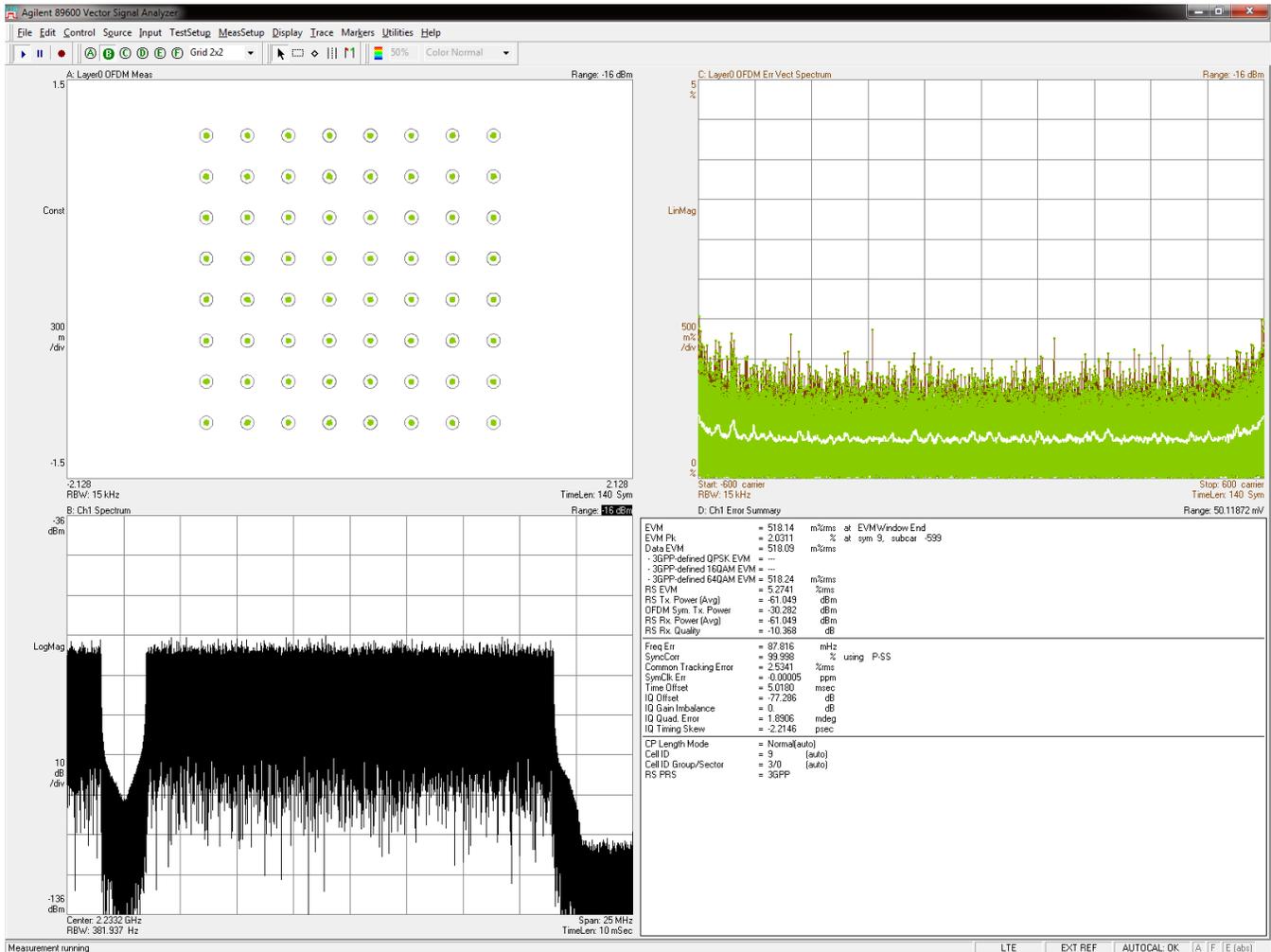
Figure 10. Measured EVM (0.52%) at 2.2332 GHz

3 Conclusion

The 800 MHz of IBW from DAC38RF8xEVM shows a good ACLR performance, –55.55 dBc, with a good flatness. The measured Error Vector Magnitude (EVM) shows around 0.5% from the up-converted modulated LTE carriers without the need of Quadrature Modulation Correction (QMC). Signal quality wise, baseband signal is up-converted to RF domain directly through RF sampling method, and therefore, there is no I/Q impairment, which give us a good EVM performance.

The next generation (5G) cellular system demands much wider bandwidth than fourth generation (4G) Long Term Evolution (LTE). DAC38RF8x shows a capability to handle 800 MHz of IBW pattern while maintaining good signal qualities in this document, and therefore, DAC38RF8x could be a good candidate for 5G related technologies.

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