Application Report
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Optimizing Signal Chain Noise on PCM186x Devices

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ABSTRACT

The PCM1860/1/2/3/4/5 devices have a highly flexible input front end that can handle very low level single ended, pseudo-differential and higher voltage differential inputs. The architecture of the PCM186x family of devices allows system designers to optimize the signal chain to avoid any increased noise floor, depending on how they have their system configured.

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1 Introduction

The PCM186x family has a highly flexible input structure allowing the device to support single ended, differential and psuedo-differential inputs. Some customers can use the Single Ended input mode to support a 2 VRMS Audio source (such as a DVD player), others may choose to use the Psuedo-Differential modes ground noise cancellation and for others, fully differential modes are used, with an input swing of 4.2 VRMS differential.

The PCM186x was designed to handle all of these input conditions, and to support a programmable gain amplifier that can boost or attenuate the signal as needed.

As the Pseudo-Differential mode (signal on positive input, ground sense on the negative input) doesn't exercise the entire range of the ADC, the architecture was designed so that lower input voltages could achieve higher Signal to Noise Ratio. The architecture was defined, so that at typical lower signal amplitudes, the ADC would provide higher performance, whilst at very high amplitudes (within -2 dBFS of ADC input) the noise floor would be allowed to increase.

2 Explanation

The ADC was designed to support maximum input signals that may be as low as 1 VRMS in differential mode all the way to a full 4.2 VRMS differential. Given market trends towards portable products connecting through AUX inputs to docks, amplifiers and AV systems, more emphasis was put on increasing sensitivity and noise floors at lower ranges, than full dynamic range.

The internal architecture of a delta sigma ADC (in this case the PCM186x) is shown in Figure 1.

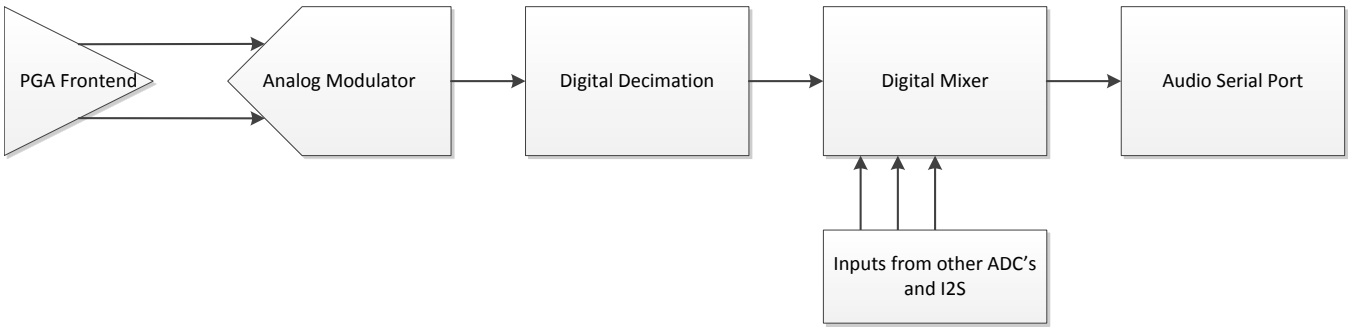

Figure 1. ADC Signal Chain Architecture of PCM186x

The modulator is the high speed oversampling converter who's data is passed to a decimator that converts the high speed multi-bit data to a lower rate 24 bit data stream. The modulator has an analog input range defined as a "modulation index" between 0 and 100%. The noise floor is not linear between 0 and 100% and silicon designers typically have to scale their analog inputs so that the maximum expected analog input lies within the flat noise floor. This is typically between 0 and ~95% modulation. Any higher can cause a noise floor that increases.

On PCM186x, given the large variance of "maximum input signal" and the availability of the PGA, we offer the capability to tune the maximum modulation index to improve performance at lower ranges, or push the signal as high as possible, even at the sacrifice of some noise floor.

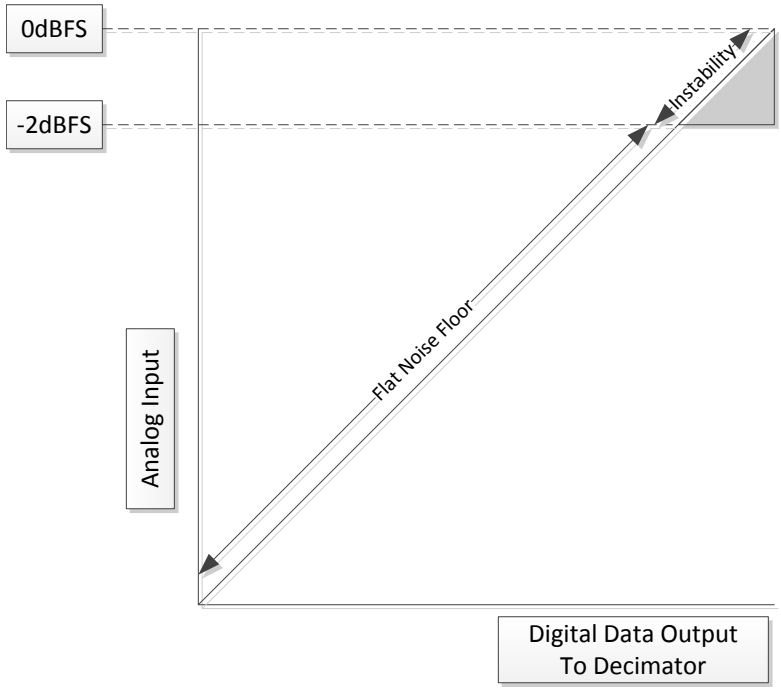

Figure 2. Input vs Output graph of a Delta Sigma Modulator

3 Sensitive Configurations

The noise floor will begin to increase when the post-PGA output is within -2 dB of the modulator full scale input (defined as 2.1 VRMS in single ended mode and 4.2VRMS in differential mode). The PCM186x PGA maps the incoming voltage to the ADC differently based on the input configuration.

3.1 Single Ended Systems

If using the system with 2.1 VRMS Single Ended Inputs, then there is a possibility that any signals over ~1.65 VRMS can cause noise modulation. Systems in single ended configurations expecting 1 VRMS input (e.g. from a smartphone) do not have noise modulation, providing their PGA gain is configured to be less than 4 dB. This can be compensated for either using attenuation in the analog PGA, or external signal conditioning. (see Section 4)

3.2 Differential Systems

Differential systems require a 3.34 VRMS differential signal before any kind of noise modulation can occur (that is -2 dB below 4.2 VRMS). Again, this can be compensated for using the PGA if the input signal really is 4.2 VRMS.

3.3 Psuedo-Differential Systems

Pseudo Differential systems, expecting a 1 VRMS or 2.1 VRMS single ended signal, along with a "grounded" input are not impacted. Even with a 2.1 VRMS input on the positive pin, the modulator, by default will see data at -6 dBFS. No more analog gain can be added to such systems, as the each input of the device has a voltage limit of 2.1 VRMS. The PGA will clip before the modulator will clip.

4 Configurations to avoid noise modulation

When working in single ended input modes (for example 2 VRMS Single Ended Mode) the recommended configuration is to limit the output of the PGA to the modulator. This can be achieved in software programmable devices (PCM1862/3/4/5), by configuring the PGA to -2 dB gain below what would be required to clip the ADC. The decimator then outputs data that is -2 dBFS. This can be compensated for in the digital mixer by adding 2 dB of gain, to bring the full scale analog signal to be fullscale of the I2S stream. The 4 channel PCM1864 and PCM1865 can have their analog and digital PGA's controlled separately, as such, the 2 dB gain can be done in the Digital PGA instead of the digital mixer.

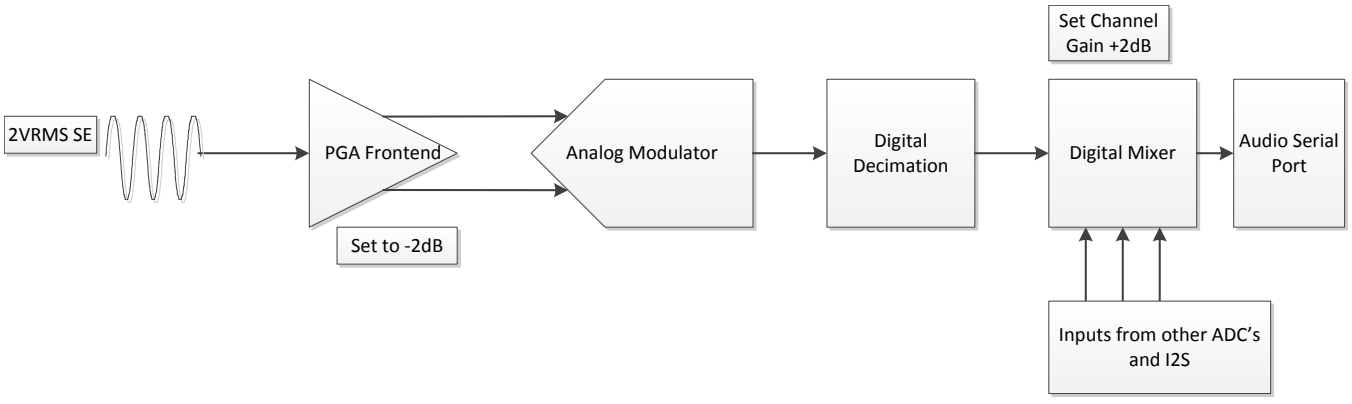

Figure 3. SW Controlled Compensation to Ensure 2.1 VRMS Inputs Avoid Noise Modulation

For hardware controlled devices (PCM1860/1), a resistor is recommended to be used to lower the input voltage to the device. The input impedance of the PCM1860/1 is nominally 20 KΩ but can vary ±20% due to manufacturing tolerance. -2 dB attenuation requires a ~5.2-KΩ resistor. Input voltage control can also be done using a standard voltage divider on the input. Designers should consider the 20 KΩ input impedance when designing their voltage divider.

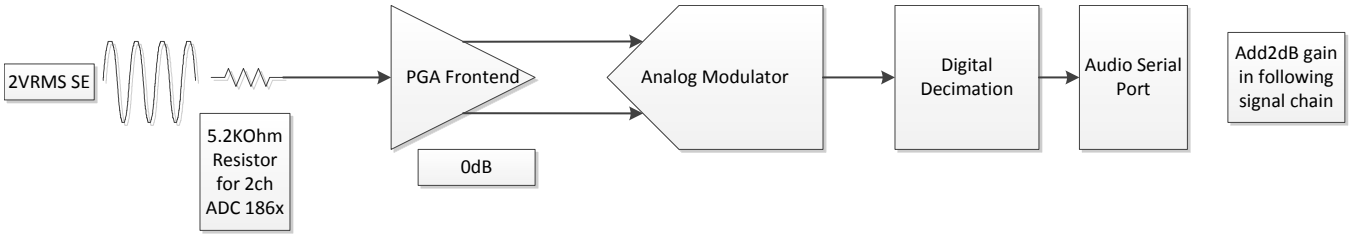

Figure 4. HW Controlled Compensation to Ensure 2.1 VRMS Inputs Avoid Noise Modulation

Analog performance with attenuated modulator inputs

With the modulator now running 2 dB below full scale, the performance of the higher grade PCM1861/3/5 will be impacted to 108dB Differential. The low grade PCM1860/2/4 remains at 103 dB.

5 Impacts on Additional Features in the PCM186x Family

The PCM186x family, especially those which are software controlled have a number of features that can assist with configuring the input signal chain

5.1 Energysense

This noise floor at high input has no impact on the Energysense system wake and system sleep detection. However, if the PGA gain is modified, then signal thresholds is 2 dB lower. For example, a if the signal wake up threshold was set to -50dBFS previously, it will now take a -48 dBFS to wake the system.

5.2 Auto Gain Suppression and Clipping detection

Once the PGA gain has been compensated with -2 dB gain the modulator will receive reduced input levels. The Auto Gain Suppression and Clipping Detection requires compensation for the attenuation that has been added to signal before the modulator.

A real world application would be an Aux system expecting 1 VRMS inputs from a smartphone in most cases, but still needs the ability to accept a 2.1 VRMS input, should a customer decide to connect a DVD player. Designers can use the Auto Gain Suppression feature to optimize the input signal at all times.

The application Figure 5 configures the device for 1 VRMS input SE, but responds to a 2.1 VRMS input by automatically attenuating the signal to full scale. An additional -2 dB of attenuation is added to maintain the flat noise floor.

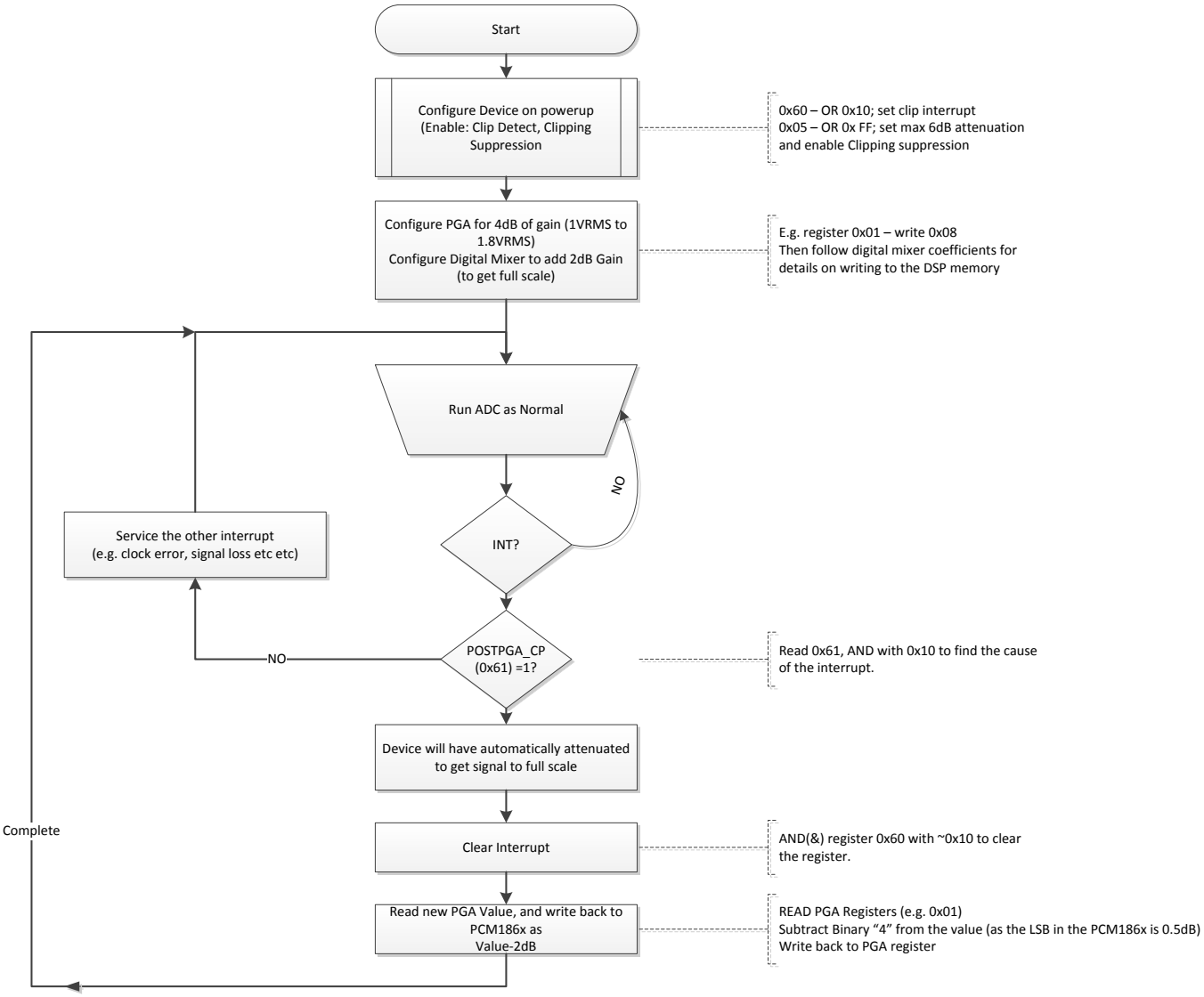

Figure 5. Workflow to Use Auto Gain Suppression With a -2 dBFS Input Signal

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