Application Report
SLAA624A–May 2014–Revised March 2016

Designing With MSP430FR58xx/FR59xx/68xx/69xx ADC

William Goh and Christy She

ABSTRACT

Designing an application with the analog-to-digital converter (ADC) requires several considerations to optimize for power and performance. This application report discusses the basics of how you would analyze a data sheet and user's guide to design your application. It goes into the fundamentals of how to optimize your design based on the external requirements and available ADC configurations. The goal is to consider various ADC parameters before writing a single line of code. This helps to avoid any unnecessary design changes down the path.

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1 ADC Overview – ADC12_B

MSP430FR58xx/FR59xx/68xx/69xx devices use a new class of 12-bit ADC12_B. The lists of features for the ADC12_B are the following:

- 200-ksps maximum conversion rate at maximum resolution of 12 bits
- Operates across the entire voltage range of the device (1.8 V to 3.6 V)
- Lowest-power 12-bit ADC in the MSP430™ MCU product portfolio
- Supports up to 32 single-ended external input channels. These can be combined to form external differential input channels or any combination in between.
- Window Comparator that allows you to set threshold levels and compare conversion results to the thresholds without any CPU intervention
- Option to enable 8-bit, 10-bit, or 12-bit conversion
- Requires 10, 12, or 14 ADC12CLK clock cycles for sample conversion at 8-bit, 10-bit, or 12-bit resolutions, respectively

- An option to save power at reduced clock rates, 1/4 the maximum using the ADC12PWRMD bit in the ADC12_B Control 2 Register (ADC12CTL2)

ADC12_B is highly configurable into various modes for best performance in your application. By default, ADC12_B is configured as a single-ended input mode converter in which all analog input signals are referenced to AVSS. ADC12_B also supports a differential input mode, which should be selected for differential signals and can also be used for single-ended signals by tying the negative input to AVSS. The advantage of using differential mode for a single-ended input is noise rejection with the cost of a small increase in current consumption. Set the ADC12DIF bit in the ADC12_B Conversion Memory Control x Register (ADC12MCTLx) to enable differential mode. Overall the same principles for designing with the ADC apply to differential and single-ended input modes.

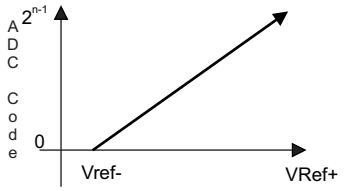
NOTE: Before proceeding, familiarize yourself with the *ADC12_B and Reference Voltage* chapter from the *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide* (SLAU367) [1].

2 Tailoring the ADC and Reference Voltages to Your Application

Each application is unique and has different reference voltage considerations. As an example, when connecting a sensor to the ADC front-end, you would need to consider the voltage dynamic range, the sensor settling time, powering and disabling the sensor when needed for an energy optimized application. Once the considerations are understood, the ADC12_B reference can be tailored for various applications through the configuration registers. Consideration areas for the reference voltage are described in this section.

2.1 Reference Voltages

A reference voltage is a fixed voltage that ideally should not have any temperature and supply dependent variations. ADCs require a reference voltage that has a negative and positive side as a reference point for the ADC input signal. It then translates the input signal to a digital value (ADC code) based on the signal relative to the reference voltage. The application code then deciphers the ADC code in reference to the input signal voltage. Figure 1 showcases a linear translation graph of a reference voltage to an ADC code.



n = No of ADC bits

Figure 1. Input Signal Voltage vs ADC Code

The maximum ADC code value is calculated by (2^n - 1) where n is the number of ADC resolution bits. The positive side of the reference voltage translates to the highest ADC code. If an input signal is higher than the reference voltage, the measurement is then saturated to the maximum ADC code value. For example, if the ADC is 12 bits, the maximum ADC code is (2^{12} – 1) = 4095 injecting a voltage above the device specification into the ADC pins can cause permanent damage to the pin or the device itself. For more information, see the data sheet parameter on analog input voltage range. For measuring voltages that exceed the input range of the ADC an external resistive voltage divider can be used.

2.1.1 Internal vs External Reference Voltage

All MSP430 ADCs have integrated internal reference voltages. The ADC also allows external references to be attached if the internal reference performance is not sufficient or if an alternate reference voltage is required. Deciding between internal and external reference needs to be determined early in the design cycle by considering the various conditions of the application. If the reference voltage is used to source multiple devices or external sensors, consider the current load. The MSP430 reference voltage output can only handle a maximum load as stated in the data sheet. The MSP430FR58xx/FR59xx/68xx/69xx reference module can generate three selectable internal reference voltages, 1.2 V, 2.0 V, 2.5 V. AVCC is also a selectable reference voltage. Using AVCC as a reference is lower power, however, it measures analog voltages ratiometric to a potential imprecise and changing AVCC voltage. For some applications, this may be exactly what is desired (for example, measuring full-bridge sensors that are also powered by AVCC).

2.1.1.1 Load Dependency

Sourcing an external device or sensor through the reference voltage is not recommended if care is not taken for proper design specification. The internal reference output buffer has limited drive strength capability. If the current drive is exceeded, the ADC and reference performance could be severely affected resulting in false measurements. Consider using an external reference voltage to source your external sensor and as an external reference voltage to the MSP430FR58xx/FR59xx/68xx/69xx device.

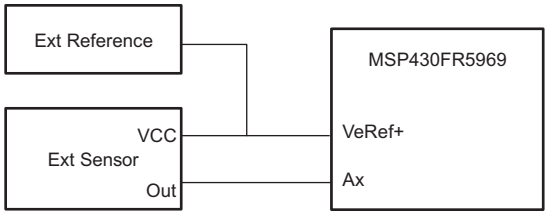


Figure 2. Example of an Analog Sensor Powered From a Dedicated LDO

Figure 2 shows an example on how a sensor could be powered and connected to the ADC for best analog performance. Deciding how the external sensor is powered based on its power requirements is critical for optimal analog performance.

2.1.1.2 Temperature Drift

Another factor that could affect the reference voltage is the dependence on temperature. The reference voltage temperature drift is located in the device-specific data sheet. If an application is in an environment with large temperature swings and accuracy is required over the entire temperature range, evaluate if the internal reference temperature coefficient is good enough. If not, consider using one of Texas Instrument's external reference solutions with a low temperature coefficient and connect use the VeREF+ pin on the MSP430.

2.1.1.3 Analog Reference Voltage Offset

Another consideration between internal vs external reference is the analog reference voltage offset. All internal references have a voltage offset that needs to be taken into consideration and TLV calibration data can be used to reduce this. For more information, see Section 4. However, using an external reference voltage for the ADC would have a smaller voltage offset relative to the internal reference. The external reference may also be calibrated to obtain the closest reference voltage target. Provide some headroom when selecting the right reference voltage for the application so that the signal is not saturated during conversion or the signal attenuated.

2.1.2 Signal Resolution

Signal resolution determines how accurate a signal can be measured when translated into a digital value since the digital value is finite. The smaller the signal resolution, the better the signal accuracy one can capture. Signal resolution is calculated based on the ADC reference voltage and the number of ADC bits. First, determine your input signal voltage peak-to-peak. Then, select the smallest reference voltage larger than the peak voltage to be captured. This provides the finest signal resolution when calculating it in code. Signal resolution can be calculated using Equation 1.

$$Signal\ Resolution = \frac{V_{R+} - V_{R-}}{2^n},\ n = ADC\ conversion\ resolution \tag{1}$$

Assuming VREF+ = 2.5 V and VREF- = 0 V and *n* is 12 bits, the signal resolution can be calculated using Equation 2.

$$Signal\ Resolution = \frac{2.5\ V}{2^{12}} = \frac{2.5\ V}{4096} = 610\ \mu V / bit \tag{2}$$

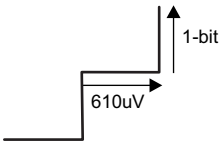


Figure 3. Signal Resolution

As an example, if your sensor output swings between 0 V to 1.8 V and you want to use the internal reference, you would select the reference voltage of 2 V. This allows the input signal to not saturate the ADC while providing the finest resolution.

Based on the signal resolution, you can calculate the ideal ADC code from the input voltage. To calculate the ADC code, assuming VREF+ is 2.5 V, 1 V input voltage and 12 bits of resolution, the following formula where Equation 1 has been solved for the signal applies.

$$ADC\ Code = \frac{Input\ Voltage}{Signal\ Resolution} = \frac{1V}{610\ \mu V / bit} = 1638 \tag{3}$$

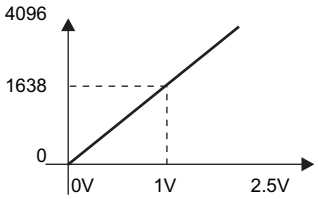


Figure 4. Input Signal to ADC Code

2.1.3 Noise Consideration

Hardware layout is critical for achieving the best ADC performance. The power supply and VREF capacitors should be designed per the user's guide [1] recommendation and properly routed.

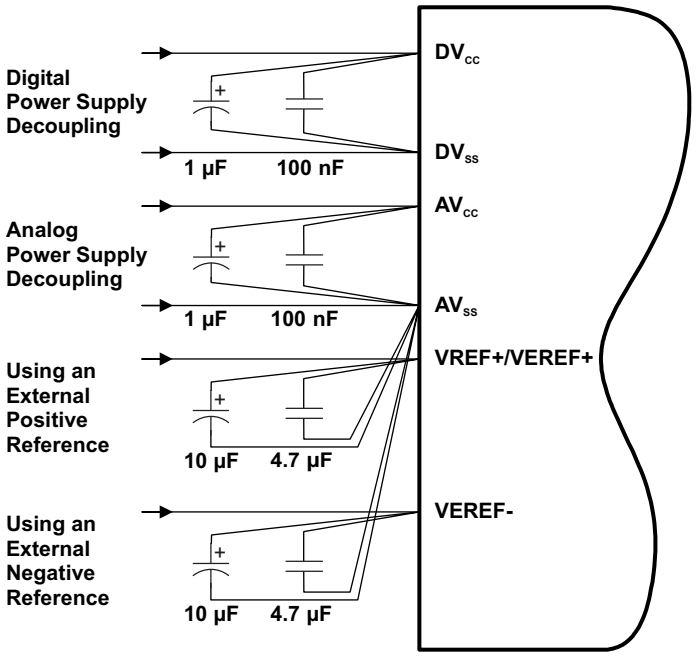


Figure 5. ADC12_B Grounding and Noise Considerations

2.1.3.1 Reference Noise

For the best ADC performance consideration, minimizing noise on the reference should be a priority. Some noise on the reference voltage is white noise and averaging the ADC results in software helps reduce its effects.

Other noise on the internal reference voltage is low frequency and random in time. It can be hard to quantify on-bench measurements but it can affect ADC performance of the MSP430FR58xx/FR59xx/68xx/69xx devices. Averaging and filtering do not help with this type of noise. In certain performance critical application the use of a specialized external precision voltage reference will help achieve better analog system performance. For more information, see the Texas Instrument's external reference page.

When an external reference is used, or the internal reference is used and REFOUT=1, the decoupling caps should be placed as close to the pin as possible to minimize noise. Suggested decoupling cap values are provided in the data sheet [2] and PCB layout advice is provided in the *ADC12_B* chapter of the user's guide [1] and also Figure 5.

2.1.4 More Resources on Voltage Reference Affecting ADC Performance

- *Journal - How the voltage reference affects ADC performance, Part 1* (SLYT331)
- *Journal - How the voltage reference affects ADC performance, Part 2* (SLYT339)
- *Journal - How the voltage reference affects ADC performance, Part 3* (SLYT355)

2.2 Selecting the Right Sample-and-Hold Time (SHT)

Sample-and-hold time determines how long to sample a signal prior to digital conversion. During sample time, an internal switch allows the input capacitor to be charged. The required time to fully charge the capacitor is dependent on the external analog front-end (AFE) connected to the ADC input pin. Figure 6 demonstrates a typical ADC model of an MSP430. The R_I and C_I value can be obtained from the device-specific data sheet.

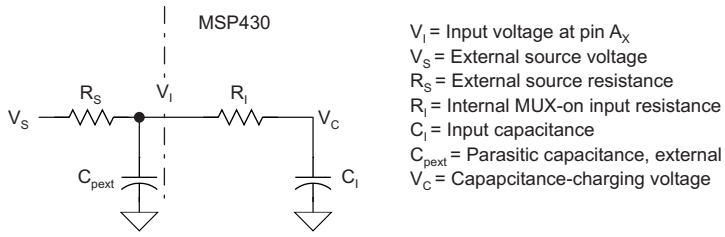


Figure 6. Analog Input Equivalent Circuit

It is critical to understand the AFE drive capability. If possible, model the AFE as depicted in Figure 6. Once known, calculate the minimum sample-and-hold time required to sample the signal based on Equation 4 from the *MSP430FR59xx, MSP430FR58xx, MSP430FR68xx, and MSP430FR69xx User's Guide* [1].

$$t_{sample} \geq (R_S + R_I) * ln\left(2^{n+2}\right) * (C_I + C_{pext}), R_S < 10\ k\Omega \tag{4}$$

Once the minimum sample-and-hold time is calculated, the appropriate settings for the ADC can be determined including selecting the right ADC clock. The key goal is to optimize the sample-and-hold time to your application. If the sample-and-hold time is excessively longer than required, it is a waste of energy for the ADC to be operational during that period of time. The sample-and-hold time will also limit the maximum sample rate. If your application requires a larger sample and hold time than the minimum, there will be a tradeoff between performance and maximum sample rate.

The following is an example of an external sensor with the assumption that it can be modeled with R_s = 1kΩ and C_{pext} = 1 nF.

R_I = 1k Ω (see [2])

C_I = 10 pF (see [2])

R_s = 1k Ω

C_{pext} = 100 pF

t_{sample} ≥ (1k Ω + 1k Ω) * ln 2^{12+2} * (10 pF + 100 pF)

t_{sample} ≥ 2.1 µs

If the ADC12CLK is at 4.8 MHz, the minimum required sample-and-hold time would be as shown below:

SHT = 2.1 µs * 4.8 MHz ≈11 cycles

The next closest sample-and-hold time (ADC12SHTx) would be 16 ADC12CLK cycles according to the *MSP430FR59xx, MSP430FR58xx, MSP430FR68xx, and MSP430FR69xx User's Guide* [1]. This value would be the most efficient to enable full ADC performance for this application example.

A C-code example implementation would look something like the following.

```
  ADC12CTL0 = ADC12SHT0_2 | ADC12ON;        // Sampling time, S&H=16, ADC12 on
  ADC12CTL1 = ADC12SHP;                     // Use sampling timer
  ADC12CTL2 = ADC12RES_2;                   // 12-bit conversion results
  ADC12MCTL0 |= ADC12INCH_1;                // A1 ADC input select; Vref=AVCC
  ADC12IER0 |= ADC12IE0;                    // Enable ADC conv complete interrupt
```

If none of the pre-fixed sample-and-hold time works, the timer could be used to trigger the sample-and-hold time for the extended period of sampling (ADC12CTL1.ADC12SHP). The following C-code example demonstrates the use of a Timer triggering the ADC12_B.

```
    // Configure ADC12
    ADC12CTL0 &= ~ADC12ENC;                 // Disable ADC12
    ADC12CTL0 = ADC12SHT0_2;                // Configure sample and hold time for 16 ADCCLK
cycles
    // ADCCLK = MODOSC; sampling timer, trigger from TA0.1, repeated single channel
    ADC12CTL1 = ADC12SHS_1 | ADC12SHP | ADC12CONSEQ_2;
    ADC12CTL2 = ADC12RES_2 | ADC12PWRMD;    // 12-
bit conversion results + low power mode since we're sampling at 1 sample/sec
    ADC12IER0 |= ADC12IE0;                  // Enable ADC conv complete interrupt
    ADC12MCTL0 |= ADC12INCH_2;              // A2 ADC input select
    ADC12CTL0 |= ADC12ON;

    // Use TimerA0.1 to trigger the ADC periodically at 100Hz
    TA0CCR0 = 32767;                        // 32768
    TA0CCR1 = 3276;                         // 10% duty cycle
    TA0CCTL1 = OUTMOD_7;                    // set/reset mode
    TA0CTL =  TASSEL_1 | MC_1;              // ACLK, Up mode
```

As a note, if the internal reference is used, ensure it is ready before any sampling is performed. The ready state of the voltage reference can be checked via the REFCTL0.REFGENRDY bit.

2.3 Clock Selection

ADC12_B requires a clock source to convert the sampled analog input pin to an ADC code. This step occurs after the sample-and-hold period as discussed in Section 2.2. If ADC12SHP=1, clock source is also needed to generate the sample-and-hold time from the internal ADC sample timer. Four clock sources can be selected for ADC12_B: MODOSC, ACLK, MCLK, and SMCLK. MODOSC is an internal clock source that is automatically enabled once requested by the ADC12_B module. There is also a clock divider that can be configured to lower the frequency. The clock source selection directly correlates to the system sampling rate. The slower the ADC12 clock, which reduces power consumption, the slower the sampling rate. Keep in mind that the ADC12_B maximum sampling rate is 200 ksps.

Another power saving feature is to use the ADC12PWRMD bit if the clock is < = 1/4 the specified maximum.

3 Window Comparator to Monitor Signal Without CPU Intervention

The window comparator has the capability to set threshold levels and compare conversion results to the thresholds without any CPU intervention during low-power modes (LPM). The thresholds are set in LSB units and if a conversion result falls within the range of pre-set low and high threshold levels, an interrupt is triggered. Note that the same window comparator thresholds are shared among all channels, and conversion results from different channels are compared against the same threshold levels when the feature is enabled.

This feature is extremely useful for saving power, because it allows the device to stay in a LPM until the ADC input reaches a specific threshold. All other conversion results are discarded automatically, and the device only wakes up on threshold triggers.

The following is a C-code example snippet on enabling the window comparator in ADC12_B.

```
#define High_Threshold 0xCCC         // ~2V
#define Low_Threshold  0x666         // ~1V

...

  // Configure ADC12
  // tsample = 16ADC12CLK cycles, tconvert = 14 ADC12CLK cycles
  // software trigger for SOC, MODOSC, single ch-single conversion,
  // tsample controlled by SHT0x settings
  // Channel 1, reference = internal, enable window comparator
  // Set thresholds for ADC12 interrupts
  // Enable Interrupts
  ADC12CTL0 = ADC12SHT0_2 | ADC12ON;
  ADC12CTL1 = ADC12SHS_0 | ADC12SSEL_0 | ADC12CONSEQ_0 | ADC12SHP;
  ADC12MCTL0 = ADC12INCH_1 | ADC12VRSEL_1 | ADC12WINC;
  ADC12HI = High_Threshold;
  ADC12LO = Low_Threshold;
  ADC12IER2 = ADC12HIIE | ADC12LOIE | ADC12INIE;

  // Configure internal reference
  while(REFCTL0 & REFGENBUSY);              // If ref generator busy, WAIT
  REFCTL0 |= REFVSEL_2|REFON;               // Select internal ref = 2.5V
                                            // Internal Reference ON
  while(!(REFCTL0 & REFGENRDY));            // Wait for reference generator
                                            // to settle
```

4 Calibration to Improve Performance

Calibration can be done to improve ADC performance. Real-time calibration provides the best performance as it accounts for temperature drift and voltage dependencies, but it can require additional hardware on the board. During production, measurements can be done specific to the application and those calibration values stored, and later used by the code to calibrate. The device also contains some calibration values pre-programmed by Texas Instruments that can be used to improve performance. These values are stored in the Device Descriptor Table (TLV). The device-specific data sheet shows the TLV calibration values available on the device and the correction equations are provided in the *Device Descriptor Table* section in [1]. To calibrate using TLV values, the code needs to implement the correction equations.

If the internal reference is used, the reference factor can be used to know the exact reference voltage at room temperature. More details on this procedure are provided in the *Device Descriptor Table* section of the user's guide [1].

The ADC has a gain factor and offset stored in TLV that is pre-programmed on the device based on measurements using an external reference at room temperature. When the calibration equations are applied, gain and offset error are improved as well as total unadjusted error. At room temperature, gain and offset error will be improved to ±0.5 LSB. Note the gain factor TLV value is measured with an external reference without internal buffer ADC12VRSEL = ADC12VRSEL_2, ADC12VRSEL_4, or ADC12VRSEL_14. Other settings (for example, using internal reference) can result in different correction factors. For obtaining the offset, TLV value is measured with ADC12VRSEL = ADC12VRSEL_2 or ADC12VRSEL_4 and VR+=2.5V and VR-=AVSS. Other settings can result in a different correction factor. As voltage drop increases on AVSS, the offset would increase and not be accounted for in the TLV value.

5 ADC12_B Example Code and Resources

- For more comprehensive code examples on using the ADC, see *MSP430FR59xx, MSP430FR58xx Code Examples* (SLAC536).
- EnergyTrace++ technology offers an advance approach in debugging and optimizing your application power consumption by observing various aspects of the code and its power consumption. To use EnergyTrace++ Technology, see MSP430 Advanced Power Optimizations.
- *MSP430 Advanced Power Optimizations: ULP Advisor and EnergyTrace Technology* (SLAA603)
- For a complete online training workshop, see the MSP430FR59xx Training Workshop wiki.

6 References

1. *MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide* (SLAU367)
2. *MSP430FR59xx, MSP430FR58xx Mixed Signal Microcontroller Data Sheet* (SLAS704)
3. *MSP430FR59xx, MSP430FR58xx Code Examples* (SLAC536)
4. MSP430 Advanced Power Optimizations
5. *MSP430 Advanced Power Optimizations: ULP Advisor and EnergyTrace Technology* (SLAA603)
6. For a complete online training workshop, see the MSP430FR59xx Training Workshop wiki.
7. *Journal - How the voltage reference affects ADC performance, Part 1* (SLYT331)
8. *Journal - How the voltage reference affects ADC performance, Part 2* (SLYT339)
9. *Journal - How the voltage reference affects ADC performance, Part 3* (SLYT355)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2014) to A Revision	Page
• Update was made in Section 2.2.	6

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