Application Report
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An Introduction to the ADS7863A

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ABSTRACT

This application note presents an introduction to the ADS7863A; a dual, 12-bit, 2x2 or 3x3 channel, simultaneous sampling analog-to-digital converter (ADC). The ADS7863A is an updated version of the ADS7863 with a higher degree of flexibility in the digital interface to the chip. This application note compares and contrasts the changes to the ADS7863 and provides some application tips and tricks to successfully implement the ADS7863A in new or existing designs.

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1 Introduction

The ADS7863A is configurable as a 2x2 channel (four fully-differential inputs) or 3x3 channel (six pseudo-differential inputs), simultaneously sampling 12–bit ADC, capable of sampling at rates up to 2MSPS. The inputs are grouped in two pairs, A and B, with independent sample and holds followed by two independent ADC channels. The conversion results are then presented via two serial data output lines for operation at full speed. For applications utilizing one serial bus, the ADS7863A can be configured to use a single serial output for both A and B channel conversion results. To ease the identification of conversion data, channel ID bits are inserted into the conversion results starting with the first two serial clocks applied to the ADS7863A.

As with the original ADS7863, control of the serial outputs and sampling scheme are accomplished by using dedicated MODE pins, M0 and M1. The Table 1 shows the pin state with the resultant channel selection method and serial output(s) used.

Table 1. Pin State and Channel Selection Method

Mode	M0 Pin	M1 Pin	Channel Selection	SDOx Used
I	0	0	Manual (via serial data input commands)	SDOA and SDOB
II	0	1	Manual (via serial data input commands)	SDOA only
III	1	0	Automatic sequencing	SDOA and SDOB
IV	1	1	Automatic sequencing	SDOA Only

There are also two special modes associated with Mode II and Mode IV (SMII and SMIV). These special operating modes allow both channel conversion results to be read out of the ADS7863A with a single RD impulse.

As with the ADS7863, the ADS7863A also helps simplify the identification of channel conversion data by outputting two bits ahead of the conversion results. The following table represents the serial data output format.

Table 2. Serial Data Output Format

Clock Cycle	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
SDO	CH0/1	CHA/B	DB11	BD10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	BD0	0	0

2 ADS7863 versus ADS7863A

Depending on the mode setting of the original ADS7863, the width and timing of the RD signal could cause unexpected behavior in the serial output data. Corrupted data, repeated data, or the swapping of channel number and pair bits were observed. The following sections describe this in more detail.

2.1 ADS7863 RD Width

Table 3 describes the observed anomalies depending on the width of the RD signal of the original ADS7863.

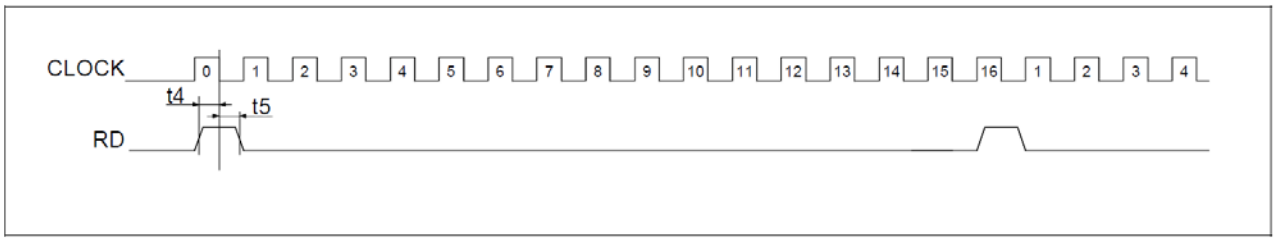
Table 3. RD Signal Anomalies

Mode	Maximum Length of RD	What happens if RD is longer?
I	Max 16 clocks	A second transfer is initiated
II	Max 2 clock periods	ADC bit is inverted if RD falls before EOC. Data is corrupt when RD falls within data output, that is, after 4 clocks. No data comes out when RD is falling after EOC.
III	Max 1 clock period	If RD is falling after 2 clocks, the channel info bits are swapped. If RD is

		falling after LSB, data is corrupt.
IV	Max 1 clock period	If RD is falling after 2 clocks, only the channel bit of A is inverted. If RD is falling after 3 clocks, the A channel bit and the ADC bits are inverted. The channel bit of B is correct. Data is corrupt when RD falls within data output, that is, after 4 clocks. No data comes out when RD is falling after EOC.
SMII	Max 32 clocks	A second transfer is initiated
SMIV	Max 1 clock period	If RD is falling after 2 or 3 clocks, only the channel bit of A is inverted. If RD is falling after 18 clocks (during channel bit of B), both channel bits are inverted.

2.2 ADS7863 RD Timing

The timing of the RD signal is described relative to the falling clock edge with 10 ns (t4) setup time and 5 ns (t5) hold time. In synchronous serial systems, such as the multi-channel buffered serial port (McBSP) of the TMS320 series processors, meeting the setup and hold requirement minimums are possible. After the introduction of the ADS7863, however, it was discovered that an additional 4 ns delay before the next rising serial clock was necessary. The information in Figure 1 describes the required timing of the RD pulse.



SYMBOL	PARAMETER	COMMENTS	ADS7863		UNIT
			MIN	MAX	
t_4	RD high setup time to CLOCK falling edge	See figure above	10		ns
t_5	RD high hold time to CLOCK falling edge	See figure above	5	t_{CLOCK}/2-4	ns

Figure 1. Required Timing of the RD Pulse

3 Application Tips and Tricks with the revised ADS7863A

With the release of the ADS7863A, the issues noted above have been addressed and the original ADS7863 has been placed on the Not Recommended for New Designs (NRND) list. Existing applications using the ADS7863, with the timing restrictions noted in section 2.2 above, will not be impacted by using the ADS7863A. Designs which use the ADS7861 will find it easier to upgrade to the ADS7863A as well.

Applications that remapped any swap in channel ID bits must revise the codes associated with the ADS7863A to correctly store the channel data. For additional support on the ADS7863 or the ADS7863A, please contact us through the Precision Data Converter Forum.

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