Design Considerations for Avoiding Timing Errors during High-Speed ADC, LVDS Data Interface with FPGA

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ABSTRACT

This application note describes the design considerations for designing the LVDS interface between the ADC and FPGA. It also provides details on LVDS Data Standards. LVDS (Low Voltage Differential Signaling) is a more widely accepted standard for ADCs digital data output along with LVCMOS. Timing analysis of LVDS data capturing into FPGA is beneficial to engineers who design with the ADC and FPGA interface. Even though this application note analyzes the LVDS interface, with few modifications, this timing analysis can be applied to other differential standards.

Contents

1 Introduction to LVDS

1.1 What is LVDS?

The LVDS (Low Voltage Differential Signaling) Standard is a popular differential data transmission standard in the industry. LVDS is two-wire, low-swing differential signaling. The major benefits include the following:

- Possibility of low supply voltage operation
- High speed data transfer
- Good common mode noise rejection
- Less noise generation

The application of the LVDS technique is for baseband data transmission over controlled impedance media of 100 Ω, where the transmission media may be PCB traces, backplanes, or cables. LVDS outputs consist of a current source of approximately 3.5 mA which drives the differential pair. The LVDS receiver has high DC input impedance; therefore, the majority of the LVDS driver current flows across the 100-Ω termination resistor generating about 350 mV across the receiver inputs.

1.2 LVDS Standard

The ANSI/TIA/EIA-644-A (LVDS) standard shown in Table 1 defines LVDS signaling. This standard defines driver output and receiver input characteristics and it is an electrical-only standard. It does not include fundamental specifications, protocols or even complete cable characteristics, since these are application dependent. ANSI/TIA/EIA-644-A is intended to be referenced by other standards that specify the complete interface, that is, connectors and protocol. This allows easy adoption into many applications and also allows the referencing standard to specify the maximum data rate required, depending on the required signal quality and media length or type.

Table 1. ANSI/TIA/EIA-644(LVDS) Standard

Parameter	Description	Min.	Max.	Units
V_{OD}	Differential output voltage	247	454	mV
V_{OS}	Offset voltage	1.125	1.375	V
V_{OD}	$|$Change to $V_{OD}|$		50	$|$mV$|$
V_{OS}	$|$Change to $V_{OS}|$		50	$|$mV$|$
I_{SA}, I_{SB}	Short circuit current		24	$|$mA$|$
tr/tf	Output rise/fall times (200 Mbps)	0.26	1.5	ns
	Output rise/fall times (<200 Mbps)	0.26	30% of tui†	ns
I_{IN}	Input current		20	$|$μA$|$
V_{TH}	Receive threshold voltage		+100	mV
V_{IN}	Input voltage range	0	2.4	V

† tui is unit interval (i.e. bit width).
Note: Actual datasheet specifications may be significantly better.

1.3   Advantages of LVDS Over Single-Ended Standards

The differential data transmission method used in LVDS is less susceptible to common-mode noise than single-ended schemes like CMOS. Differential transmission uses two wires with opposite current and voltage swings instead of the one wire used in CMOS to convey the data. The advantage of LVDS is that if noise is coupled onto two wires as a common-mode and is thus rejected by the LVDS receivers, which looks at only the difference between the two signals. The differential signals also tend to radiate less noise than single-ended signals due to the canceling of magnetic fields. In addition, the current-mode driver is not prone to ringing and switching spikes, further reducing noise. The comparison chart in Table 2 provides a better understanding of the LVDS features and advantages. The common mode voltage ranges of an LVDS transmitter and receiver is shown in Figure 1 for easy understanding.

Table 2. Comparison of LVDS with Other Signaling Standards

Parameter	RS-422	PECL	LVDS
Differential driver output voltage	±2 to ±5V	±600 to 1000 mV	±250-450 mV
Receiver input threshold	±200 mV	±200 to 300 mV	±100 mV
Data rate	<30 Mbps	>400 Mbps	>400 Mbps

Parameter	RS-422	PECL	LVDS*
Supply current quad driver (no load, static)	60 mA (max)	32 to 65 mA (max)	8.0 mA
Supply current quad receiver (no load, static)	23 mA (max)	40 mA (max)	15 mA (max)
Propagation delay of driver	11 ns (max)	4.5 ns (max)	1.7 ns (max)
Propagation delay of receiver	30 ns (max)	7.0 ns (max)	2.7 ns (max)
Pulse skew (driver or receiver)	N/A	500 ps (max)	400 ps (max)

*LVDS devices noted are DS90LV047A/048A

The ANSI/TIA/EIA standard recommends a maximum data rate of 655 Mbps based on a limiting set of assumptions and it also provides a theoretical maximum of 1.923 Gbps based on a loss less medium. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling from the environment.
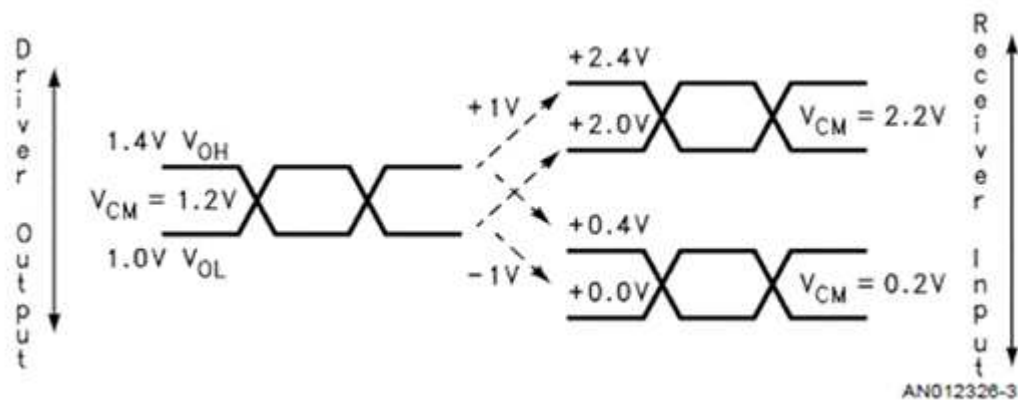

Figure 1. Common Mode Voltage Range

2   Marginal Capturing Analysis of ADC LVDS Data

When the data is captured without the sufficient setup and hold time in the LVDS receiver, then it is called marginal capturing. Marginal capturing of the data can happen due to mismatch in the trace lengths between LVDS pairs. For example, the marginal capturing happens in a 12-bit ADC, if the 6 DDR LVDS pairs are not routed with the same distance to FPGA. During the marginal capturing, some of the data bits may change its value which is equivalent to providing improper ADC data to FPGA.

Figure 2 indicates the marginal capture data which is captured inside the FPGA from the ADS6129 12-bit ADC.
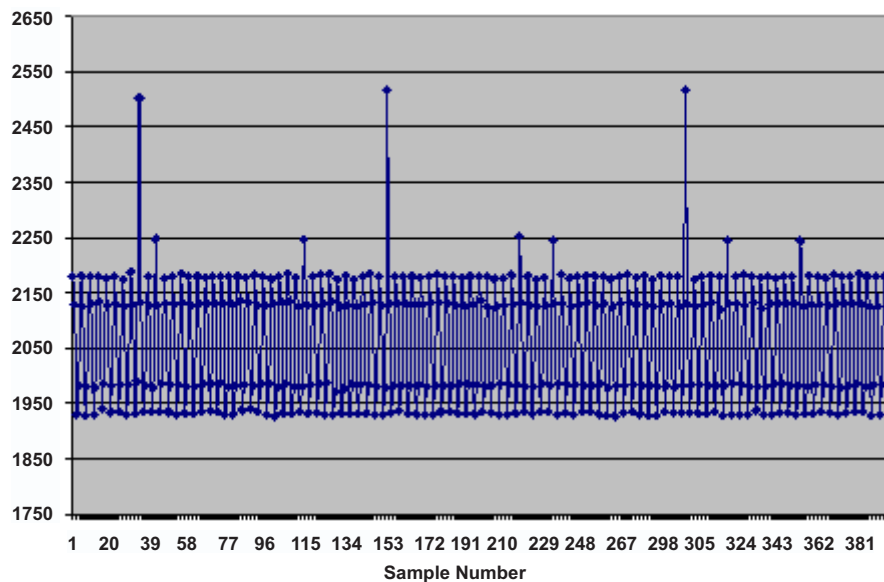

Figure 2. Marginal Capturing Data Plot

You can observe the peaks in Figure 2 due to the marginal capturing of the ADC data. In this case, the marginal capturing is observed for bits D6 and D8. The peaks are due to setup and hold time violations for D6 and D8 bits. The x axis represents the sample number and the y axis represents the signal amplitude of 12-bit ADC. The next section covers details on removing the marginal capturing issue.

3   Handling Marginal Capturing Problem

The marginal capturing problem can be resolved by two methods. One method is to use the ADC LVDS features for changing the delays of LVDS data lines with respect to LVDS output clock. The other method is to use the delay elements inside the FPGA.

3.1   *Using the Delay Feature Inside ADC*

The ADC LVDS data can be delayed, with respect to clock, by shifting output clock edges using the serial interface or parallel mode of ADC. Here, selectively introducing the delay for a particular LVDS pair is not available. Only shifting the output clock edge is possible by which it will change the setup and hold relations of all LVDS pairs, with respect to output clock.

Figure 3 provides the details on the clock position shifting feature in serial mode for the ADS6129. If the application needs the device to work in parallel mode, the voltage on the SEN pin can be changed in parallel mode to delay the output clock, as shown in Figure 4. In the ADS6129, one can first use the serial interface to delay the output clock and see if capture gets clean. Next, program the same delay forcing device in parallel mode and applying a relevant voltage on the SEN pin.

A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
44			<CLKOUT POSN> *Output clock position control*				0	0

LVDS Interface

D7-D5   **<CLKOUT POSN> Output clock rising edge position**

000   Default output clock position (refer to timing specification table)

100   Default output clock position (refer to timing specification table)

101   Rising edge shifted by + (4/26)Ts

110   Rising edge aligned with data transition

111   Rising edge shifted by - (4/26)Ts

D4-D2   **<CLKOUT POSN> Output clock falling edge position**

000   Default output clock position (refer to timing specification table)

100   Default output clock position (refer to timing specification table)

101   Falling edge shifted by + (4/26)Ts

110   Falling edge aligned with data transition

111   Falling edge shifted by - (4/26)Ts

Figure 3. Clock Position Shifting Feature for the ADS6129 in Serial Mode

Table 3. SEN – Analog Control Pin

SEN	Description – Output Clock Edge Programmability
0	LVDS: Data and output clock transitions are aligned. CMOS: Setup time increases by (6xTs/26), Hold time reduces by (6xTs/26)
(3/8) AVDD	LVDS: Setup time decreases by (4xTs/26), Hold time reduces by (4xTs/26) CMOS: Setup time increases by (9xTs/26), Hold time reduces by (9xTs/26)
(5/8) AVDD	LVDS: Setup time increases by (4xTs/26), Hold time reduces by (4xTs/26) CMOS: Setup time increases by (3xTs/26), Hold time reduces by (3xTs/26)
AVDD	Default output clock position (Setup/hold timings of output data with respect to this clock position is specified in the timing characteristics table)

3.2   Using the Delay Feature Inside FPGA

The other method of solving the marginal capture issue is by using the delay features inside the FPGAs. FPGAs have delay elements for each LVDS pair. For example, Xilinx FPGAs has the delay element called 'IDELAY' which can be used to change the individual delays for each LVDS pair. The IDELAY of FPGA is very flexible where it can be inserted between any LVDS pair of ADC and FPGA. For the marginal capturing issue shown in Figure 2, LVDS pairs D6_D7 and D8_D9 need to be delayed using the IDELAY element. Also, the skew across LVDS data pairs also can be compensated by using this IDELAY element inside the FPGA.

The delay elements are shown in Figure 4. The capture scheme of ADS6129 is shown in this diagram along with the FPGA IDELAY elements of Virtex FPGA.
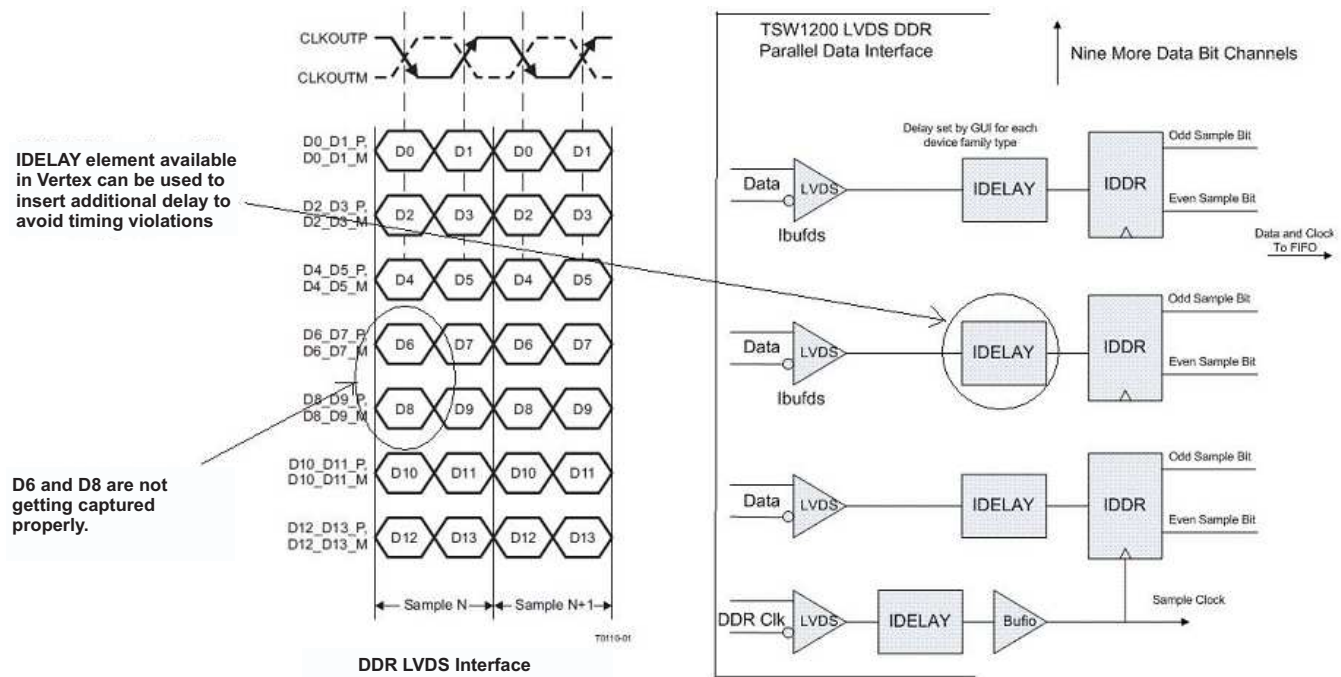
Figure 4. FPGA Delay Block Along with ADC LVDS Data

Even though the IDELAY element is available, IDELAY usage is not a must, unless the initial analysis of the board says that it has a non-length matched board and layout.

4 Checking the Timing Between the ADC LVDS Data and FPGA Using ADC Test Pattern Feature

For carrying out the setup and hold time validations, the system designer can use the test mode to generate the particular pattern which can be verified inside the FPGA. In test mode, bit flipping on every rising and falling edge can be programmed using the user custom pattern. This is the best way to test the health condition of the ADC LVDS data interface with FPGA. Figure 5 provides the information of this test pattern feature of ADS6129 and ADS6149.

A7−A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
51	<Custom Pattern>							
52	0	0	<Custom Pattern>					

D7–D0 **<CUSTOM LOW>**

8 lower bits of custom pattern available at the output instead of ADC data.

D5–D0 **<CUSTOM HIGH>**

6 upper bits of custom pattern available at the output instead of ADC data

Figure 5. Custom Test Pattern Option Inside ADC

This test identifies the proper interface between the ADC and FPGA. If the test mode data is captured perfectly with a test pattern of bit flipping on every clock cycle, it provides the confidence of the proper setup and hold times for the actual input. If the test mode is passed, it can be considered that the ADC LVDS data interface with FPGA is proper.

Eye diagrams can be generated using the TEST pattern and as well as with the NORMAL analog input signal. For illustration purposes, ADS6129 is used with 245.7 MSPS sampling rate and with a NORMAL input signal of 10 MHz at the input.

Figure 6 represents the eye diagram of the digitized data for the NORMAL analog input signal of 10 MHz. The eye diagram for the RAMP test signal for ADS6129 is shown in Figure 7.
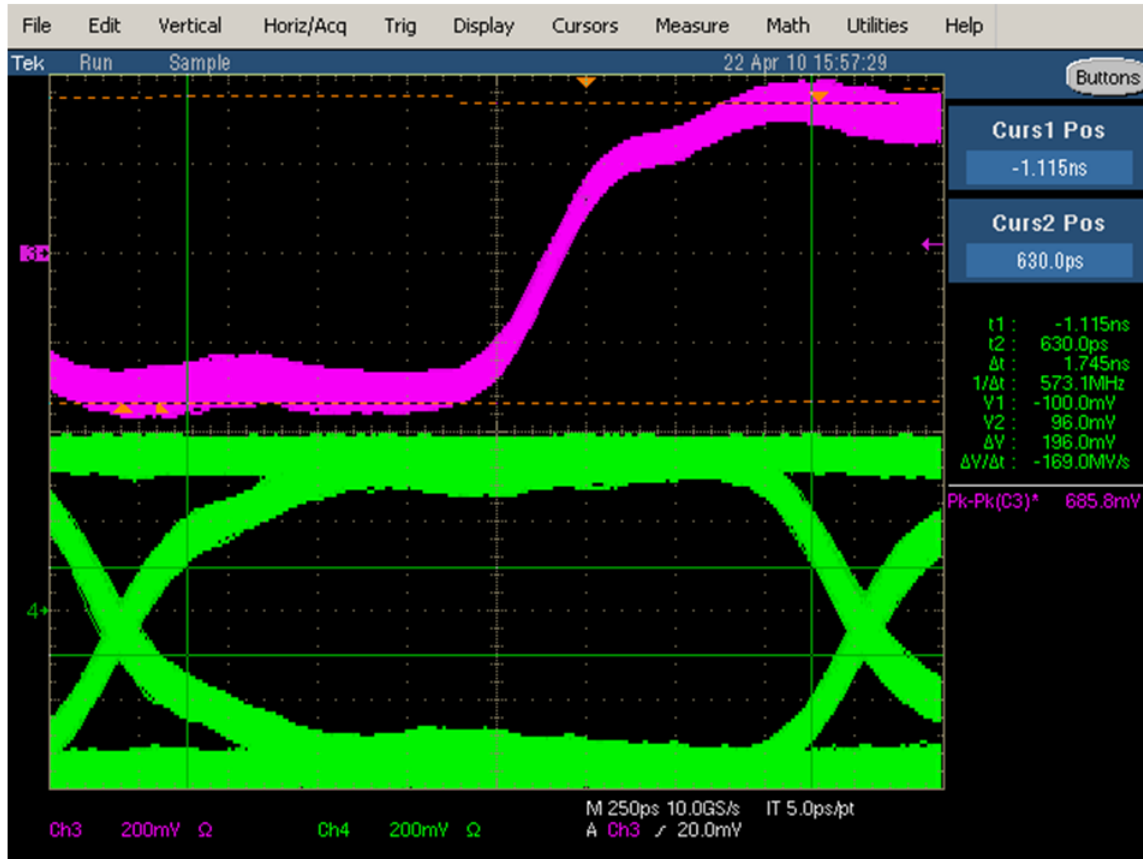

Figure 6. Eye Diagram of the Digitized Data for the NORMAL Input Analog Signal of 10 MHz
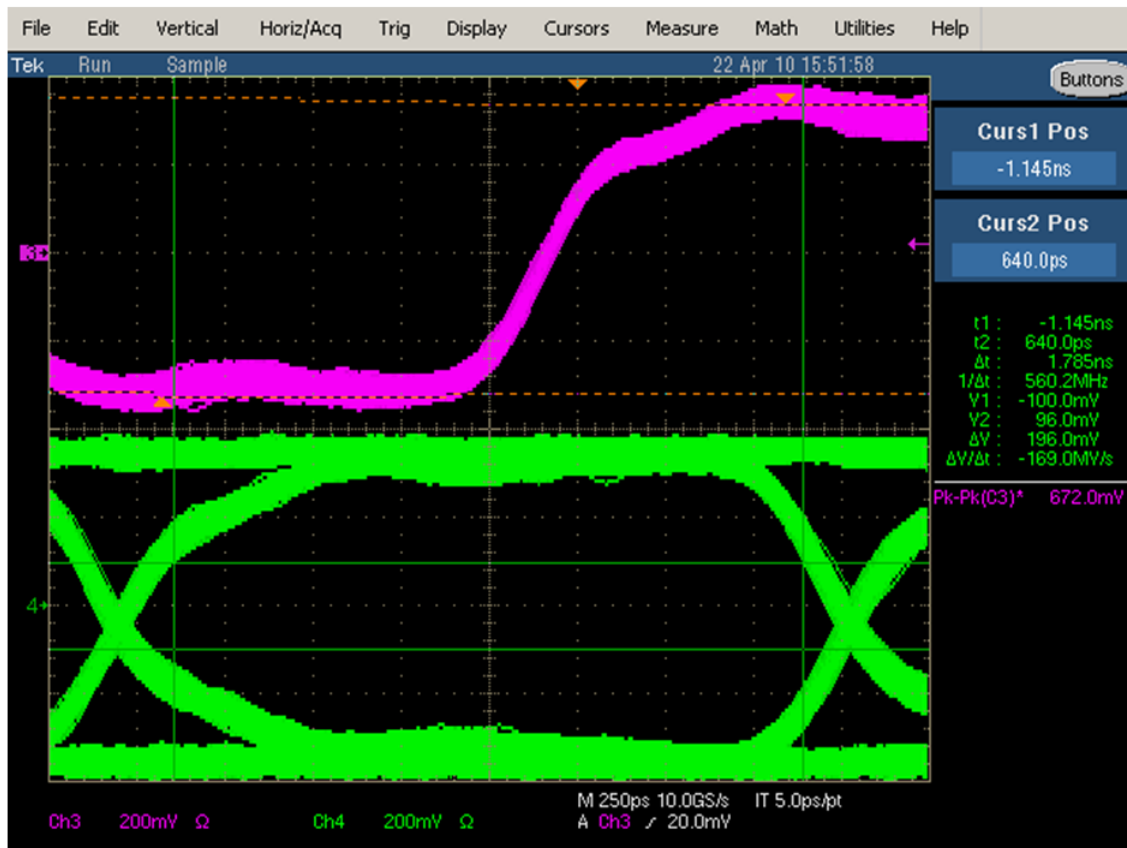
Figure 7. Eye Diagram of the Digitized Data of RAMP Test Input Signal

These figures are captured using a high-bandwidth Tektronix scope, TDS7245 (2.5 GHz BW) and measured differentially at one of the LVDS pairs for RAMP test signal and NORMAL input signal conditions.

When comparing the eye diagram of digitized data of a NORMAL analog input signal (Figure 6) and RAMP test pattern (Figure 7), both look very similar. However, with close observation, it is clear that the data-valid window reduces by around 40 ps, in the case of digitized data of the NORMAL analog input signal.

This shows that capturing the data marginally in your design gives occasional glitches in the case of a RAMP test signal; whereas, more frequent glitches arise for the digitized data of the NORMAL analog input signal.

As discussed in the previous section, the IDELAY element of FPGA can be used to fine tune the marginal capture, in case any skew gets introduced among data lines because of PCB routing or by FPGA itself during compilation of code with given timing constraints.

In the ADS6129 and in most of the other high-speed ADCs, test patterns and digitized input data both come out from the same LVDS serializer block. This block maintains the timing relation between the output clock and output data; therefore, there is not any difference in timing between test pattern and digitized data for a NORMAL input. But if there is some amount of coupling (cross-talk) among output data-lines, mostly due to board routing, timing may slightly differ as the output toggling pattern will be different in case of test-pattern and actual input signal digitized data. When a PCB is properly routed with tight matching among LVDS data pairs and clock, don't expect the difference in timing to be more than tens of pico seconds. As we have seen for ADS6129 from Figure 6 and Figure 7, at 250 MSPS the data-valid window (which is about 1.7 ns wide) reduces by just 40 ps with digitized data for the NORMAL signal against the RAMP test data. So it is evident that if RAMP passes the capture test in FPGA, digitized data for the NORMAL analog input signal also passes, unless it is a marginal capture.

Remember that the datasheet numbers are characterized over temperature with full-scale sinewave input signal and not based on test patterns. The timings with test patterns such as RAMP test signal might be better than those with digitized data of actual analog input signal.

Also, please note that for testing the validity of LVDS data between ADC and FPGA, do not use toggle test patterns which change data every clock cycle (single data rate). Rather, use a test pattern which changes every clock edge (double data rate) which is a more stringent test for performing timing analysis.

5   Design Consideration in LVDS Signal Routing Between ADC and FPGA

1. If the routing distance between the ADC output and FPGA input pins is more, then care must be taken to maintain controlled differential impedance near 100 Ω. The physical length of each trace between the LVDS pairs of ADC outputs and the FPGA inputs should be matched within 5 mm of each other for better performance. Mismatch creates a phase difference between voltages along the signal pairs and radiates as common mode noise. All LVDS signals need to be routed as 100-Ω differential lines. The overall lengths of the differential pairs are not critical but the matching between the differential pairs within the specified mils is important. This matching specification is dependent on the ADC sampling rate and the setup and hold time margins.
2. At any cut between the ADC LVDS output and FPGA input, the differential characteristic impedance should be between 90 Ω to 110 Ω. The impedance matching is very important due to the fast-edge-rate of LVDS signals.
3. It is always better to use a minimum 4 layers in the PCB. Separate layers for ground, supply, and single-ended signals (like CMOS) and LVDS signals are required for highspeed designs.
4. A minimum number of PCB vias for the LVDS lines is always better. It is also better to use 45 degree turning and to avoid 90 degree turns.
5. LVDS signals are not intended to work without a termination resistor. Use the surface mount resistor of 100 Ω within 7 mm from the FPGA LVDS connections. The best option is to use the internal 100- Ω termination resistor of FPGA, if available. For an internal FPGA termination resistor, the input LVDS termination register needs to be made "TRUE" in the FPGA glue logic.
6. Routing the high-speed traces on the top layer avoids the vias and also inductance due to the vias. However, routing the high-speed traces on the middle layers help in better noise suppression. Routing noisy signals on a strip line (middle layer) rather than a micro-strip line (top/bottom) helps reduce EMI.

6   Conclusion

Understanding the LVDS data capturing issues will help in designing a reliable ADC and FPGA interface. The delay features of ADC and FPGA provide the flexibility for avoiding the delays introduced due to the trace length mismatches. The marginal capturing can be eliminated with the use of these features. The test patterns inside the ADC will help the designer for testing the correctness of the ADC and FPGA LVDS interface capture link.

7   References

1. ADS6129/ADS6149 Datasheet (SLWS211B).
2. LVDS Standard (TIA/EIA - 644).
3. LVDS Owner's Manual (SNLA187).

Revision History

Changes from Original (June 2013) to A Revision   **Page**

- Changed document to the latest TI application report template.…………………………………………………………… 1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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