Application Report
SLAA571A–November 2012–Revised May 2015

Design Challenges and Improvement Techniques for SAR ADC Driver Circuit

Dale Li *High Performance Analog/Field Application*

ABSTRACT

Driver circuit design of switched-capacitor successive approximation register (SAR) analog-to-digital converters (ADC) is critical. The ADS8568 is a typical device using this kind of architecture. The ADS8568's 8-channel, 16-bit, simultaneous sampling ADC with true bipolar input, supports up to 510-KSPS sampling rate per channel. The ADS8568's structure is perfectly suitable for relay measurement and protection systems of industrial power automation applications. This application report presents the solution with the system performance improvement techniques to resolve the challenges of designing the driver circuit for the ADS8568 with comparison tests that also demonstrate these performance improvements.

Contents

List of Figures

List of Tables

1 Introduction

In power line measurement and protection systems, it is often required to simultaneously sample large numbers of voltage and current channels in multi-phase power distribution and transmission networks and critical to have the simultaneous sampling capability to maintain the phase information between the voltage and current channels. The ADS8568 is the 8-channel, 16-bit simultaneous sampling SAR ADC with true bipolar input up to ±12 V; these features make it ideal for capturing voltage and current signals from PT(Voltage Transformer) and CT(Current Transformer) with an operational amplifier or directly in this kind of system application.

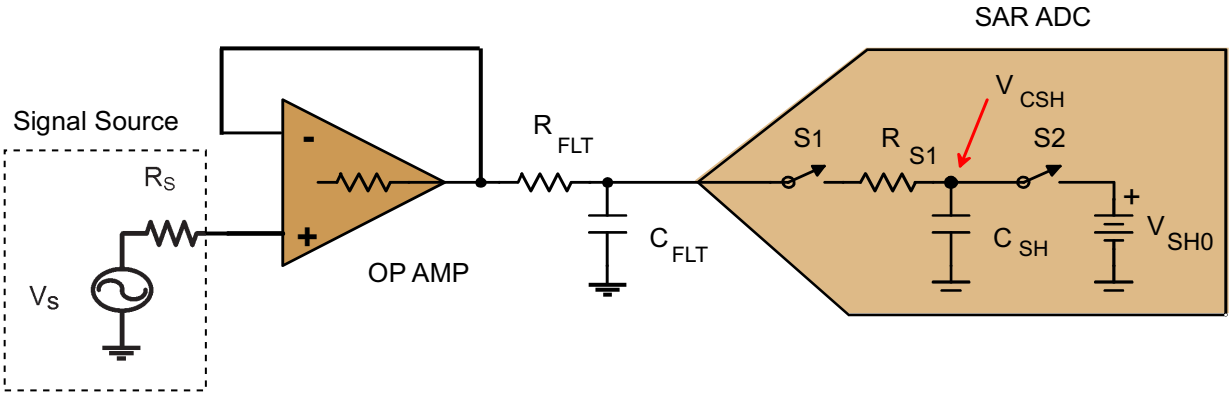

Figure 1. Typical Driver Circuit for SAR ADC

For optimum SAR-ADC performance, the recommended driver circuit is an operational amplifier used in combination with an RC (resistor-capacitor) filter as shown in Figure 1. This driver circuit's major functions include:

- Signal conditioning for input signal from the source
- Filter function
- Isolation between the signal source and ADC
- Providing enough charges to the internal sampling capacitor of SAR ADC which uses the switched capacitor array architecture

The driver circuit must have the ability to charge the ADC's internal input sampling capacitor to the proper value and maintain stability during the ADC's acquisition period. The C_{FLT} provides a nearly perfect input source to the SAR ADC. R_{FLT} keeps the amplifier stable by isolating the amplifier's output stage from the capacitive load. The selection of components for the driver circuit is important and the proper selections make it possible to get the optimal system performance, including the value selections of R_{FLT} and C_{FLT}.

2 Design Challenge for a Driver Circuit Without An Amplifier

To simplify the circuit design and save cost, it is popular to design the driver circuit of SAR ADCs without any amplifier in power line measurement and protection systems. Engineers only use one first-order passive RC filter and sometimes a second-order RC filter is used to get faster roll-off and stop-band attenuation.

But if proper care is not taken with system architecture or if the correct value of components R_{FLT} and C_{FLT} are not selected, the circuit could produce system errors and the system performance suffers in the area of DC and AC performance, THD (total harmonic distortion), for example. THD is a very important system parameter for industrial replay protection and an important measurement system in power automation applications.

2.1 Driver Circuit Without an Amplifier

The circuit in Figure 2 is a typical circuit without a front-end amplifier used widely in industrial replay protection and measurement systems. The second-order RC filter or much larger value R_{FLT} and C_{FLT} are often used in this kind of application too, thus providing poor system performance. The operating frequency for CT and PT isolation and measurement transformers is 50 Hz (or 60 Hz). The input signal is usually ±10 V or ±5-V bipolar, 50-Hz sine wave from PT or CT (signal source, V_S). To filter the noise and get the optimal filter result, the larger value resistor (R_{FLT}) and capacitor (C_{FLT}) are usually used. This also provides a lower cut-off frequency of the filter. The reason for using this big resistor is the demand of isolation between the SAR ADC and signal resource because there is not any front-end amplifier. In general, 20, 80 or 200 sample points per cycle is often used and depends on system demand, so the sampling rate of the ADC is 1 KSPS, 4 KSPS, or 10 KSPS for a 50-Hz sine-wave input signal.

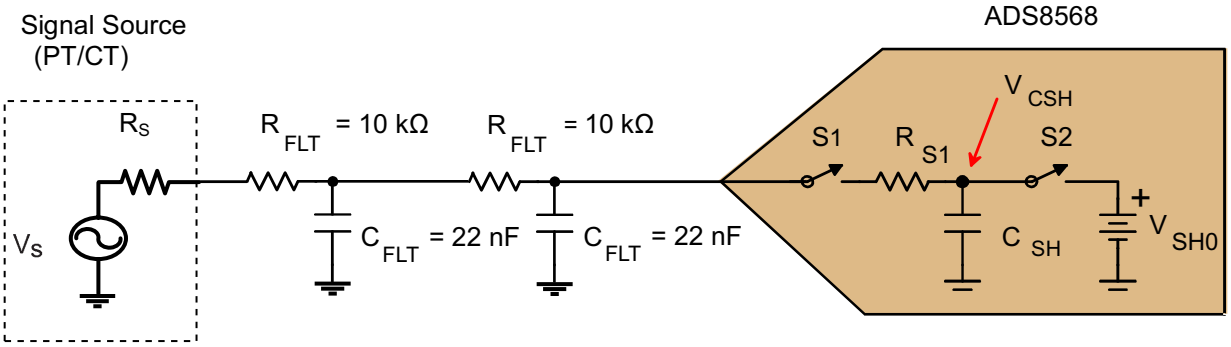

Figure 2. ADS8568's Driver Circuit Without a Front-End Amplifier

After tests, the system performances are bad for this circuit configuration, including THD, SINAD (Signal-to-Noise and Distortion ratio) and SFDR (Spurious Free Dynamic Range) performances. If the filter order is increased, from first order to second order, the performances are worse. If the sampling rate is increased, the performances for the same circuit are much worse.

2.2 Sampling Rate and Acquisition Time

SAR ADC's sampling rate and acquisition times are important parameters in the design challenges. SAR ADC's sampling rate usually correlates to ADC's acquisition time (t_{ACQ}) and conversion time (t_{CONV}).

$$T = \frac{1}{t_S} = t_{ACQ} + t_{CONV} \quad (1)$$

f_S is the sampling rate.

For ADS8568,

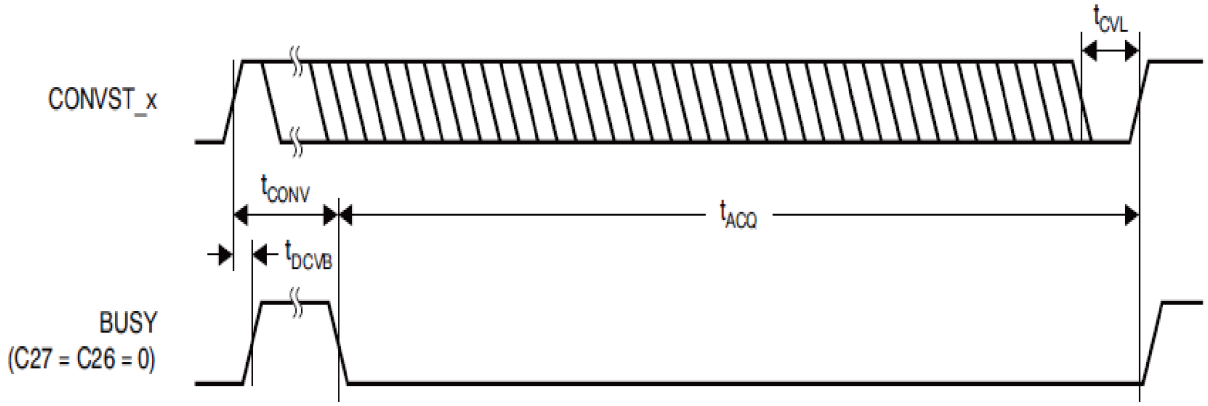

Figure 3. ADS8568's Acquisition Time and Conversion Time

The conversion time (t_{CONV}, 1.7 µs) in ADS8568's data sheet is the maximum time the ADS8568 needs for one conversion. The acquisition time (t_{ACQ}, 280 ns) in ADS8568's data sheet is the minimum time to specify excellent performance at the highest sampling rate. The real and operating acquisition time to ADC depends on the real sampling rate because the conversion time is approximately fixed and the ADC enters into the acquisition status automatically after the conversion is finished and when the BUSY signal is going down.

2.3 Design Challenge for the Driver Circuit

When designing the driver circuit of switched-capacitor input structure SAR ADCs, the time constant (τ_{FLT}) of the RC filter in front of the ADC or the equivalent time constant (τ_{TOT}) must be considered. This τ_{FLT} determines the settling time of the filter. This time constant also depends on the acquisition time (t_{ACQ}) and must be properly set so that k (the time constant multiplier) time constants are allowed during the converter's operating acquisition time.

Figure 4 shows a simplified model for the capacitive input stage of the circuit in Figure 2, if just considering the first-order RC filter (see reference 2).

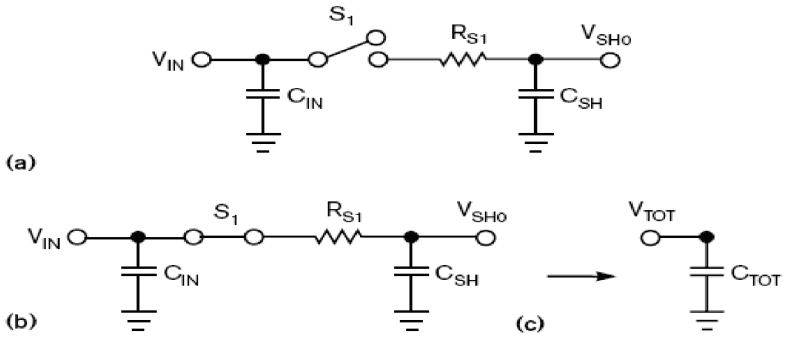

Figure 4. Simplified Model for First-Order RC Filter

Use the following equations according to the charge redistribution between C_{FLT} and C_{SH}:

$$t_{ACQ} \geq k_3 \times \tau$$

$$k_3 = \ln\left(\frac{1}{\alpha + 1} \times 2^{N+1}\right), \quad \alpha = \frac{C_{FLT}}{C_{SH}} \tag{2}$$

Where t_{ACQ} is acquisition time

k_3 is new time-constant multiplier

τ is the time-constant

N is data converter's resolution

For the first-order RC filter system in Figure 2,

$$\alpha = \frac{C_{FLT}}{C_{SH}} = \frac{22\ nF}{20\ pF} = 1100 \tag{3}$$

So,

$$k_3 = \ln\left(\frac{1}{\alpha+1} \times 2^{N+1}\right) = \ln\left(\frac{1}{1100+1} \times 2^{16+1}\right) = 4.78 \tag{4}$$

When ADS8568's sampling rate (f_S) is 10 KSPS, the operating acquisition time is,

$$t_{ACQ} = \frac{1}{f_S} - t_{CONV} = \frac{1}{10k} \times 10^6 - 1.7\mu s = 98.3\mu s \tag{5}$$

Calculate the required time constant of ADC,

$$\tau_1 \le \frac{t_{ACQ}}{k_3} = \frac{09.3\mu s}{4.78} = 20.56\mu s \tag{6}$$

When ADS8568's sampling rate (f_S) is 4 KSPS, the operating acquisition time is,

$$t_{ACQ} = \frac{1}{f_S} - t_{CONV} = \frac{1}{4k} \times 10^6 - 1.7\mu s = 248.3\mu s \tag{7}$$

Calculate the required time constant of ADC,

$$\tau_2 \le \frac{t_{ACQ}}{k_3} = \frac{248.3\mu s}{4.78} = 51.95\mu s \tag{8}$$

When ADS8568's sampling rate (f_S) is 1 KSPS, the operating acquisition time is,

$$t_{ACQ} = \frac{1}{f_S} - t_{CONV} = \frac{1}{1k} \times 10^6 - 1.7\mu s = 998.3\mu s \tag{9}$$

Calculate the required time constant of ADC:

$$\tau_3 \le \frac{t_{ACQ}}{k_3} = \frac{998.3\mu s}{4.78} = 208.85\mu s \tag{10}$$

But the time constant of an input circuit using the first-order RC filter configuration in Figure 2, is:

$$\tau_{TOT} = (R_S + R_{FLT}) \times (C_{FLT} + C_{SH}) = 10K\Omega \times (22nF + 20pF) = 220.2\mu s \tag{11}$$

Where R_S = 0 Ω and C_{SH} = 20 pF for ±2 V_{REF} input range to ADS8568.

This time constant is larger because of the large values of resistor (R_{FLT}) and capacitor (C_{FLT}), and observably cannot meet the requirement for Equation 7 and Equation 8, cannot track the voltage of the input signal and cannot charge the ADC's internal sampling capacitor to the proper value during the operating acquisition time, also affecting and limiting system performance. But, τ_{TOT} is very close to τ_3 in Equation 10 and basically does not degrade the performance of the signal chain for the sampling rate in Equation 10. The following comparison tests demonstrate this too.

If a second-order RC filter is used, the time constant is much larger and also cannot meet the requirement of charging the SAR ADC's internal sampling capacitor.

Because no amplifier is used as an active filter in Figure 2, the RC filter acts as all filter functions. The input signal from power lines is only a 50-Hz frequency signal, so to get a better filter effect, the low cut-off frequency RC filter is often used. That is why the larger resistor and capacitor values are selected. The cut-off frequency of the first-order RC filter designed in Figure 2 is:

$$f_{-3dB} = \frac{1}{2\pi(R_S + R_{FLT})C_{FLT}} = \frac{1}{2\pi \times 10k \times 22nF} = 723.4Hz \tag{12}$$

Sometimes, the lower cut-off frequency RC filter is used; for example, 361.7 Hz with 20-kΩ resistor and 22-nF capacitor.

So for the driver circuit design of the switched-capacitor input structure SAR ADC without any front-end amplifier, it is critical to consider the trade-off between the time constant and the cut-off frequency of the filter, it is also a challenge to balance this trade-off.

2.4 Improvement Techniques

The time constant is determined directly by the values of resistor R_{FLT} and capacitor C_{FLT} or the amount of filter order. From Equation 2, two techniques are used to meet this equation, to resolve the system performance issue and challenge in the circuit in Figure 2, increasing the acquisition time (t_{ACQ}) of ADC directly and decreasing the filter orders or the component value of the RC filter.

2.4.1 Increase Acquisition Time

According to Equation 1, the sampling rate (f_S) of SAR ADC is reduced to increase the acquisition time (t_{ACQ}). The acquisition time can be increased from 98.3 µs to 248.3 µs by reducing the sampling rate from 10 KSPS to 4 KSPS, furthermore, to 998.3 µs with a 1 KSPS sampling rate. These have been calculated in Section 2.3 and the following comparison tests also demonstrate the system performance improvement with acquisition time extension.

2.4.2 Decrease the Filter Orders and Component Value

Another technique resolving this performance issue is reducing the filter order amount or the values of resistor (R_{FLT}) and capacitor (C_{FLT}) directly. These techniques absolutely decrease the time constant in Equation 1. The RC filter orders can be reduced from second order to first order, the capacitor value also can be reduced from 22-nF to 820-pF. The following comparison tests also demonstrate the system performance improvement by reducing the RC filter orders and the capacitor value. The big resistor is reserved because of the isolation requirement.

3 Performance Test

3.1 Test System

Figure 5 shows the typical test system for AC performance in this report. The software for this report was developed with *Code Composer Studio*™ V3.3 based on TI's TMS320F28335 Digital Signal Processor (DSP™) with an ADS8568 test board. The FFT wave forms are created in ADCPro software, which is available for download from the Texas Instruments website www.ti.com.

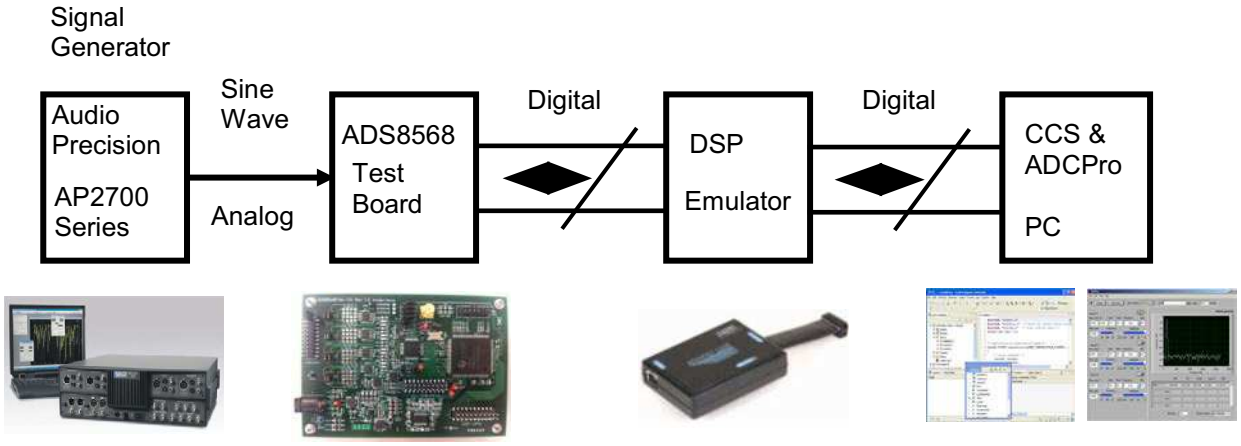

Figure 5. Performance Test System for the ADS8568 Circuit

3.2 Performance Comparison Test

The following tests are based on the same circuit board. The test signal, V_S, is the high-performance, low-distortion, bipolar and 50-Hz sine-wave signal from the SYS-2722 generator of Audio Precision. The –0.5 dBFS signal amplitude of V_S is used for the following tests in Table 1 through Table 3.

The FFT waveforms for these test data are shown in Section 6 through Section 8.

Table 1 is the system AC performance results based on the original design in Figure 2 with a second-order RC filter (R_{FLT} = 10 kΩ, C_{FLT} = 22 nF). The system AC performance tests are done based on different sampling rates of the ADS8568; 1 KSPS, 4 KSPS, and 10 KSPS for 20, 80, and 200 sample points per cycle of sine wave. From the test data, the lower sampling rate for the same driver configuration, also the longer acquisition time, and the better system AC performance, especially for THD, SINAD, and SFDR is shown. The THD is improved from –65.46 dB with 10 KSPS sampling rate to 92.80 dB with 1 KSPS sampling rate.

Table 1. Test Result for Second-Order Filter – R_{FLT} = 10 kΩ, C_{FLT} = 22 nF (unit: dBc)

Sampling Speed	SNR	THD	SINAD	SFDR
10 KSPS	85.05	–65.46	65.41	67
4 KSPS	84.69	–74.74	74.32	76.2
1 KSPS	86.35	–92.80	85.47	94.1

If reducing the filter orders from second to first order of the RC filter in Figure 2, the same tests are finished and the new test results are listed in Table 2. The measurement results show that increasing the acquisition time, reducing the sampling rate from 10 KSPS to 1 KSPS, improves the system AC performance. With the longer acquisition time, the THD improves from –79.97 dB to –100.88 dB. The test results in Table 2 also prove the performance improvement with the time constant reduction by reducing the filter orders.

Table 2. Test Result for First-Order Filter – R_{FLT} = 10 kΩ, C_{FLT} = 22 nF (unit: dBc)

Sampling Speed	SNR	THD	SINAD	SFDR
10 KSPS	85.92	–70.97	70.83	73.3
4 KSPS	85.32	–82.32	80.56	84.6
1 KSPS	86.96	–100.88	86.79	105.8

For the first-order filter, continue reducing the value for C_{FLT} from 22-nF to 820-pF, the test results in Table 3 for this configuration show that the system AC performance is significantly improved. With the lower sampling rate and longer acquisition time, the THD improves from –96.88 dB to –103.61 dB. The THD and SFDR performances are much better than before, especially for same higher sampling rate, the improvement in THD is approximately 26 dB from 22-nF to 820-pF CFLT.

Table 3. Test Result for First-Order Filter – R_{FLT} = 10 kΩ, C_{FLT} = 820 pF (unit: dBc)

Sampling Speed	SNR	THD	SINAD	SFDR
10 KSPS	86.08	–96.88	85.73	106.8
4 KSPS	85.03	–99.30	84.87	105.8
1 KSPS	85.56	–103.61	85.49	107.4

These measurement results show and prove that the length of the acquisition time, the RC filter orders and the value of components in the RC filter, affect the system performance. The system improvement is obvious by decreasing the sampling rate and reducing the filter orders and the value of the components of the filter.

4 Conclusion

This application report presents the popular driver circuits without an amplifier to SAR ADC in industrial application, discusses the challenges along with the driving circuit of the switched-capacitor input structure SAR ADC, and analyzes the root reason and trade-offs between the performance demand and RC filter design. Based on the input signal, ADC's sampling rate, input capacitor and resistor of filter, and the system performance demand, it is important to balance these critical conditions. Two improvement techniques are introduced with demonstration tests in this report. This application report is also suitable for the ADS8548 and ADS8528, TI's SAR ADCs.

5 References

1. ADS8568, ADS8548, ADS8528 Data Sheet (SBAS543A)
2. Oljaca, M. and B. Baker. (2007). External components improve SAR-ADC accuracy. EDN. June 7, 2007. Download at: www.edn.com/article/CA4314401

6 Appendix A. FFT for Second-Order Filter (R_{FLT} = 10 kΩ, C_{FLT} = 22 nF)

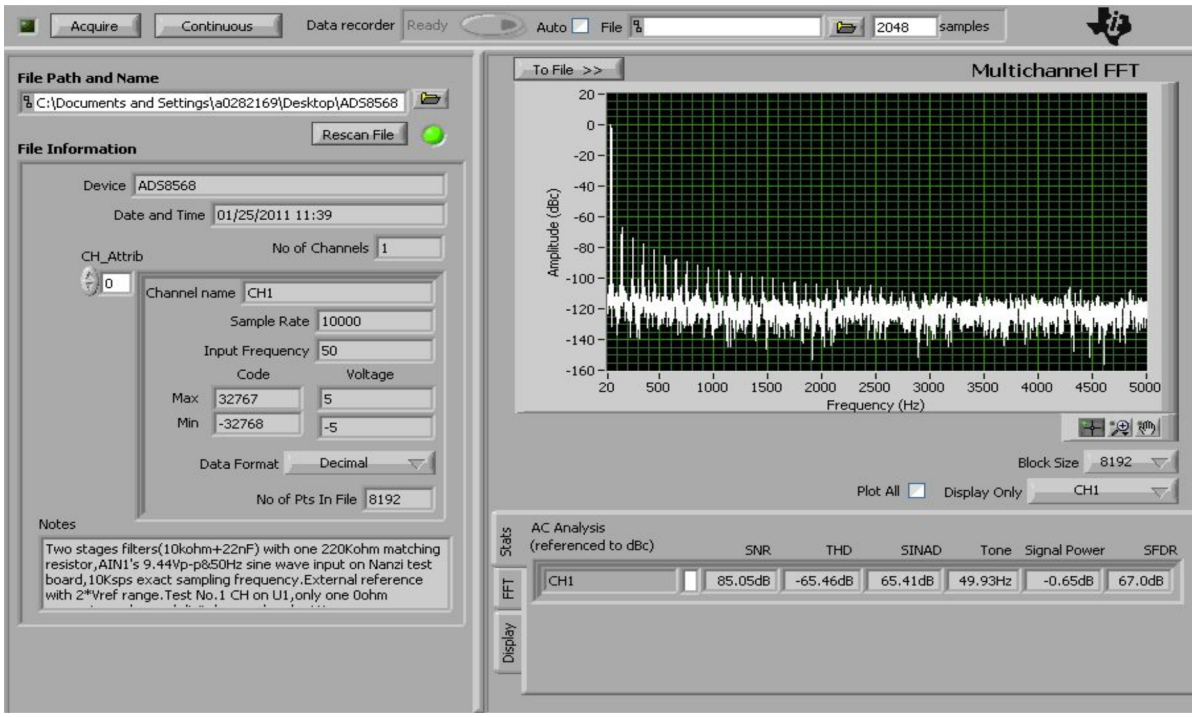

Figure 6. FFT for 10-KSPS Sampling Rate (V_S = –0.5 dBFS)

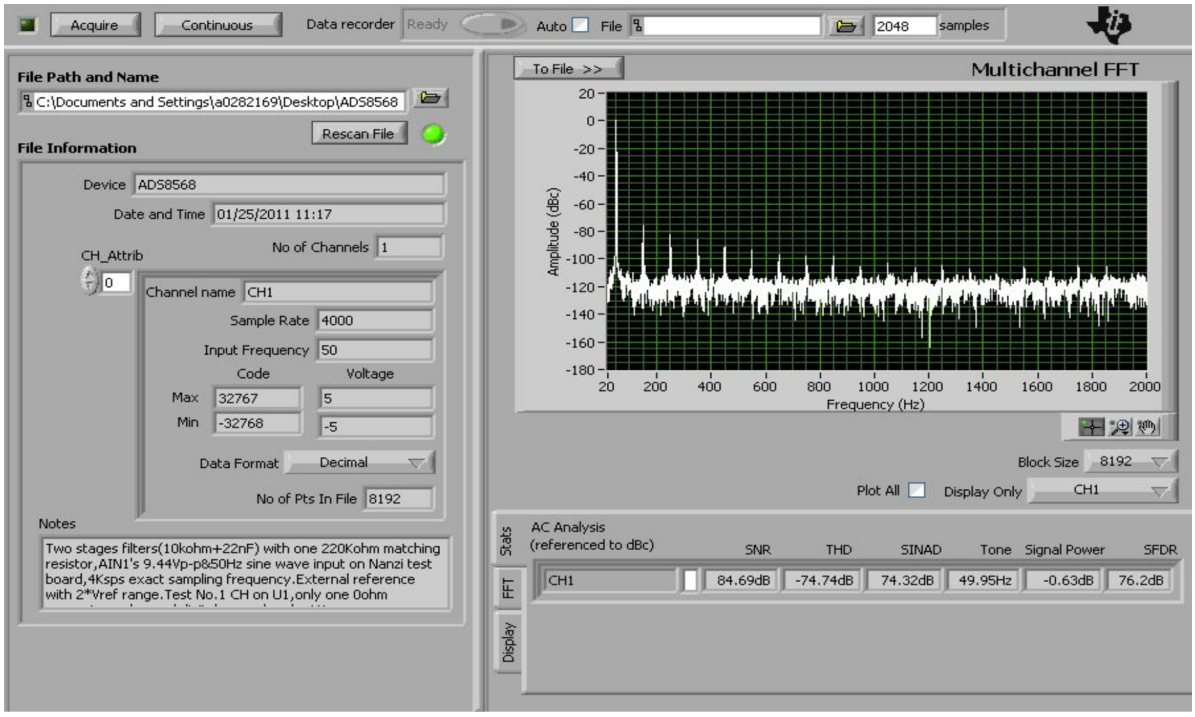

Figure 7. FFT for 4-KSPS Sampling Rate (V_S = –0.5 dBFS)

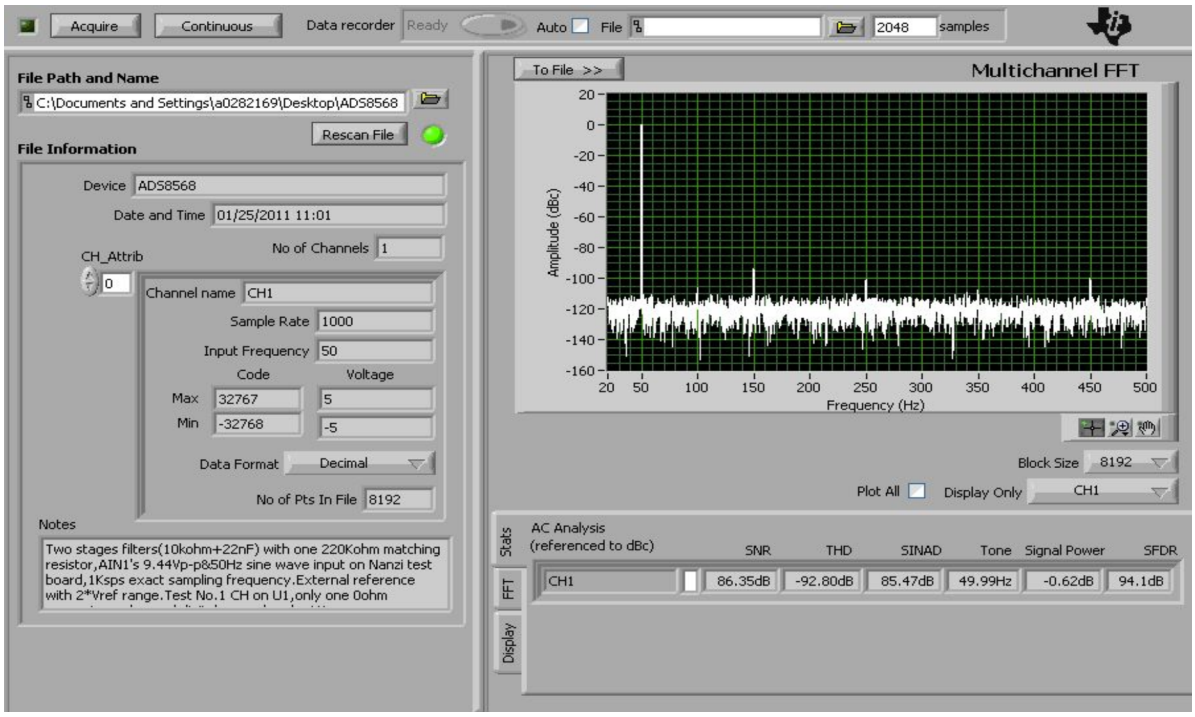

Figure 8. FFT for 1-KSPS Sampling Rate (V_S = –0.5 dBFS)

7 Appendix B. FFT for First-Order Filter (R_{FLT} = 10 kΩ, C_{FLT} = 22 nF)

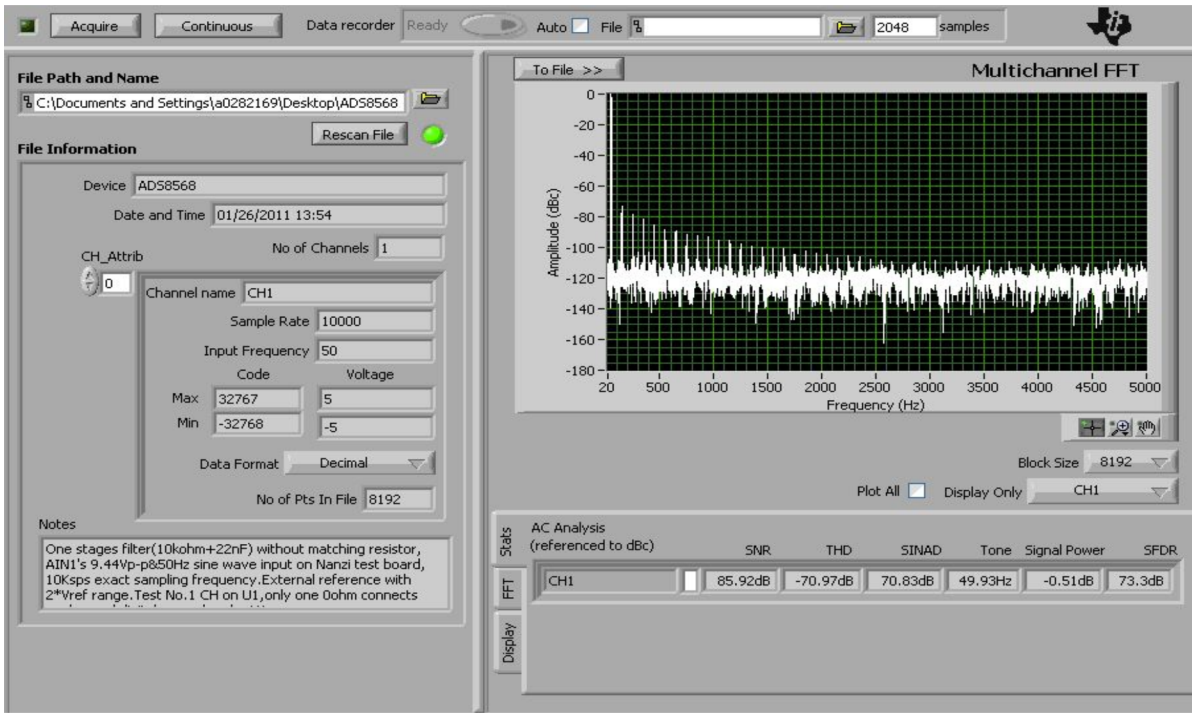

Figure 9. FFT for 10-KSPS Sampling Rate (V_S = –0.5 dBFS)

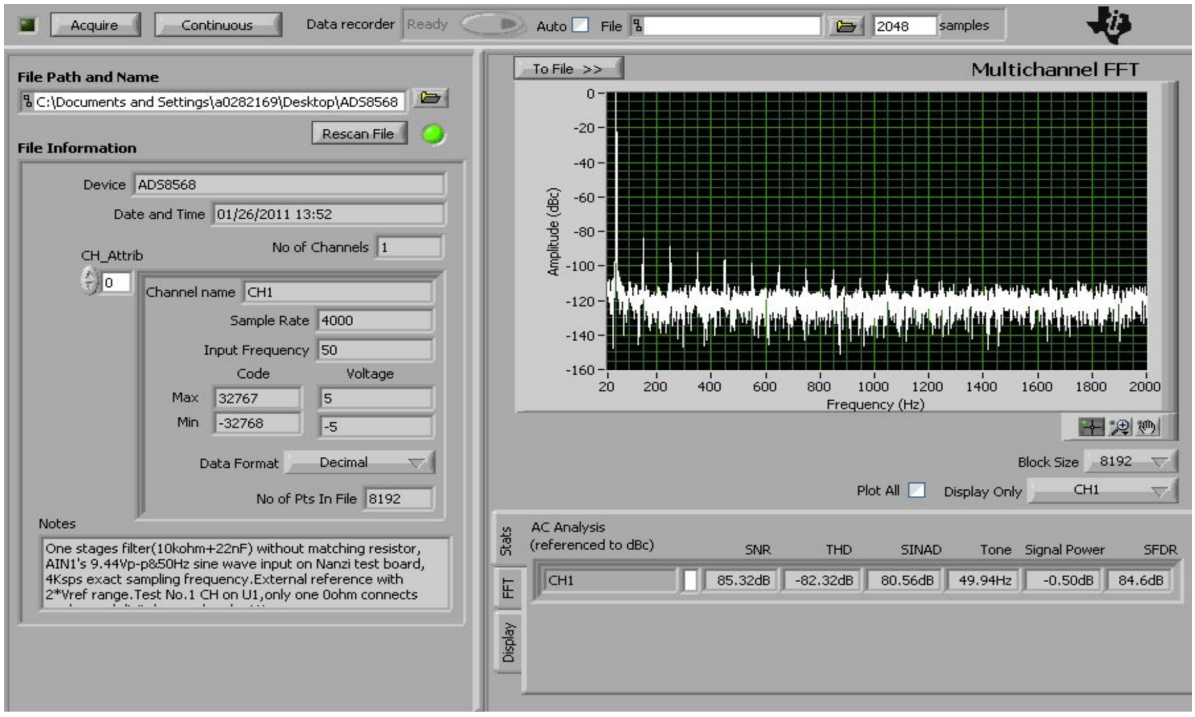

Figure 10. FFT for 4-KSPS Sampling Rate (V_S = –0.5 dBFS)

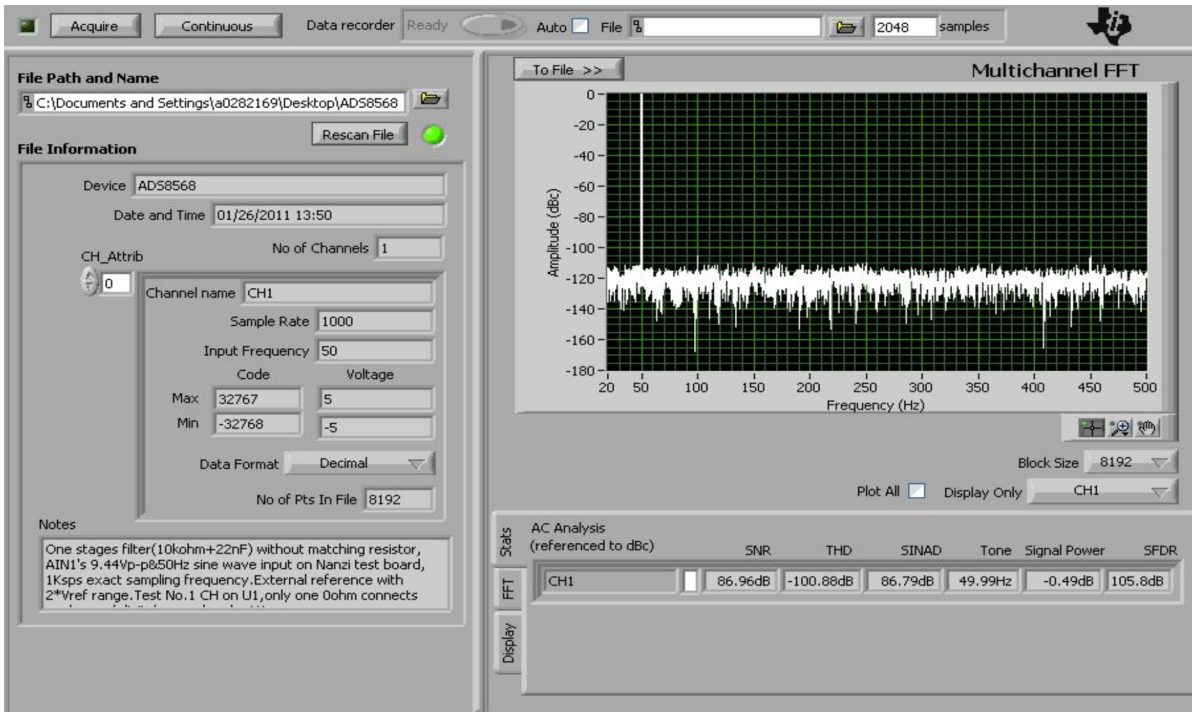

Figure 11. FFT for 1-KSPS Sampling Rate (V_S = –0.5 dBFS)

8 Appendix C. FFT for First-Order Filter (R_{FLT} = 10 kΩ, C_{FLT} = 820 pF)

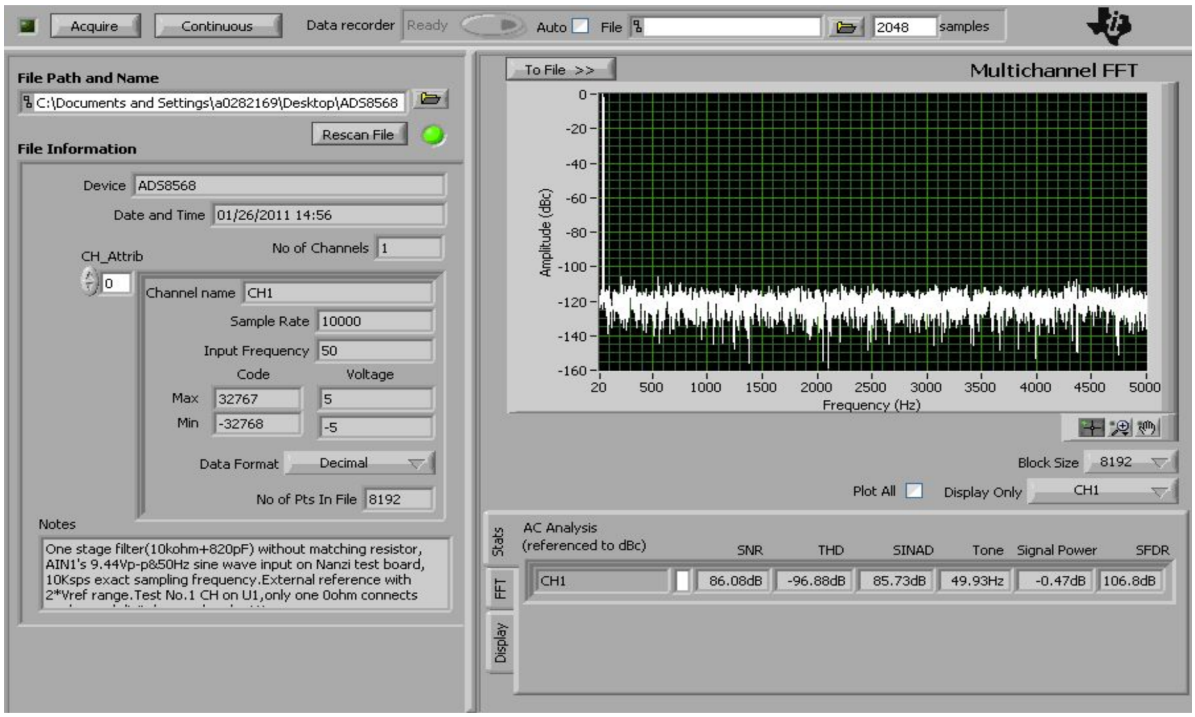

Figure 12. FFT for 10-KSPS Sampling Rate (V_S = –0.5 dBFS)

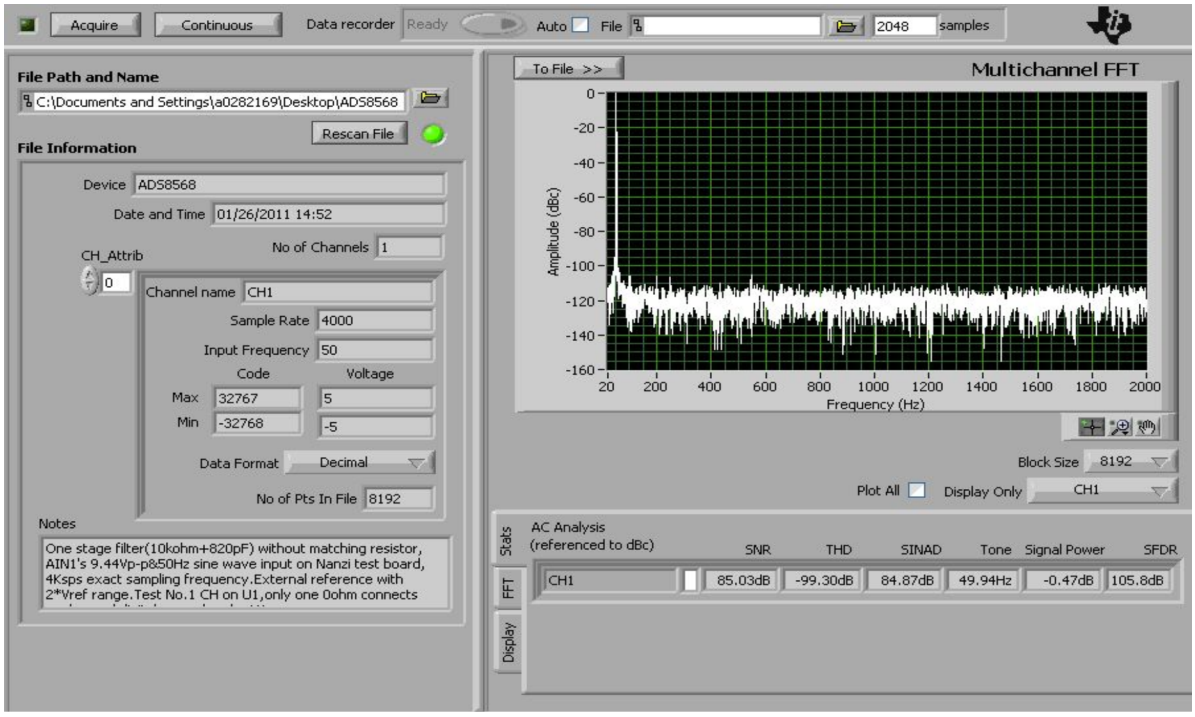

Figure 13. FFT for 4-KSPS Sampling Rate (V_S = –0.5 dBFS)

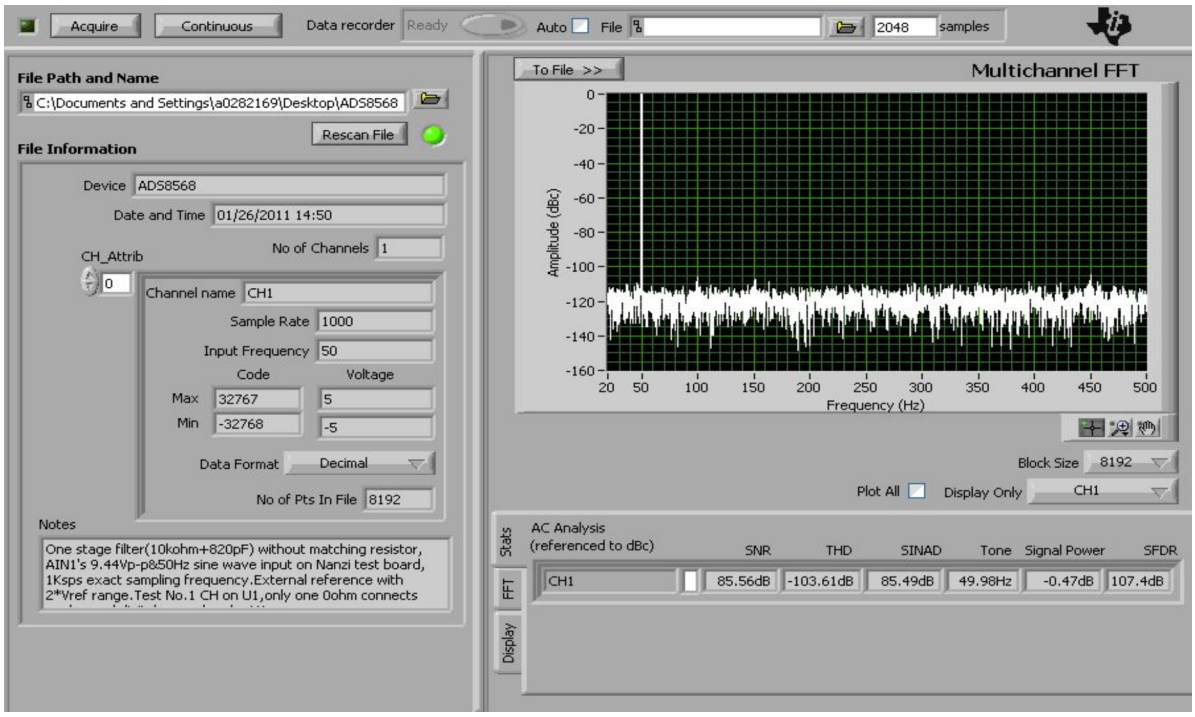

Figure 14. FFT for 1-KSPS Sampling Rate (V_S = –0.5 dBFS)

Revision History

Changes from Original (November 2012) to A Revision	Page
• Changed format to latest TI application report template.	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265