Application Report
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Stereo AGC Functionality for the TLV320AIC3254

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ABSTRACT

This report describes how to configure the TLV320AIC3254 (or *AIC3254*) very low-power stereo audio codec for stereo automatic gain control (AGC) operation.

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1 Introduction

The analog-to-digital converter (ADC) channel for the AIC3254 provides an AGC function for recording. AGC can be used to maintain a nominally-constant output level while recording. All the ADC processing blocks (also known as PRBs) support this AGC functionality.

The AGC architecture supported in the PRBs provides independent control of the AGC function for the left and right channels. For example, if the target AGC gain is –12 dB, the left channel signal level is –14 dB, and the right channel signal level is –18 dB, the AGC will then bring both channel signals to –12 dB. The gain applied to the left channel would be +2 dB while the gain applied to the right channel is +6 dB.

In some applications, however, it is desirable to maintain the level difference between the left and right channels while using AGC. This capability is also known as *stereo AGC functionality*. In stereo AGC, the same gain is applied to both the left and right channels. In the above example, then, for stereo AGC functionality, +2 dB will be applied to both channels. The left channel will move up to –12 dB, and the right channel will move up to –16 dB. The relative level difference of 4 dB is maintained between the left and the right channels.

Figure 1 shows the difference between normal AGC and stereo AGC operation.

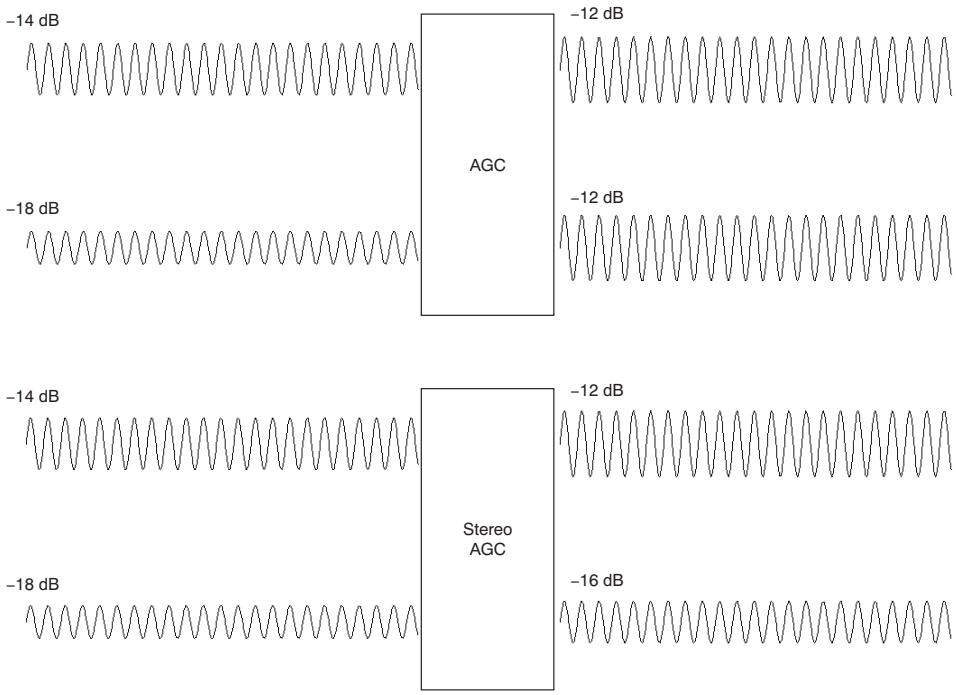

Figure 1. Stereo AGC Operation

2 Stereo AGC Recording Operation (STAGC_R)

The signal chain for stereo AGC recording operation (STAGC_R) is shown in Figure 2.

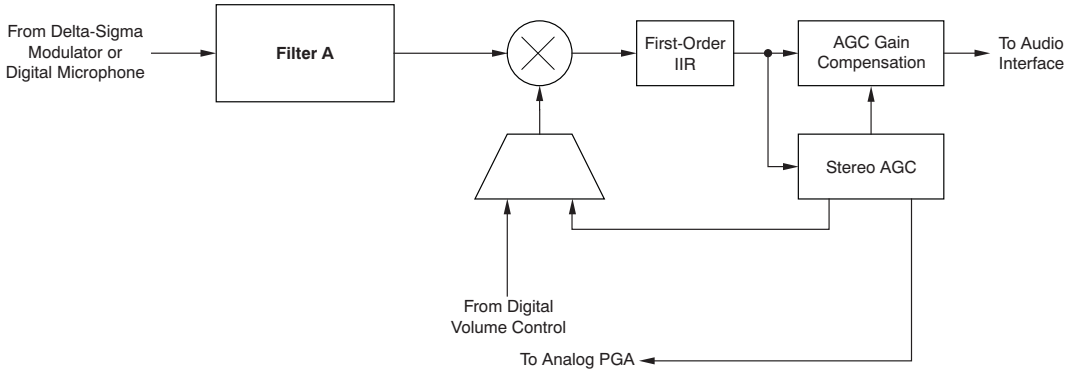

Figure 2. STAGC_R Signal Chain

STAGC_R first applies the AGC algorithm on the channel that has the higher signal strength. The same AGC gain will then be applied to the other channel. The difference in levels between the two channels will be maintained at the AGC output.

3 Stereo AGC Parameter Control

Stereo AGC controls both the left and right channel gains based on the maximum signal strength. Therefore, when changing AGC parameters, it is important to maintain synchronization between the left and right channel gains using a state-machine synchronizer. Otherwise, the left and right channel gain controls become out of sync, and will never recover.

Consider an example. We assume that the stereo AGC is running in steady state and is applying the same gain to the left and right channels. The user now wants to change the target gain for both channels. The target gain values are located in two different registers: Page 0, Register 86, D6-D4 = target gain for left channel; Page 0, Register 94, D6-D4 = target gain for right channel. There will be a slight time difference between the programming of these register control bits. When the target gain for left channel has been changed (and the target gain of the right channel is not yet changed), the left and the right channel AGC state machines will behave differently, and will have a different gain value for each channel. Subsequently, when the target gain for the right channel also changes, both the channel state machines will start running in tandem; but the difference in gain values that was introduced during the transition period will remain. This difference will result in a permanent mismatch of level differences between the two channels at the AGC output. Figure 3 illustrates this effect.

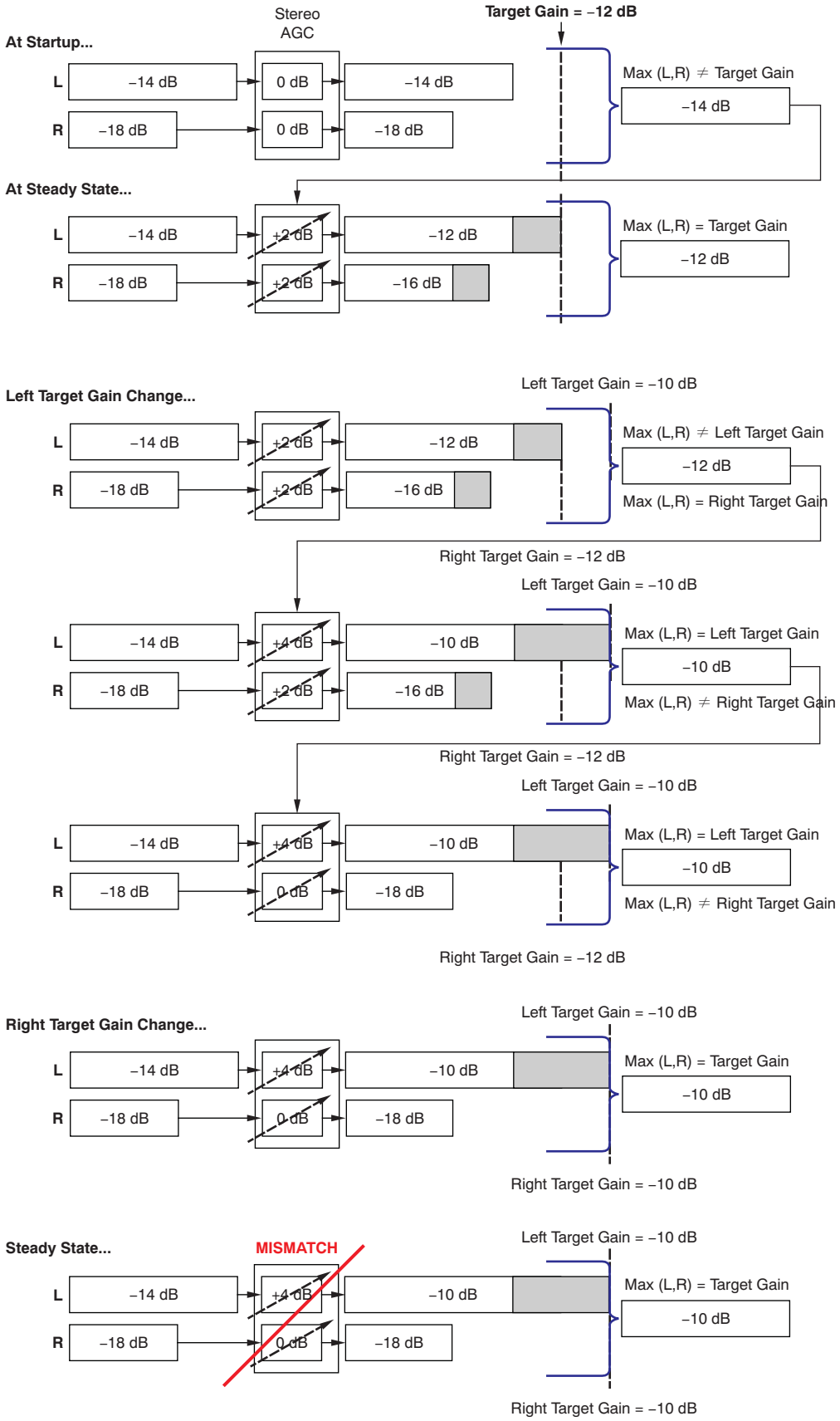

Figure 3. STAGC_R Gain Mismatch

3.1 STAGC_R State Machine Synchronizer

To avoid the gain mismatch described in Section 3, a state machine synchronization sequence is required when an AGC parameter changes on the fly. Table 1 describes this sequence.

Table 1. STAGC_R Synchronization Sequence

Step	Description/Associated Registers
Mute ADC left and right channels	This step ensures that the AGC state machine receives zero input. Register(s): • p0_r82_b7 = 1 (mute left ADC) • p0_r82_b3 = 1 (mute right ADC)
Disable Noise Gate for left and right channels (If originally enabled)	This step ensures that the AGC will perform gain control even with zero input. The applied gain will continue to increase (because input is zero) until it saturates to the maximum programmed AGC gain level. Register(s): • p0_r87_b5-b1 = 00000b (left channel ADC Noise Gate disable, store the original value) • p0_r95_b5-b1 = 00000b (right channel ADC Noise Gate disable, store the original value)
Change desired AGC parameters	
Read Left and Right AGC gain, and wait until they reach maximum programmed AGC gain	This step ensures that both the Left and the Right AGC state machines are synchronous with each other. Flags(s): • p0_r93_b7-b0 = Left Channel AGC Gain (= p0_r88_b6-b0, Left Channel AGC Maximum Gain) • p0_r101_b7-b0 = Right Channel AGC Gain (= p0_r96_b6-b0, Right Channel AGC Maximum Gain)
Enable Noise Detection for left and right channels (If originally enabled)	Register(s): • p0_r87_b5-b1 = Original Value • p0_r95_b5-b1 = Original Value
Unmute ADC left and right channels	The new AGC parameters are in effect. Because the unmute bits for the left and the right ADC channels are in the same register, AGC state machine synchronization is maintained. Register(s) • p0_r82_b7 = 0 (unmute left ADC) • p0_r82_b3 = 0 (unmute right ADC)

4 Using STAGC_R from Control Software

STAGC_R can be evaluated with both the TLV320AIC3254EVM-K and TLV320AIC3254EVM-U control software. This function can be accessed under *miniDSP Apps* > *Stereo AGC*, and is shown in Figure 4.

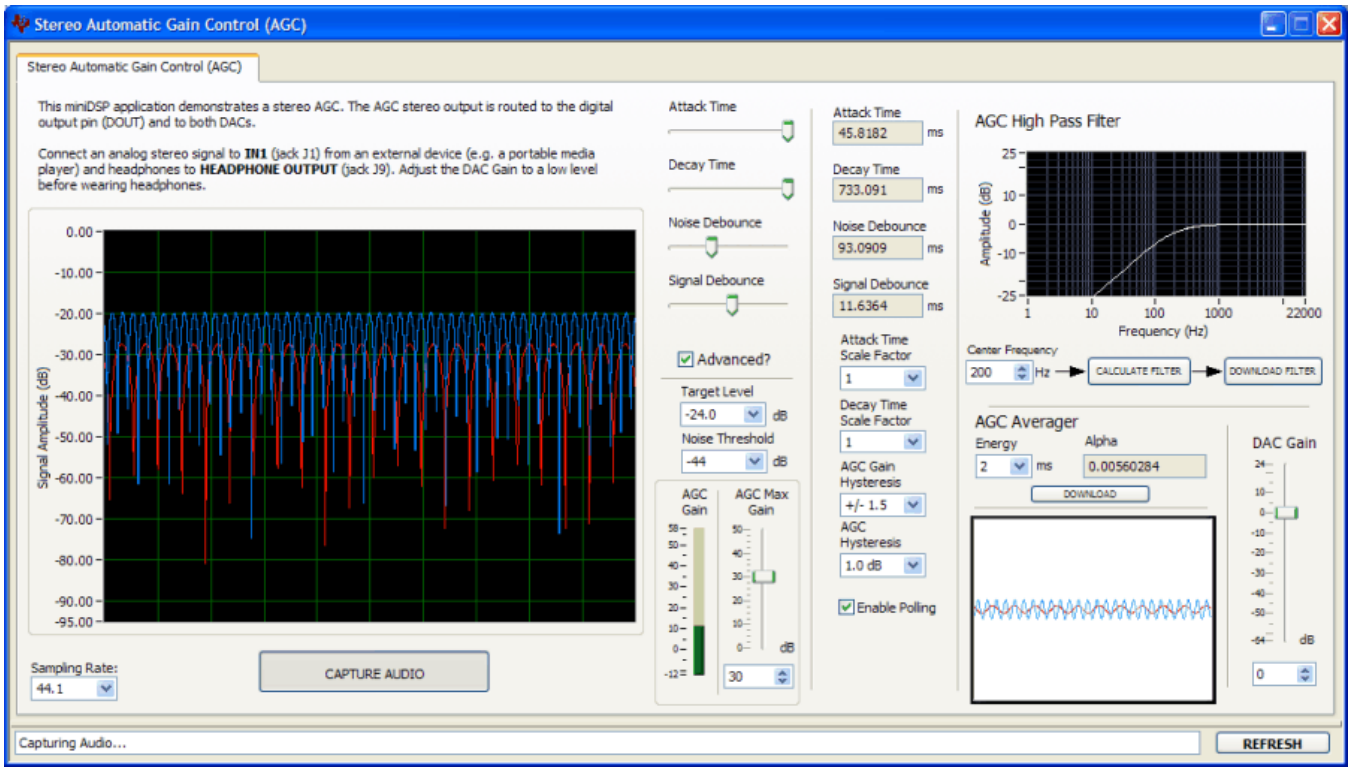

Figure 4. Stereo AGC Panel

In Figure 5, two sinusoids of different amplitude and frequency are fed to each channel through the IN1 inputs. Figure 5 shows the absolute value of the processed waveform in decibels.

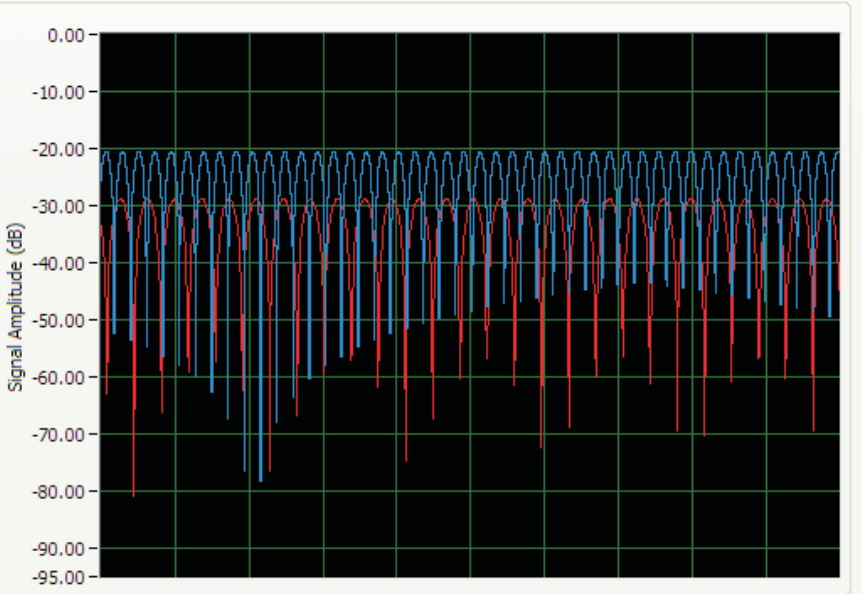

Figure 5. Left Channel (Blue) with Higher Input Level

If the target level is set to –24 dB, the AGC will try to gain (or attenuate) the highest level signal to reach the target level, assuming that the signal is already above the noise threshold. The AGC measures the absolute average value (AAV) of the signal. Figure 5 shows the blue waveform with a peak level of approximately –20 dB, which corresponds to a waveform with an AAV of –24 dB.

The signal with highest amplitude will dominate the AGC level detection. This effect is shown in Figure 6, where the right channel (in red) increases at a level higher than the left channel (blue).

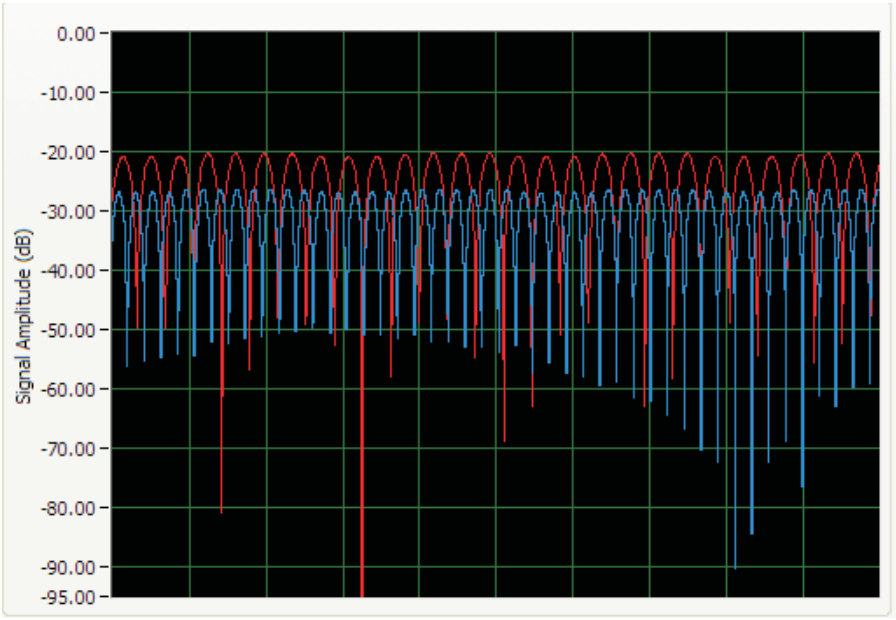

Figure 6. Right Channel (Red) with Higher Input Level

The AGC Max Gain slider, shown in Figure 7, can be modified to limit the amount of gain by which the AGC PGA will increase. This parameter is useful in order to prevent signals that are closer to the noise threshold from gaining too much when trying to reach the target level. The AGC gain flag shows the current value of the AGC gain in real time, and can be enabled by checking the *Enable Polling* box (refer to Figure 4).

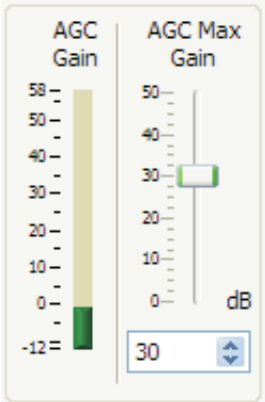

Figure 7. AGC Gain Indicator and AGC Max Gain Control

The AGC will try to gain the PGA in order to reach the target level. However, as noted previously, the target level may not be reached if the AGC Max Gain limits the PGA, or if the signal falls below the noise threshold. Figure 8 shows the Target Level and Noise Threshold Controls.

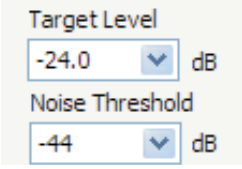

Figure 8. Target Level and Noise Threshold Controls

The Attack, Decay, and Debounce parameters (shown in Figure 9) control the dynamic performance of the AGC. The attack time controls how fast the AGC PGA decreases, while the decay time controls how fast the AGC PGA increases. The signal debounce ignores sudden AAV transients above the noise threshold. The noise debounce ignores sudden AAV transients below the noise threshold. Refer to the TLV320AIC3254 product data sheet for additional details on AGC parameters.

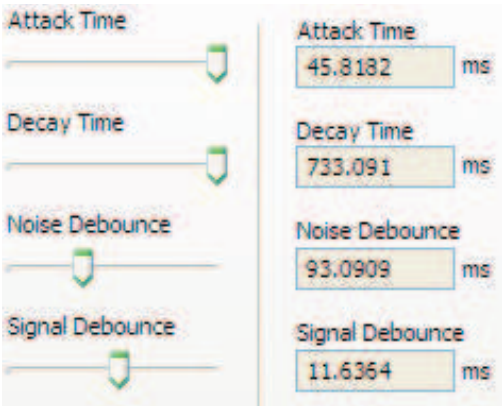

Figure 9. Attack, Decay and Debounce Controls and Indicators

The AGC High-Pass Filter programs the infinite impulse response (IIR) filter shown in Figure 10. To change the high-pass filter response, enter the center frequency, click **Calculate Filter** (which also shows the response in the graph) and then click **Download Filter**. The AGC High-Pass Filter is typically used to block dc offsets and low frequency transients.

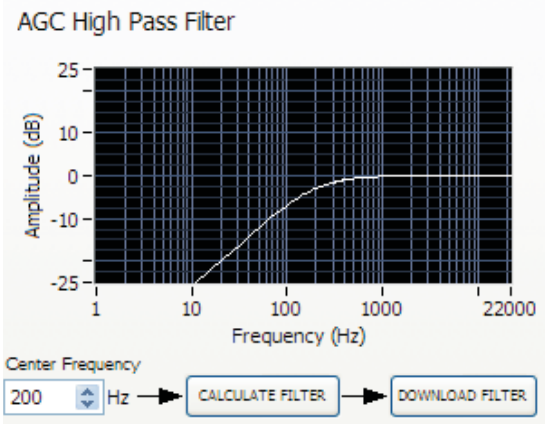

Figure 10. AGC High-Pass Filter

The AGC Absolute Averager (AAV) determines the average level of the input signal. The time constant of the AAV can be set using the controls shown in Figure 11. Normally, the time constant should be approximately 10 to 15 times slower than the time period of the lowest frequency in the signal. This slower rate is required to prevent harmonic distortion of the signal. At the same time, however, the time constant should not be too slow because it could start to modulate the output.

For example, if the lowest frequency is 300 Hz (time period = 3.3 ms), then the AAV time constant should be between 30 ms to 50 ms.

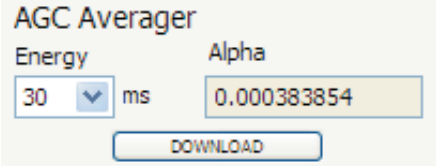

Figure 11. AGC Averager

By changing the value of the sample rate control, all the time-dependent parameters (such as AGC HPF, AGC Averager, Attack Time, Decay Time, and Debounce) are updated in the software graphical user interface (or GUI; refer to Figure 4). Figure 12 shows the updated parameters for an 8-kHz sampling rate. Note that changing the sample rate control only changes the indicators and coefficients for the parameters noted here. The default script only supports 44.1-kHz and 48-kHz operation, but could be modified as needed. To change the USB audio sample rate, see the *Tools > EEPROM Writer* panel in the software GUI.

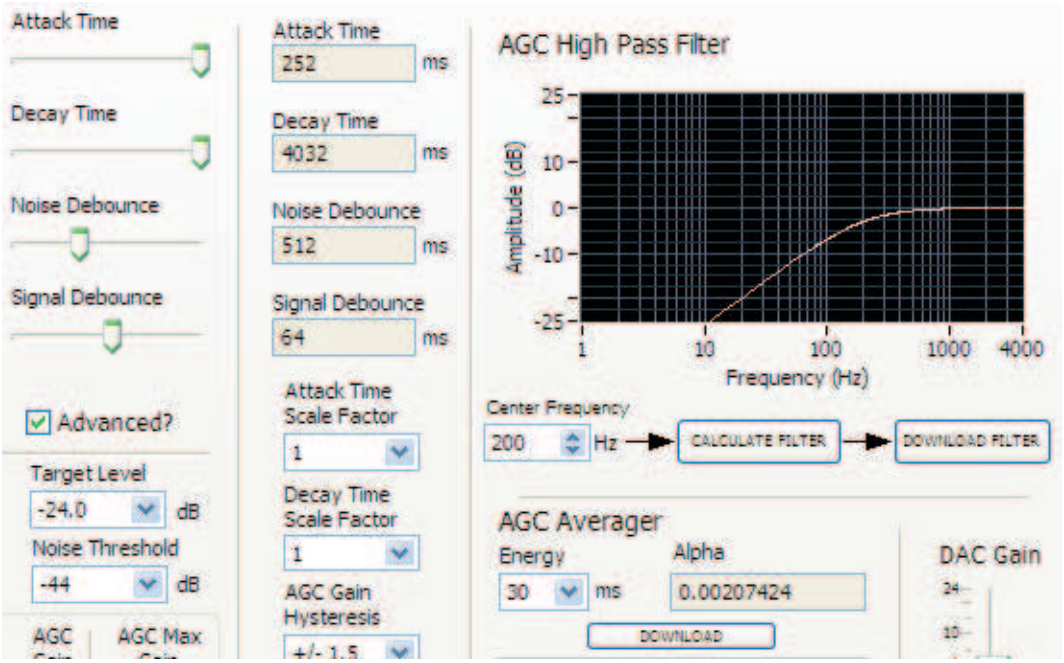

Figure 12. Controls Affected by Sample Rate Change

The initialization code also loops back the ADC data into the digital-to-analog converter (DAC) channel. This feature allows the user to monitor the AGC performance through the headphone out jack. The DAC Gain control (shown in Figure 13) adjusts the volume of the DAC output. It is recommended to not wear headphones until the DAC gain is set to a comfortable listening level.

Figure 13. DAC Gain Control

5 Appendix A. STAGC_R Sample Initialization Script

The script provided in Example 1 contains the miniDSP script required to use the STAGC_R function. In most applications, it is not required to change STAGC_R parameters on the fly. Configuring these parameters beforehand does not require the synchronization sequence as long as these parameters are written before powering the LADC and RADC channels. The entire initialization script can be found in *C:\Program Files\Texas Instruments\AIC3254 CS\DATA\EVM\AIC3254\ST_AGC* of the AIC3254 control software.

Example 1. STAGC_R Sample Initialization Script

```
w 30 00 00 # Switch to Page 0
w 30 01 01 # Initialize the device through software reset

# PLACE MINIDSP CODE HERE

# PLACE DEVICE CONFIGURATION HERE

w 30 00 00 # Switch to Page 0
w 30 56 f3 # Enable left AGC, target level = -24 dB, Hysteresis = +/- 1.5dB
w 30 57 10 # Left AGC Noise Threshold = -60 dB
w 30 58 3c # Left AGC Max Gain = 30 dB
w 30 59 f8 # Left AGC Attack Time = 45 ms. (63*(32/Fs))
w 30 5a f8 # Left AGC Decay Time = 730 ms. (63*(512/Fs))
w 30 5b 0b # Left AGC Noise Debounce Time = 93 ms. (4096/Fs)
w 30 5c 08 # Left AGC Signal Debounce Time = 11 ms. (512/Fs)
w 30 5e f3 # Enable right AGC, target level = -24 dB, Hysteresis = +/- 1.5dB
w 30 5f 10 # Right AGC Noise Threshold = -60 dB
w 30 60 3c # Right AGC Max Gain = 30 dB
w 30 61 f8 # Right AGC Attack Time = 45 ms. (63*(32/Fs))
w 30 62 f8 # Left AGC Decay Time = 730 ms. (63*(512/Fs))
w 30 63 0b # Right AGC Noise Debounce Time = 93 ms. (4096/Fs)
w 30 64 08 # Right AGC Signal Debounce Time = 11 ms. (512/Fs)
w 30 51 c0 # Powerup ADC left and right channels
w 30 52 00 # Unmute ADC left and right channels
```

For both STAGC_R and standard AGC, the sequence given in Example 2 should be followed when shutting down the ADCs.

Example 2. General ADC Channel Shutdown Procedure

```
…
…
…
# -- Disable AGCs
w 30 00 00 # Switch to Page 0
w 30 52 88 # Mute LADC/RADC to prevent gain change artifacts
w 30 57 00 # Disable LAGC noise gate
w 30 56 00 # Disable LAGC
w 30 5f 00 # Disable RAGC noise gate
w 30 5e 00 # Disable RAGC
# -- Power off ADCs
w 30 51 00 # Power off LADC/RADC
…
…
```

6 Appendix B. STAGC_R Example Scripts

The script in Example 3 illustrates how to change the target level on the fly. These parameters are assumed:

- LAGC/RAGC Max Gain = 30dB (p0_r88_b6-b0 / p0_r96_b6-b0)
- LAGC/RAGC Noise Threshold Enabled and set to -70dB (p0_r87_b5-b1 / p0_r95_b5-b1)

Example 3. STAGC_R Target Level Change Example

```
# -- A change in target level of -12dB is desired:
w 30 00 00 # Switch to Page 0
w 30 52 88 # Mute LADC/RADC
w 30 57 00 # Disable LAGC Noise Threshold, keep LAGC Hysteresis at 1dB
w 30 5F 00 # Disable RAGC Noise Threshold, keep RAGC Hysteresis at 1dB
w 30 56 B3 # Set LAGC Target Level = -12dB
w 30 5E B3 # Set RAGC Target Level = -12dB
f 30 5D 00111100 # Wait for LAGC Gain flag to reach LAGC Max Gain (00111100 = 30dB)
f 30 65 00111100 # Wait for RAGC Gain flag to reach LAGC Max Gain (00111100 = 30dB)
w 30 57 2A # Re-enable LAGC Noise Threshold = -70dB, keep LAGC Hysteresis at 1dB
w 30 5F 2A # Re-enable RAGC Noise Threshold = -70dB, keep RAGC Hysteresis at 1dB
w 30 52 88 # Un-mute LADC/RADC
```

The script presented in Example 4 can be executed afterwards if it is desired to change the STAGC_R Maximum Allowed Gain to 40 dB (instead of 30 dB).

Example 4. STAGC_R Maximum Allowed Gain Change Example

```
# -- A change in maximum AGC allowed gain of 40dB is desired:
w 30 00 00 # Switch to Page 0
w 30 52 88 # Mute LADC/RADC
w 30 57 00 # Disable LAGC Noise Threshold, keep LAGC Hysteresis at 1dB
w 30 5F 00 # Disable RAGC Noise Threshold, keep RAGC Hysteresis at 1dB
w 30 58 50 # Set LAGC Max Gain = 40dB
w 30 60 50 # Set RAGC Max Gain = 40dB
f 30 5D 01010000 # Wait for LAGC Gain flag to reach LAGC Max Gain (01010000 = 40dB)
f 30 65 01010000 # Wait for RAGC Gain flag to reach LAGC Max Gain (01010000 = 40dB)
w 30 57 2A # Re-enable LAGC Noise Threshold = -70dB, keep LAGC Hysteresis at 1dB
w 30 5F 2A # Re-enable RAGC Noise Threshold = -70dB, keep RAGC Hysteresis at 1dB
w 30 52 88 # Un-mute LADC/RADC
```

Note that it is not necessary to perform this sequence for each parameter individually. A group of parameters can be grouped together as long as the sequence described in Table 1 is followed. This approach is shown in Example 5, where all the AGC parameters are programmed. Note that the MCU should keep track of the STAGC_R Max Gain programmed in Registers 0x58 and 0x60 when reading Registers 0x5D and 0x65, as shown below.

Example 5. STAGC_R All Parameter Change

```
# -- Mute ADCs and disable noise threshold:
w 30 00 00 # Switch to Page 0
w 30 52 88 # Mute LADC/RADC
w 30 57 40 # Disable LAGC Noise Threshold, Hysteresis = 2dB
w 30 5F 40 # Disable RAGC Noise Threshold, Hysteresis = 2dB
# -- Begin STAGC_R parameter change
w 30 56 12 # Set LAGC Target Level = -8dB, Gain Hysteresis = 1dB
w 30 5E 12 # Set RAGC Target Level = -8dB, Gain Hysteresis = 1dB
w 30 58 28 # Set LAGC Max Gain = 20dB
w 30 60 28 # Set RAGC Max Gain = 20dB
w 30 59 10 # Set LAGC Attack = 5*32 ADC_FS cycles, scale factor = 1
w 30 61 10 # Set RAGC Attack = 5*32 ADC_FS cycles, scale factor = 1
w 30 5A 10 # Set LAGC Decay = 5*512 ADC_FS cycles, scale factor = 1
w 30 62 10 # Set RAGC Decay = 5*512 ADC_FS cycles, scale factor = 1
w 30 5B 01 # Set LAGC Noise Debounce = 4 ADC_FS cycles
w 30 63 01 # Set RAGC Noise Debounce = 4 ADC_FS cycles
w 30 5C 01 # Set LAGC Signal Debounce = 4 ADC_FS cycles
w 30 64 01 # Set RAGC Signal Debounce = 4 ADC_FS cycles
# -- End STAGC_R parameter change
f 30 5D 00101000 # Wait for LAGC Gain flag to reach LAGC Max Gain (00101000 = 20dB)
f 30 65 00101000 # Wait for RAGC Gain flag to reach LAGC Max Gain (00101000 = 20dB)
w 30 57 74 # Re-enable LAGC Noise Threshold = -80dB, Hysteresis = 2dB
w 30 5F 74 # Re-enable RAGC Noise Threshold = -80dB, Hysteresis = 2dB
w 30 52 88 # Un-mute LADC/RADC
```

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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