Application Report
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Upgrading From the ADS7813 to the ADS8513

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ABSTRACT

This application report applies to current designs using the Texas Instruments ADS7813 device in a surface-mount SO-16 (DW) package. This document guides users of the ADS78xx device, with regards to potential compatibility issues that can be encountered when upgrading to the new ADS85xx part series.

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1 Package and Pin Compatibility

The ADS8513 device is designed to be fully pin-compatible with the surface mount SO-16 (DW package) version of the ADS7813 device. The updated chip features the same 40-KSPS throughput and the same analog input ranges with slightly lower power dissipation.

This table is hyperlinked to provide easy access to the associated ADS7813 and ADS8513 device data sheets. As new family products are added, this table will expand to include new part numbers.

Current ADS78xx Family	New ADS85xx Family
ADS7813 – SBAS043	ADS8513 – SLAS486

2 Electrical Compatibility

This section describes potential electrical compatibility issues.

2.1 Absolute MAX Voltage Input Changes

The new ADS85xx devices differ in the maximum working supply voltage as Table 1 shows.

Table 1. Maximum Working Supply Voltage Differences

ADS78xx MAX Voltage Specification	
V_{ANA}	7 V
V_{DIG}	7 V
ADS85xx MAX Voltage Specification	
V_{ANA}	6 V
V_{DIG}	6 V

2.2 Input Impedance and Capacitance Changes

The new ADS85xx devices have the same typical input impedance based on the input range, but have different input capacitance features. The major differences are noted in Table 2.

Table 2. Different Input Capacitance Features

PARAMETER	CONDITIONS (See Device Data Sheet)	78 SERIES			85 SERIES			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
ADSxx13								
Capacitance			35			45		pF

2.3 Performance Compatibility

The new ADS8513 device has performance characteristics that meet or exceed the specifications listed in the ADS7813 device data sheet (SBAS043). Primary interest regarding specific improvements depends on the actual application, but in general, all AC and DC specifications remain the same.

3 Functional and Timing Differences

These sections discuss the functionality and timing differences between the ADS7813 and ADS8513 devices.

3.1 Functional Compatibility

The ADS8513 device retains the same basic functionality of the ADS7813. There are no differences in the start of a conversion cycle or reading conversion data through the serial interface.

3.2 Timing Compatibility

Timing changes related to the ADS8513 device are discussed in detail throughout the Comparison of the ADS7813 and ADS8513 Basic Conversion Timing Characteristics section. Depending on the specific application, these timing changes may affect the drop in replacement or ease of use in designs or end systems currently using the ADS7813. A careful review of Table 3 through Table 8 will highlight the ADS7813 and ADS8513 timing differences.

3.3 Comparison of the ADS7813 and ADS8513 Basic Conversion Timing Characteristics

Table 3 provides a side-by-side comparison of the basic conversion timing differences between the ADS7813 and the ADS8513. The **bold text** items show the timing differences which are most likely to have an impact on current ADS7813 serial interface designs.

Table 3. Comparison of Basic Timing Characteristics

SYMBOL	DESCRIPTION	ADS7813			ADS8513			UNIT
ADS7813 / ADS8513		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Conversion Plus Acquisition Time			25			25	µs
t2	**$\overline{\text{CONV}}$ LOW to All Digital Inputs Stable**			**8**			**19**	µs
t3	**$\overline{\text{CONV}}$ LOW to Initiate a Conversion**	0.04			0.04		12	µs
t4	**$\overline{\text{BUSY}}$ Rising to Any Digital Input Active**	**0**			**5**			ns
t5	**$\overline{\text{CONV}}$ HIGH Prior to Start of Conversion ($\overline{\text{CONV}}$ high time)**	**2000**			**15**			ns
t6	$\overline{\text{BUSY}}$ LOW		19	20		18	20	µs
t7	**$\overline{\text{CONV}}$ LOW to $\overline{\text{BUSY}}$ LOW**		**85**	**120**		12	20	ns
t8	**Aperture Delay ($\overline{\text{CONV}}$ falling edge to actual conversion start)**		**40**			**5**		ns
t9	Conversion Time		18	20		18	20	µs
t10	**Conversion Complete to $\overline{\text{BUSY}}$ Rising**		**1.1**	**2**		**90**		ns
t11	**Acquisition Time**			**5**		**7**		µs

3.4 Comparison of ADS7813 and ADS8513 Internal Clock Serial Data Timing Characteristics

Table 4 provides a side-by-side comparison of the serial timing differences between the ADS7813 and the ADS8513 when using the internal conversion clock (read previous data during conversion). Refer to the Using the Internal Serial Clock section for other potential application issues. The **bold text** items show the timing differences which are most likely to have an impact on current ADS7813 serial interface designs when using the internal data clock feature of the devices.

Table 4. Serial Timing Differences When Using Internal Clock (EXT/$\overline{\text{INT}}$ and $\overline{\text{CS}}$ LOW)

SYMBOL	DESCRIPTION	ADS7813			ADS8513			UNIT
ADS7813 / ADS8513		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Conversion Plus Acquisition Time			25			25	µs
t12	**$\overline{\text{CONV}}$ LOW to Rising Edge of First Internal DATACLK**		**1.4**			**2.0**		µs
t13	**Internal DATACLK HIGH**	**250**	**350**	**500**	**300**	**410**	**425**	ns
t14	**Internal DATACLK LOW**	**600**	**760**	**875**	**300**	**410**	**425**	ns
t15	**Internal DATACLK Period**		**1.1**		**0.6**	**0.82**	**0.85**	µs
t16	**DATA Valid to Internal DATACLK Rising**	**20**			**150**	**204**		ns
t17	**Internal DATACLK Falling to DATA Not Valid**	**400**			**150**	**208**		ns
t18	**Falling Edge of Last DATACLK to $\overline{\text{BUSY}}$ Rising**		**0.8**			**4.4**	**5**	µs

3.5 Comparison of ADS7813 and ADS8513 External Data Clock Serial Timing Characteristics

The next four sections show the timing relationships of the ADS7813 and ADS8513 with the application of an external serial I/O clock. Refer to the Using the External Serial Clock section for other potential application issues.

3.5.1 Reading Data After a Conversion Completes

Table 5 provides a side-by-side comparison of the serial timing differences between the ADS7813 and the ADS8513 when using an external clock to read data after a conversion cycle is completed. The **bold text** items show the timing differences which are most likely to have an impact on current ADS7813 designs.

Table 5. Serial Timing, External Clock, Clocking After the Conversion Completes (EXT/$\overline{INT}$ and $\overline{CS}$ LOW)

SYMBOL	DESCRIPTION	ADS7813			ADS8513			UNIT
ADS7813 / ADS8513		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Conversion Plus Acquisition Time			25			25	µs
t4	**$\overline{BUSY}$ Rising to Any Digital Input Active**	**0**			**5**			ns
t5	**$\overline{CONV}$ HIGH Prior to Start of Conversion $\overline{CONV}$ (high time)**	**2000**			**15**			ns
t19	**External DATACLK Rising to DATA Not Valid**	**15**			**4**	**14**		ns
t20	**External DATACLK Rising to DATA Valid**		**55**	**85**	**2**	**12**	**20**	ns
t21	**External DATACLK HIGH**	**50**			**15**			ns
t22	**External DATACLK LOW**	**50**			**15**			ns
t23	**External DATACLK Period**	**100**			**35**			ns

3.5.2 Read Data During the Next Conversion

Table 6 provides a side-by-side comparison of the serial timing differences between the ADS7813 and the ADS8513 when using an external clock to read previous conversion results during the current conversion cycle. The **bold text** items show the timing differences which are most likely to have an impact on current ADS7813 serial interface designs when using this operating mode.

Table 6. Serial Timing, External Clock, Clocking During the Next Conversion (EXT/$\overline{INT}$ and $\overline{CS}$ LOW)

SYMBOL	DESCRIPTION	ADS7813			ADS8513			UNIT
ADS7813 / ADS8513		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Conversion Plus Acquisition Time			25			25	µs
t2	**$\overline{CONV}$ LOW to All Digital Inputs Stable**			**8**			**19**	µs
t19	**External DATACLK Rising to DATA Not Valid**	**15**			**4**	**14**		ns
t20	**External DATACLK Rising to DATA Valid**		**55**	**85**	**2**	**12**	**20**	
t21	**External DATACLK HIGH**	**50**			**15**			ns
t22	**External DATACLK LOW**	**50**			**15**			ns
t23	**External DATACLK Period**	**100**			**35**			ns
t24	**$\overline{CONV}$ LOW to External DATACLK Active**	**100**			**15**			ns
t25	**External DATACLK LOW or $\overline{CS}$ HIGH to $\overline{BUSY}$ Rising**	**2**					**1**	µns

3.5.3 Read Data After Conversion and During the Next Conversion

Table 7 provides a side-by-side comparison of the serial timing differences between the ADS7813 and the ADS8513 when using an external clock to read data which spans two acquisition cycles. The **bold text** items show the timing differences which are most likely to have an impact on current ADS7813 serial interface designs when using an external serial clock to read data in this manner.

Table 7. Serial Timing, External Clock, Clocking After the Conversion Completes and During the Next Conversion (EXT/$\overline{INT}$ and $\overline{CS}$ LOW)

SYMBOL	DESCRIPTION	ADS7813			ADS8513			UNIT
ADS7813 / ADS8513		MIN	TYP	MAX	MIN	TYP	MAX	
t4	**$\overline{BUSY}$ Rising to Any Digital Input Active**	**0**			**5**			ns
t5	**$\overline{CONV}$ HIGH Prior to Start of Conversion ($\overline{CONV}$ high time)**	**2000**			**15**			ns
t24	**$\overline{CONV}$ LOW to External DATACLK Active**	**100**			**15**			ns
t25	**External DATACLK LOW or $\overline{CS}$ HIGH to $\overline{BUSY}$ Rising**	**2**					**1**	µs

3.6 Chip Select Timing

Table 8 provides a comparison of the chip select timing differences between the ADS7813 and the ADS8513. The $\overline{CS}$ input allows the digital outputs of the ADS78/8513 to be disabled and gates the external DATACLK signal when EXT/$\overline{INT}$ is HIGH.

Table 8. $\overline{CS}$ Timing

SYMBOL	DESCRIPTION	ADS7813			ADS8513			UNIT
ADS7813 / ADS8513		MIN	TYP	MAX	MIN	TYP	MAX	
t26	**$\overline{CS}$ LOW to Digital Outputs Enabled**	**85**			**15**			ns
t27	**$\overline{CS}$ HIGH to Digital Outputs Disabled**	**85**			**15**			ns

4 Potential Application Issues

4.1 Using the Internal Serial Clock

When operating the new ADS8513 device in the internal DATACLK operating mode, a user may notice an impact on reading serial data either on the rising clock or on the falling clock edges. In the ADS7813 device, the internal data clock was framed by the output data to provide significantly longer valid data times with respect to the rising clock edge. With the ADS8513, valid data times with respect to the rising clock edge are reduced from 760 ns typical to 410 ns typical. Valid data with respect to the falling clock edge have increased by 60 ns typical.

4.2 Using the External Serial Clock

When operating the new ADS8513 device with an external serial clock, it is important to ensure the clock is low at the application of the $\overline{\text{CONV}}$ signal. The ADS8513 operates properly when configured with an SPI processor using CPOL=0 and CPHA=1 (SCLK dwells low and data is read on the falling SCLK). The ADS7813 device released its MSB regardless of the state of the SCLK upon the application of $\overline{\text{CONV}}$, the ADS8513 does not release the MSB if SCLK is high when $\overline{\text{CONV}}$ goes low.

4.3 Multiplexed Analog Inputs

Applications that require multiple channels often do so by adding a multiplexor to the analog input of the ADC. Multiplexed input applications should avoid switching the analog input during the conversion process as noise on the input could degrade the conversion results. To avoid potential issues, consider using the rising edge of BUSY to signal the analog multiplexer.

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