Application Report

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Set Up and Use TSC Timings

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ABSTRACT

This application report helps users to understand, set up, and use the programming timings in the register-based touch screen controller (TSC) devices. It displays the timings functions and discusses the effect on the system interface traffic and on the system power consumption.

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1 Introduction

Texas Instruments produces a family of high-performance, resistive touch screen controller (TSC) devices, such as ADS7846 or TSC2005.

A TSC device goes between a resistive touch screen (panel) and a host processor. The panel functions as the touch sensor, and the processor usually is the center of multiple tasks/functions in an application or product.

Figure 1 is a typical 4-wire, resistive TSC system. A TSC device has two interfaces: the analog interface is the connection to the panel, and the digital interface is the bridge to the processor.

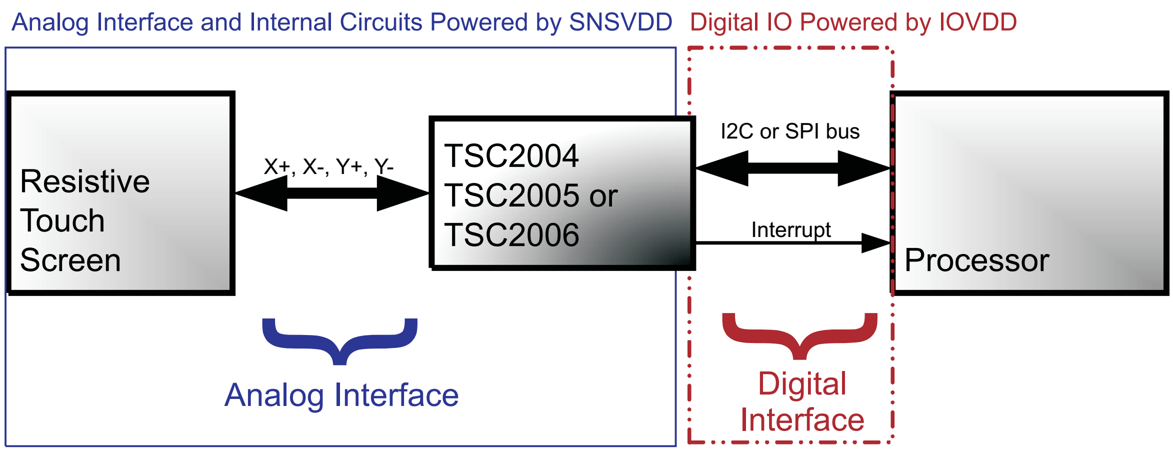

Figure 1. Block Diagram of a Touch Screen System Using TI's TSC2004/5/6 Device

TI's TSC devices were designed with inventive features and many advantages such as:

- Acquiring precise and reliable touch data
- Cutting power consumption of the touch screen system
- Reducing the interference and overhead to the processor

This application report focuses only on the functions and characteristics of several programmable timings, featured in the register-based TI TSC devices, such as the TSC2004, the TSC2005, and the TSC2006. These programmable timings significantly affect the analog interface and should be set up to optimize the entire system's performance.

2 Touch Panel Driving Power

On a resistive touch screen system, the touch panel's driving current, provided by the TSC device through the analog interface, has the highest impact on the power consumption in the touch screen system. This touch panel power consumption is decided by the touch panel's resistance and the TSC power supply (SNSVDD) voltage. Figure 2 shows the relationship. The touch screen is driven by the touch screen controller from the giving SNSVDD, and the panel's resistance determines the peak drive current.

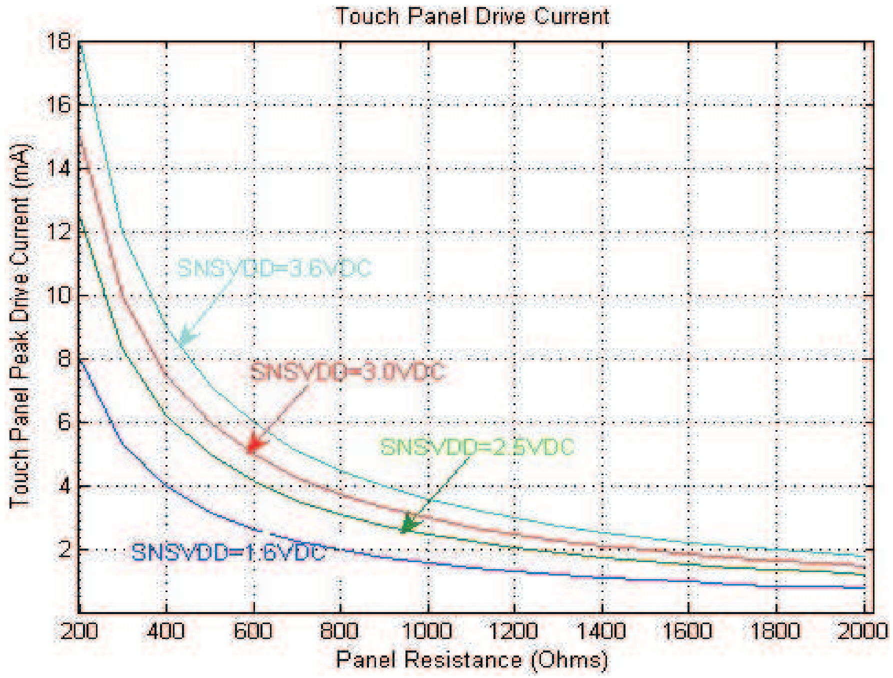

Figure 2. Touch Panel Power Consumption

Figure 2 considers only the ideal TSC driving condition where the TSC's internal resistance is ignored because it is small (5 Ω to 6 Ω) comparing to the touch panel's resistance (100s to 1000s Ω). Thus, the actual power consumption in practice should be a little less than that shown in Figure 2.

A user can reduce power consumption in three ways:

1. Use touch screens with higher resistance
2. Use low power supply SNSVDD to the TSC
3. Reduce the driver-ON time or the driver's ON/OFF ratio.

Touch panels with higher resistance are likely to cause more noise and longer settling time, which limits selection options for users.

The TSC2004/5/6 has the lowest power supply requirement in today's market. The TSC2004/5/6 is designed with its power supply SNSVDD in the range of 1.6 Vdc to 3.6 Vdc and can still function well with the SNSVDD power supply as low as 1.4 Vdc.

To reduce the driver-ON time involves setting various touch screen timings and delays, which is the main topic of this application report. Table 1 lists relevant parameters concerning these timings and delays. The sections that follow detail their functions and effects.

Table 1. TSC2004/5/6 CFR (Configuration Registers) Timing Settings

Settings	Location	Description	How to Effect Power
CL1~CL0	D12~D11 of CFR0	ADC Conversion Clock Control: CL1~CL0 = 00b — $f_{ADC} = f_{OSC}$ CL1~CL0 = 01b — $f_{ADC} = f_{OSC}/2$ CL1~CL0 = 10b — $f_{ADC} = f_{OSC}/4$	Faster f_{ADC} (CL1~CL0 = 00b) uses shorter time and thus less SNSVDD power
PV2~PV0	D10~D8 of CFR0	Panel Voltage Stabilization (PVS) Time Control: (Time between panel driver ON and starting sample) From 0 µs (PV2~PV0 = 000b) to 100 ms (PV2~PV0 = 111b)	Shorter PVS time PV2~PV0 = 000b) uses shorter driver ON time and thus less SNSVDD power

Table 1. TSC2004/5/6 CFR (Configuration Registers) Timing Settings (continued)

Settings	Location	Description	How to Effect Power
PR2~PR0	D7~D5 of CFR0	TSC wait-time to allow the pin's capacitance to be fully precharged From 20 µs (PR2~PR0 = 000b) to 1.364 ms (PR2~PR0 = 111b)	Not consuming extra SNSVDD power
SN2~SN0	D4~D2 of CFR0	TSC wait-time to sense if the screen is touched after converting a touch coordinate. From 32 µs (SN2~SN0 = 000b) to 2.656 ms (SN~SN0 = 111b)	Not consuming extra SNSVDD power
BTD2–BTD0	D2~D0 of CFR1	Batch Delay Timing	Discussed by a separate application report on TSC Operation Schemes (SLAA359)

3 Effect of ADC Clock

A TSC2004/5/6 device contains a nominal 4-MHz internal clock, which is used to drive the state machines inside the device that performs the many functions. This clock is divided down to provide a clock to run the SAR A/D converter. If the 4-MHz clock is used directly (divided by 1), the A/D converter is limited to a 10-bit resolution; using higher resolutions at this speed does not result in accurate conversions. The 12-bit resolution requires that the conversion clock run at either 2 MHz (divided by 2) or 1 MHz (divided by 4).

The division ratio for the ADC clock is set in the configuration register 0 or CFR0, by CL1 and CL0 bits. See CL1~CL0 in Table 1.

The ability to change the conversion clock rate allows the user to choose the optimal value for the ADC resolution, speed, and power dissipation. Higher clock frequency results in faster touch data converting speed, shorter touch driver-ON time, and thus usually lower SNSVDD power consumption.

Figure 3 and Figure 4 shows an example on the ADC clock's effect on the analog interface traffic, i.e., X+, X–, Y+, and Y- lines. In these illustrations, a TSC drives the touch panel to acquire X, Y, Z1, and Z2 coordinates, and three samples per coordinate. Figure 3 is an analog interface with the clock frequency set to 2 MHz; Figure 4 has a 1-MHz clock frequency. In Figure 3 and Figure 4, other than the ADC clock frequency difference, all other settings were completely identical, that is, PVS = 0 µs, PR = 20 µs, and SN = 32 µs (these timers are discussed in the next section).

The ADC clock frequency determines the length of the TSC acquisition time and TSC driver-ON time. The faster the ADC clock, the shorter the driver is on. For example, sampling 3 Y data with ADC clock = 2 MHz uses only about 1/2 time comparing to that with ADC clock = 1 MHz, comparing Figure 3 to Figure 4.

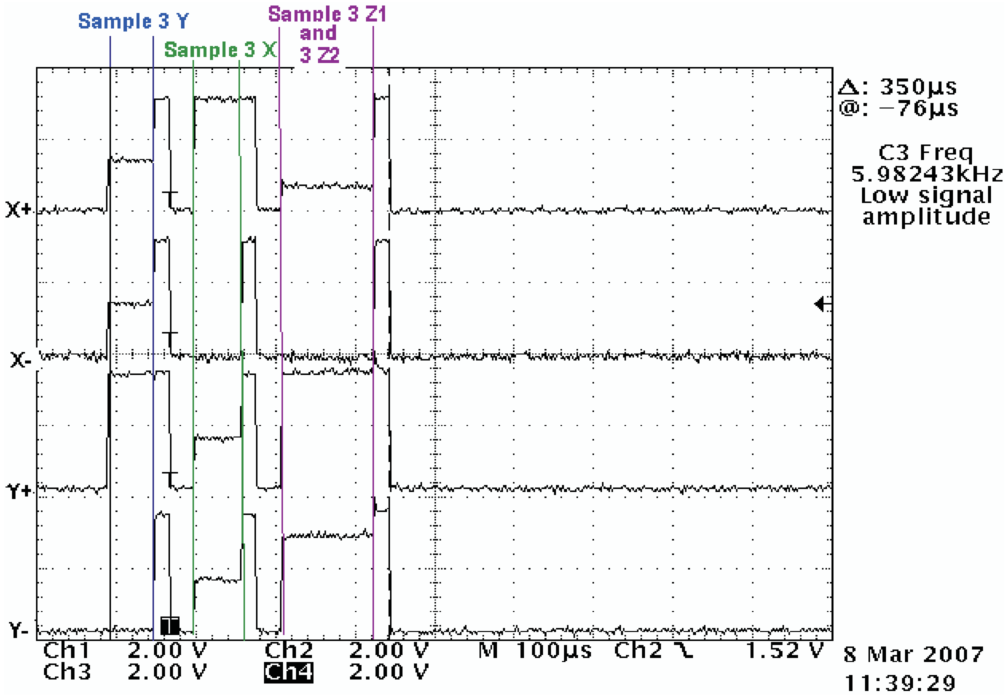

Figure 3. Analog Interface Under ADC Clock = 2 MHz

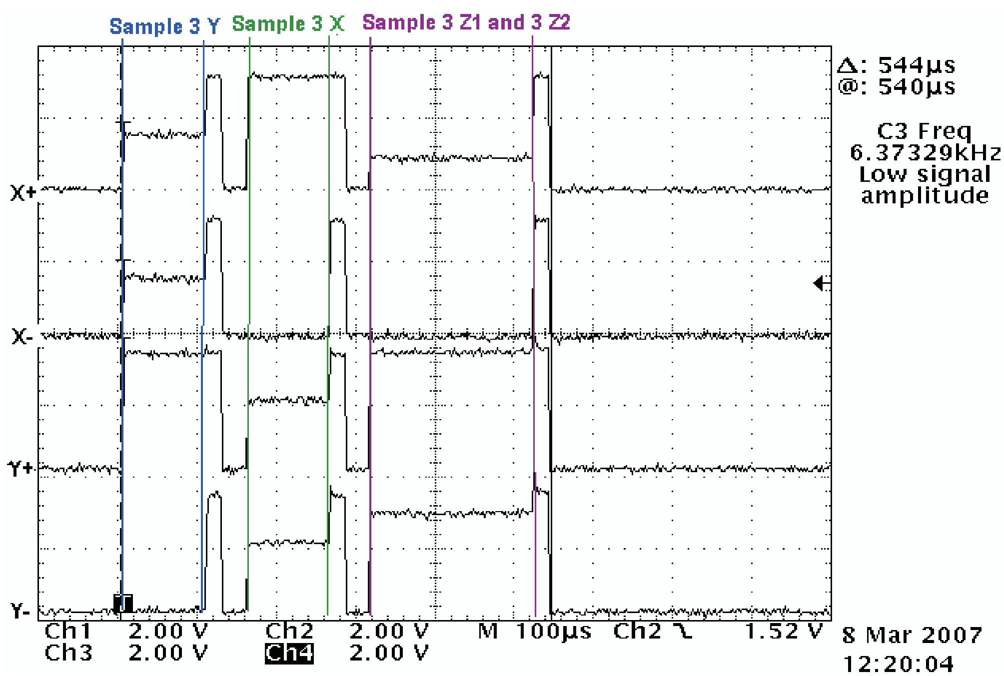

Figure 4. Analog Interface Under ADC Clock = 1 MHz

Mathematically, the analog power supply SNSVDD current can be expressed by.

$$I = f(V_{SNSVDD}) + \left(\frac{V_{SNSVDD}}{R}\right) \times \left(\frac{SSPS \times S \times B}{F}\right) \tag{1}$$

Where, I denotes the SNSVDD current, and it includes two parts: the internal circuitry power consumption or f(VSNSVDD); and the current to drive the external resistive touch panel or as expressed in Equation 1 that $V_{SNSVDD}/R \times SSPS \times S \times B / F$.

In Equation 1:

V_{SNSVDD} is the SNSVDD voltage (in V);

R is the touch panel's average resistance (in Ω);

SSPS is S*ample Sets Per Second*, which indicates how many sets of touch data the host gets within a second;

S is the number of data in a set of samples;

B is the TSC resolution, either 10 bit or 12 bit; and

F is ADC clock frequency, which can be 4, 2, or 1 MHz.

A concern for using the faster ADC clock is due to the analog interface's settling timing or transients; the higher clock frequency may reduce the data's accuracy in those cases where the TSC starts its data acquisitions before the analog interface lines reach the stable voltages. Therefore, it may be necessary to add some delays on the analog interface in order to wait for the interface to become stable before an ADC starts working. These delays may include the panel voltage stabilization time, the pins' precharge time, and/or the sense time, as is discussed next.

4 Panel Voltage Stabilization Time

Panel voltage stabilization (PVS) time specifies a delay time from the moment the touch screen drivers are enabled, to the time the voltage is sampled and a conversion is started. These bits allow the user to adjust the appropriate settling time for the touch panel based on the external capacitances at the analog interface lines.

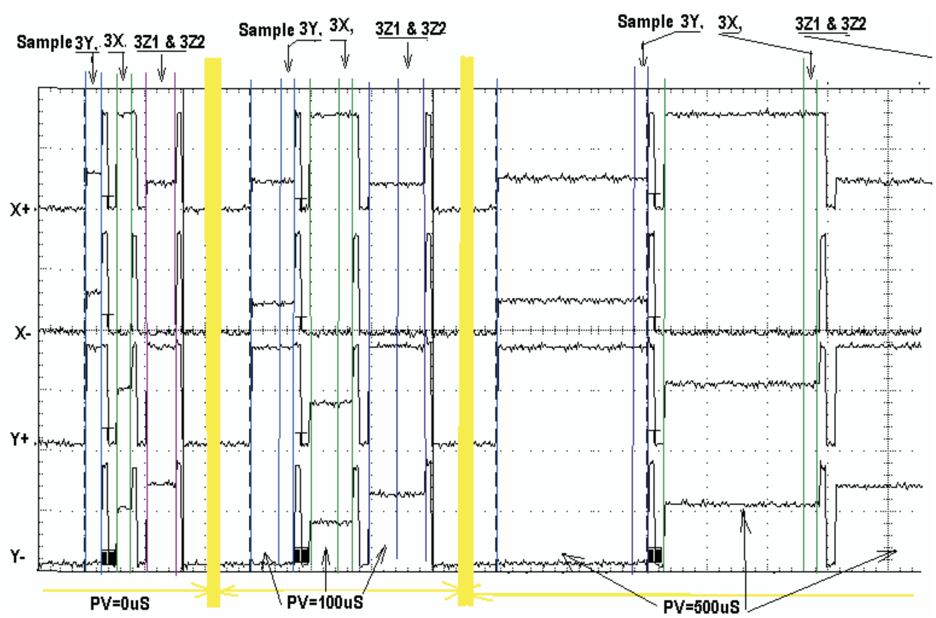

Figure 5. Panel Voltage Stabilization 0 µs, 100 µs, and 500 µs

Figure 5 shows examples where with PVS = 0 µs (no PVS delay), 100 µs, and 500 µs. In the examples, the TSC takes the sets of 4 x 3 = 12 data, and they are 3 X, 3 Y, 3 Z1, and 3 Z2. Because TSC2004/5/6 always performs the Y coordinate first when it was set to X/Y or X/Y/Z scan mode, the sequence for getting a set of samples in Figure 5 is:

- TSC adds driver power to Y+ (SNSVDD) and Y- (AGND); waits PVS µs; and acquires 3 Y data;
- TSC adds driver power to X+ (SNSVDD) and X- (AGND); waits PVS µs; and acquires 3 X data; and
- TSC adds driver power to Y+ (SNSVDD) and X- (AGND); waits PVS µs; and acquires 3 Z1 and 3 Z2 data.

The PVS delay consumes power because a driver is ON during the PVS delay. The power can be expressed as:

$$I_{PVS} = \left(\frac{V_{SNSVDD}}{R}\right) \times SSPS \times PVS \times 3 \tag{2}$$

Where PVS is the PVS delay/wait time and 3 here is due to X, Y, and Z driver ON. Thus, a complete expression of analog power consumption can be, based on Equation 1:

$$I = f(V_{SNSVDD}) + \left[\frac{V_{SNSVDD}}{R} \times SSPS \times \left(\frac{S \times B}{F} + 3 \times PVS\right)\right] \tag{3}$$

for X/Y/Z 3-dimension coordinates. Similarly, for X/Y 2-dimension touch data, it becomes:

$$I = f(V_{SNSVDD}) + \left[\frac{V_{SNSVDD}}{R} \times SSPS \times \left(\frac{S \times B}{F} + 2 \times PVS\right)\right] \tag{4}$$

5 Other TSC Timings

Unlike the ADC clock frequency (CL1~CL0) and panel voltage stabilization time (PV2~PV0), the other two TSC timings in CFR0 (Table 1) affect the bus shape and traffic speed but do not effect power consumption of the analog interface.

As can be seen in Figure 5 that there are some *added* time/delay between samplings of two coordinates, such as the time after sampling Y and before X driver ON, which are the precharge time (PR2~PR0) and sense time (SN2~SN0).

The precharge time (PR2~PR0) sets the amount of time allowed for precharging any pin capacitance on the touch screen during the TSC ADC conversions as shown by Figure 6.

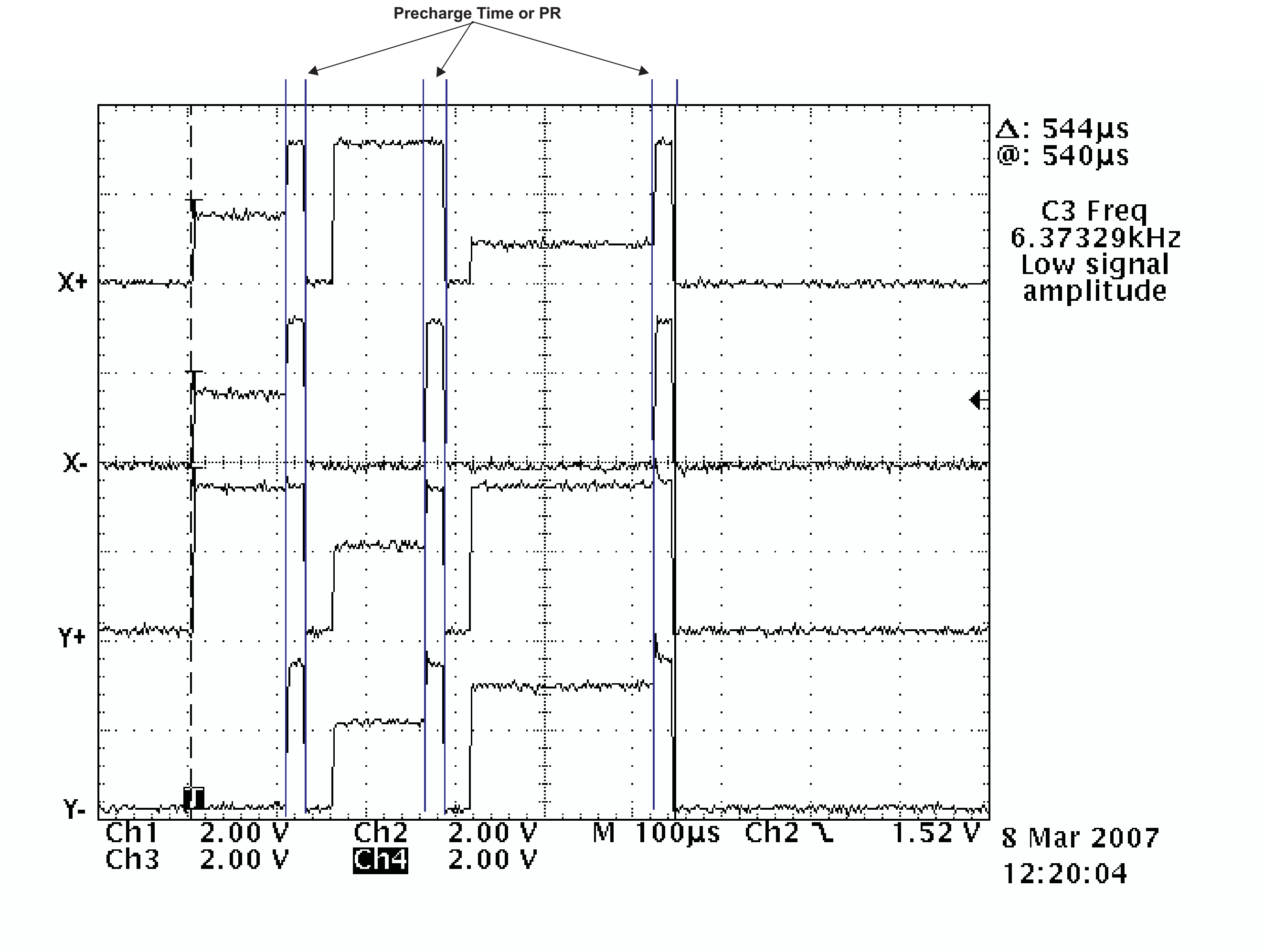

Figure 6. Precharge Time on TSC Analog Interface Lines

The sense time (SN2~SN0) sets the amount of delay for the TSC device to wait between two coordinates during TSC ADC conversions, as shown by Figure 7.

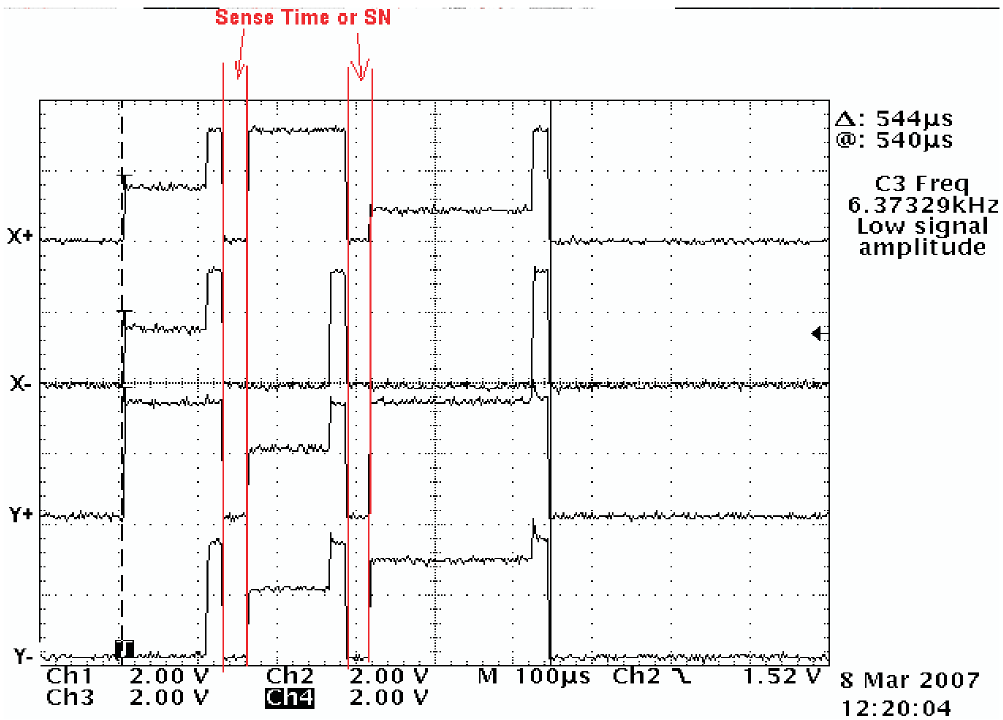

Figure 7. Sense Time on TSC Analog Interface Lines

If a pressure remains on the touch panel, the TSC devices may automatically and continuously acquire touch data; as many as several thousands SSPS of touch data can be driven-ON, sampled, converted, and processed. For a real-world application, however, users usually need only 100 ~ 500 SSPS touch data due to a human's controlling/responding limit. To save power, users often do not want the system to acquire any unnecessary data.

A touch screen controller's SSPS can be reduced in several ways:

- Use the batch delay to add waiting time between the sets of touch data
- Insert delays, such as PR and SN (but not PVS), to slow down the coordinate samples within a set because PR and SN do not consume power.

See Table 1 for their bit locations and for the selectable time ranges.

6 Conclusion

This application report discusses the programmable timings and functions in TI TSC2004, TSC2005, or TSC2006 touch screen controller device. These timings includes the ADC clock frequency (CL1~CL0), the touch panel voltage stabilization time (PV2~PV0), the TSC input pins' precharge time (PR2~PR0), and the sense time between coordinate samples (SN2~SN0).

All timing settings affect the analog interface traffic speed and interval. In addition, the ADC clock frequency (CL) and the touch panel voltage stabilization time (PVS) affect analog interface power consumption.

7 References

1. *Operation Schemes of Touch Screen Controllers* application report (SLAA359)
2. UNPUBLISHED*TSC2004, 1.2V to 3.6V, 12-Bit, Nanopower, 4-wire Touch Screen Controller With I2C™ Interface* data sheet (SBAS408)
3. *TSC2005, 1.6V to 3.6V, 12-Bit, Nanopower, 4-wire Touch Screen Controller With SPI™ Interface* data sheet (SBAS379)