Application Report
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Upgrading From ADS7806/07 To ADS8506/07 Devices

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ABSTRACT

The information in this application report is for current applications using the Texas Instruments ADS7806/07 devices in a surface-mount SO-28 (DW) package. This document helps users with ADS78xx devices through potential compatibility issues when upgrading to the new ADS85xx part series.

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1 Package and Pin Compatibility

The ADS8506/07 devices are designed to be fully pin-compatible with the surface mount SO-28 (DW package) version of the ADS7806/07 devices. The updated chip features the same 40-KSPS throughput and the same analog input ranges, with slightly lower power dissipation.

This table is hyperlinked to provide easy access to the associated ADS7806/07 and ADS8506/07 device data sheets. As new family products are added, this table will be expanded to include the new parts.

Current ADS78xx Family	New ADS85xx Family
ADS7806 – SBAS021	ADS8506 – SLAS484
ADS7807 – SBAS022	ADS8507 – SLAS381

2 Electrical Compatibility

This section describes potential electrical compatibility issues.

QSPI is a trademark of Motorola, Inc.

2.1 Absolute MAX Voltage Input Changes

The new ADS85xx devices differ in the maximum working supply voltage as Table 1 shows.

Table 1. Maximum Working Supply Voltage Differences

ADS78xx MAX Voltage Specification	
V_{ANA}	7 V
V_{DIG}	7 V
ADS85xx MAX Voltage Specification	
V_{ANA}	6 V
V_{DIG}	6 V

2.2 Input Impedance and Capacitance Changes

The new ADS85xx devices have the same typical input impedance based on the input range, but have different input capacitance features. The major differences are noted in Table 2.

Table 2. Different Input Capacitance Features

PARAMETER	CONDITIONS	78xx SERIES			85xx SERIES			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
ADSxx06/07								
Capacitance			35			45		pF
Impedance	±10-V Range		45.7			45.7		kΩ
	0V to 5V Range		20.0			20.0		kΩ
	0V to 4V Range		21.4			21.4		kΩ

2.3 Performance Compatibility

The new ADS8506/07 devices have performance characteristics that meet or exceed the specifications listed in the ADS7806/07 device data sheets. Primary interest regarding specific improvements depends on the actual application, but in general, all AC and DC specifications remain the same.

3 Functional and Timing Differences

These sections discuss the functionality and timing differences between the ADS7806/07 and the ADS8506/07 devices.

3.1 Functional Compatibility

The ADS8506/07 devices retain the same basic functionality of the ADS7806/07. There are no differences in the start of a conversion cycle, reading conversion data (either serially or through the parallel interface), or daisy-chain (TAG) operation.

The ADS8506/07 devices do not have the same QSPI™ interface as described in the ADS7806/07 Applications Information sections of the SBAS021 and SBAS022 data sheets. The ADS8506/07 do not offer the same tri-state capability to output serial data on the D7 pin.

3.2 Timing Compatibility

Timing changes related to the ADS8506/07 devices are discussed in detail throughout the next section. Depending on the specific application, these timing changes may affect the drop in replacement or ease of use in designs or end systems currently using the ADS7806/07. A careful review of Table 3 through Table 8, highlights the timing differences between the ADS7806/07 and ADS8506/07 devices.

3.3 Comparison of the ADS7806/07 and ADS8506/07 Parallel Timing Characteristics

Table 3 provides a side-by-side comparison of the parallel timing differences between the ADS7806 and the ADS8506. The **bold text** items show the timing differences which are most likely to have an impact on current ADS78/8506 designs.

Table 3. ADS78/8506 Parallel Timing Differences

SYMBOL	DESCRIPTION	ADS7806			ADS8506			UNIT
ADS7806 / ADS8507		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Convert Pulse Width	0.04		12	0.04		12	µs
t2	**Data Valid Delay after R/C LOW**		**14.7**	**20**		**13.5**	**15**	µs
t3	BUSY Delay from Start of Conversion			85			85	ns
t4	**BUSY LOW**		**14.7**	**20**		**13.5**	**15**	µs
t5	BUSY Delay after End of Conversion		90			90		ns
t6	Aperture Delay		40			40		ns
t7	**Conversion Time**		**14.7**	**20**		**13.5**	**15**	µs
t8	**Acquisition Time**			**5**		**11.5**		µs
t9	Bus Relinquish Time	10		83	10		83	ns
t10	BUSY Delay after Data Valid	20	60		20	60		ns
t11	**Previous Data Valid after Start of Conversion**	**12**	**14.7**			**13.5**	**15**	µs
t12	Bus Access Time and BYTE Delay			83		10	83	ns
t21	R/C to CS Setup Time	10			10			ns
t7 + t8	Throughput Time			25			25	µs

Table 4 provides a side-by-side comparison of the parallel timing differences between the ADS7807 and the ADS8507. The **bold text** items show the timing differences which are most likely to have an impact on current ADS78/8507 designs.

Table 4. ADS78/8507 Parallel Timing Differences

SYMBOL	DESCRIPTION	ADS7807			ADS8507			UNIT
ADS7806 / ADS8507		MIN	TYP	MAX	MIN	TYP	MAX	
t1	Convert Pulse Width	0.04		12	0.04		12	µs
t2	**Data Valid Delay after R/C LOW**		**19**	**20**		**18**	**20**	µs
t3	BUSY Delay from Start of Conversion			85			85	ns
t4	BUSY LOW		19	20		19	20	µs
t5	BUSY Delay after End of Conversion		90			90		ns
t6	Aperture Delay		40			40		ns
t7	Conversion Time		19	20	19	20		µs
t8	Acquisition Time			5		5		µs
t9	Bus Relinquish Time	10		83	10		83	ns
t10	BUSY Delay after Data Valid	20	60		20	60		ns
t11	**Previous Data Valid after Start of Conversion**	**12**	**19**		**12**	**18**		µs
t12	Bus Access Time and BYTE Delay			83			83	ns
t21	R/C to CS Setup Time	10			10			ns
t7 + t8	Throughput Time			25			25	µs

3.4 Comparison of ADS7806/07 and ADS8506/07 Internal Data Clock Serial Timing Characteristics

Table 5 provides a side-by-side comparison of the serial timing differences between the ADS7806 and the ADS8507, when using the internal conversion clock (read previous data during conversion). The **bold text** items show the timing differences which are most likely to have an impact on current ADS7806 serial interface designs when using the internal data clock and TAG tied low.

Table 5. ADS78/8506 Serial Timing Differences When Using Internal Conversion Clock

SYMBOL	DESCRIPTION	ADS7806			ADS8506			UNIT
ADS7806 / ADS8506		MIN	TYP	MAX	MIN	TYP	MAX	
t1 / t_{w1}	Convert Pulse Width	0.04		12	0.04		12	µs
t4 / t_{w2}	**BUSY Low**		**14.7**	**20**		**13.5**	**15**	µs
t7 / t_{conv}	**Conversion Time**		**14.7**	**20**		**13.5**	**15**	µs
t8 / t_{acq}	**Acquisition Time**			**5**	**10**	**11.5**		µs
t13 / t_{d4}	**Start of Conversion to DATACLK Delay**		**1.4**			**0.204**		µs
t14 / t_{c1}	**DATACLK Period**		**1.1**		**0.6**	**0.82**	**0.85**	µs
t15 / t_{d5}	**Data Valid to DATACLK HIGH Delay**	**20**	**75**		**150**	**204**		ns
t16 / t_{d6}	**Data Valid to DATACLK LOW Delay**	**400**	**600**		**150**	**208**		ns
t7 + t8 t_{conv} + t_{acq}	Throughput Time			25			25	µs

Table 6 provides a side-by-side comparison of the serial timing differences between the ADS7807 and the ADS8507, when using the internal conversion clock (read previous data during conversion). The **bold text** items show the timing differences which are most likely to have an impact on current ADS7807 serial interface designs when using the internal data clock and TAG tied low.

Table 6. ADS78/8507 Serial Timing Differences When Using Internal Conversion Clock

SYMBOL	DESCRIPTION	ADS7807			ADS8507			UNIT
ADS7807 / ADS8507		MIN	TYP	MAX	MIN	TYP	MAX	
t1 / t_{w1}	Convert Pulse Width	0.04		12	0.04		12	µs
t4 / t_{w2}	**BUSY Low**		**19**	**20**		**18**	**20**	µs
t7 / t_{conv}	**Conversion Time**		**19**	**20**		**18**	**20**	µs
t8 / t_{acq}	**Acquisition Time**			**5**	**5**	**7**		µs
t13 / t_{d4}	**Start of Conversion to DATACLK Delay**		**1.4**			**0.270**		µs
t14 / t_{c1}	**DATACLK Period**		**1.1**		**0.6**	**0.82**	**0.85**	µs
t15 / t_{d5}	**Data Valid to DATACLK HIGH Delay**	**20**	**75**		**15**	**35**		ns
t16 / t_{d6}	**Data Valid to DATACLK LOW Delay**	**400**	**600**		**20**	**35**		ns
t7 + t8 t_{conv}+ t_{acq}	Throughput Time			25			25	µs

3.5 Comparison of ADS7806/07 and ADS8506/07 External Data Clock Serial Timing Characteristics

These sections show the various timing relationships among the ADS7806/07 and ADS8506/07 devices with the application of an external serial I/O clock.

3.5.1 Read Previous Data During Conversion

Table 7 provides a side-by-side comparison of the serial timing differences between the ADS7806/07 and the ADS8506/07 when using an external clock to read previous data *during* a conversion cycle. The **bold text** items show the timing differences which are most likely to have an impact on current ADS7806/07 designs.

Table 7. Serial Timing Differences When Using External Clock to Read Previous Data During Conversion Cycle

SYMBOL	DESCRIPTION	ADS7806/07			ADS8506/07			UNIT
ADS7806/07 / ADS8506/07		MIN	TYP	MAX	MIN	TYP	MAX	
t1 / t_{w1}	Convert Pulse Width	0.04		12	0.04		12	µs
t3 / t_{d1}	**BUSY Delay from Start of Conversion**			**85**		12	**20**	ns
t17 / t_{c2}	**External DATACLK Period**	**100**			**35**			ns
t18 / t_{w3}	**External DATACLK High**	**40**			**15**			ns
t19 / t_{w4}	**External DATACLK Low**	**50**			**15**			ns
t20 / t_{su1}	**$\overline{CS}$ and R/C to External DATACLK Setup**	**25**			**15**			ns
t21 / t_{su2}	R/C to $\overline{CS}$ Setup Time	10			10			ns
t22 / t_{d8}	**Valid Data after DATACLK HIGH**	**25**			**2**		**20**	ns

3.5.2 Read Data After Conversion

Table 8 provides a side-by-side comparison of the serial timing differences between the ADS7806/07 and the ADS8506/07 devices when using an external clock to read data *following* a conversion cycle. The **bold text** items show the timing differences which are most likely to have an impact on current ADS7806/07 serial interface designs when using the external clock.

Table 8. Serial Timing Differences When Using External Clock to Read Data Following Conversion Cycle

SYMBOL	DESCRIPTION	ADS7806/07			ADS8506/07			UNIT
ADS7806/07 / ADS8506/07		MIN	TYP	MAX	MIN	TYP	MAX	
t1 / t_{w1}	Convert Pulse Width	0.04		12	0.04		12	µs
t3 / t_{d1}	**BUSY Delay from Start of Conversion**			**85**		12	**20**	ns
t17 / t_{c2}	**External DATACLK Period**	**100**			**35**			ns
t18 / t_{w3}	**External DATACLK High**	**40**			**15**			ns
t19 / t_{w4}	**External DATACLK Low**	**50**			**15**			ns
t20 / t_{su1}	**$\overline{CS}$ and R/C to External DATACLK Setup**	**25**			**15**			ns
t21 / t_{su3}	R/C to $\overline{CS}$ Setup Time	10			10			ns
t22 / t_{d8}	**Valid Data after DATACLK HIGH**	**25**			**2**		**20**	ns

4 Potential Application Issues

4.1 Parallel Mode Operation

The new ADS8506/07 devices, operating in the parallel mode, should not have any major impact on the current ADS7806/07 designs. The timing parameters and operating modes are nearly identical. If issues are identified, they will discussed in publication updates.

4.2 Serial Modes of Operation

When operating the new ADS8506/07 device in the internal DATACLK operating mode, a user may notice that an impact on reading serial data on either the rising clock or the falling clock edges. In the ADS7806/07 device, the internal data clock was framed by the output data in order to provide significantly longer hold times to the falling DATACLK edge. In the ADS8506/07 devices, the setup and hold times of the output data are essentially equalized to 35 ns typical. If issues are identified, they will discussed in updates of this publication.

As mentioned in the Functional Compatibility (Section 3.1), the ADS8506 and ADS8507 devices do not provide the same tri-state capability to offer serial data output on D7 (pin 9). Applications that require tri-stable SDO need to modify the circuitry to include an external buffer such as a SN74 series single bus buffer gate. Members of the 1G125 single gate bus buffer family offer an $\overline{OE}$ input pin which, when used in conjunction with the ADS8506/07 $\overline{CS}$ input, provides tri-state capabilities on a shared serial data bus.

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