Application Report
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MSP430™ 32-kHz Crystal Oscillators

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ABSTRACT

Selection of the right crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for ultra-low-power operation of an MSP430™ MCU. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

For additional information about the factors that influence the accuracy of the low-frequency oscillator, see MSP430™ LFXT1 Oscillator Accuracy.

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1 The 32-kHz Crystal Oscillator

1.1 The Crystal

For an ultra-low-power design, only low-frequency crystals are usable, because with higher-frequency oscillators, the current consumption increases significantly. Tuning-fork crystals typically have a frequency range of 10 kHz to 200 kHz in fundamental mode and a maximum drive level of 1 µW. These parameters make them the first choice for the 32768-Hz ultra-low-power crystal oscillator in MSP430 microcontrollers.

Every MSP430 MCU has a built-in crystal oscillator that can be operated with a tuning-fork crystal at 32768 Hz (often called 32 kHz). The mechanical oscillation (see Figure 1) of a 32-kHz tuning fork crystal is converted into an electrical signal. The equivalent electrical circuit of a crystal (see Figure 2) gives these electrical characteristics:

- C_M motional capacitance
- L_M motional inductance
- R_M mechanical losses during oscillation
- C_0 parasitic capacitance of package and pins

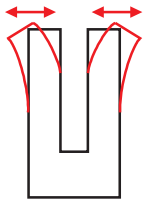


Figure 1. Mechanical Oscillation of a Tuning-Fork Crystal

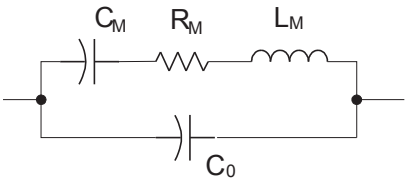


Figure 2. Equivalent Circuit of a Crystal

The series-resonance circuit consisting of C_M, L_M, and R_M represents the electrical equivalent of the mechanical resonance of the tuning fork. The frequency characteristics of a crystal's reactance are shown in Figure 3 and give two special frequencies:

- F_S (series resonance frequency) solely depends on C_M and L_M and gives a very stable frequency value.

$$F_S = \frac{1}{2\pi\sqrt{L_M C_M}}$$

- F_A (anti-resonance or parallel-resonance frequency), in addition, also depends on C_0, the parasitic capacitance of package and pins, which is not as precise as the other parameters, C_M and L_M. Hence, F_A gives a less well-defined frequency than F_S.

$$F_A = \frac{1}{2\pi\sqrt{L_M C_M}} \sqrt{1 + \frac{C_M}{C_0}}$$

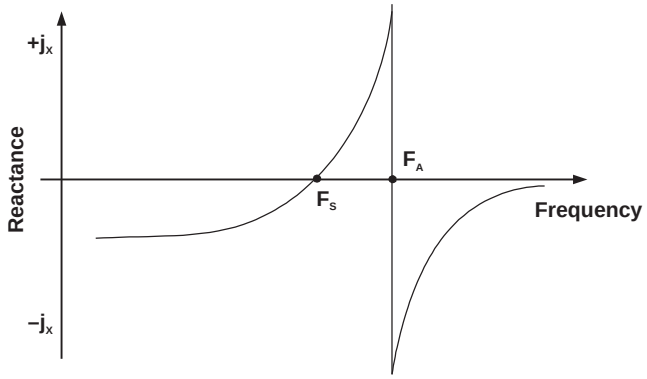


Figure 3. Reactance of a Crystal

The equivalent series resistance (ESR) can be calculated with the formula in Equation 1 from the equivalent circuit in Figure 2:

$$ESR = R_M \left(1 + \frac{C_0}{C_L}\right)^2 \quad (1)$$

C_0 is shown in Figure 2 and given by the crystal's data sheet, as is R_M or ESR. C_L is the required load capacitance of a crystal and is also given by the crystal's data sheet.

1.2 The Oscillator

The principle circuit of an oscillator is shown in Figure 4. Two basic parameters must be fulfilled to enable oscillation:

- Closed loop gain ≥ 1 for oscillator start up and closed loop gain = 1 for stable oscillation
- Closed loop phase shift = n × 360°

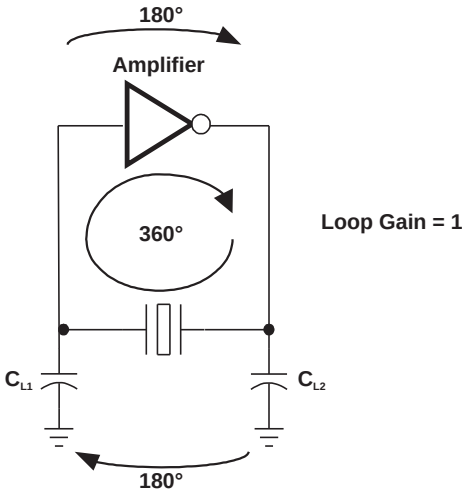


Figure 4. Principle Pierce Oscillator Circuit

Figure 4 shows the Pierce oscillator circuit, which takes advantage of the crystal's serial resonance frequency. The inverting amplifier gives a phase shift of approximately 180°. The feedback circuit consisting of a 32-kHz crystal and two load capacitors adds another 180° phase shift. This results in the required oscillator closed-loop phase shift of 360°. The closed-loop gain must be adjusted with the gain of the inverting amplifier. All MSP430 32-kHz crystal oscillators are Pierce oscillators.

2 Crystal Selection

The most important parameters when choosing a crystal are:

- Crystal's required effective load capacitance (for 32-kHz crystals, typically 6 pF to 15 pF)
- Crystal's ESR (for 32-kHz crystals, typically 30 kΩ to 100 kΩ)
- Tolerance (typically 5 ppm to 30 ppm)

All of these crystal parameters are given by the crystal data sheet but can be also measured at the real crystal using, for example, crystal impedance bridge, a vector voltmeter, or a network analyzer. It is very important to know these parameters, because otherwise it is not possible to design a stable oscillator.

2.1 Effective Load Capacitance

The Pierce oscillator (see Figure 4) uses two load capacitors, C_{L1} and C_{L2}, as load for the crystal. These capacitors generate, together with the crystal's inductance (L_M) (see Figure 2), the required 180° phase shift of the feedback loop. From the view of the crystal, these capacitors are a serial connection through GND. Hence, if using two equal capacitors, the values of these capacitors must be twice the required load capacitance. It is also important to consider all parasitic capacitances, such as PCB traces and MSP430 MCU pin capacitance, for the calculation of the necessary capacitors according to Equation 2.

$$C_{Load} = \frac{C'_{L1} \times C'_{L2}}{C'_{L1} + C'_{L2}} \quad (2)$$

Where:

$C'_{L1} = C_{L1} + C_{L1Parasitic}$

$C'_{L2} = C_{L2} + C_{L2Parasitic}$

When using equal capacitors for C_{L1} and C_{L2} and a symmetric layout with equal parasitic capacitance on both crystal pins, the effective load capacitance is shown in Equation 3.

$$C_{Load} = \frac{C_{L1} + C_{Parasitic}}{2} \quad (3)$$

Example:

Crystal requires 12 pF load.
Parasitic capacitance per pin is 2 pF.
$C_{L1} = (2 \times C_{Load}) - C_{Parasitic} = (2 \times 12\ pF) - 2\ pF = 22\ pF$
$C_{L2} = C_{L1} = 22\ pF$

One result of choosing the wrong load capacitors, which can be easily measured, is an incorrect oscillation frequency. Figure 5 shows a typical curve of frequency vs load capacitance.

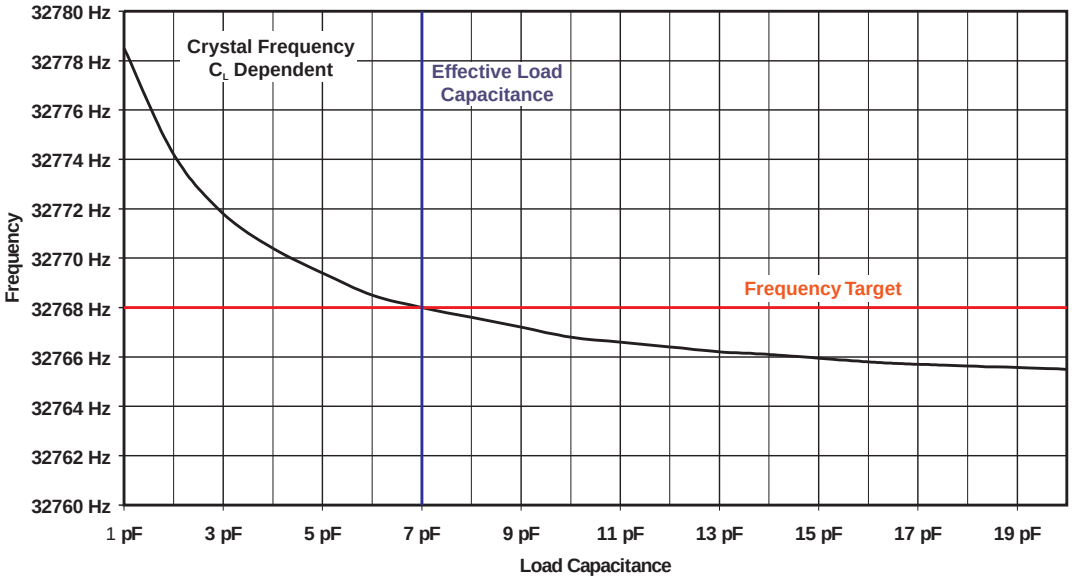


Figure 5. Frequency vs Load Capacitance for a 0-ppm Crystal

All MSP430 MCU 32-kHz oscillators have built-in load capacitors, C_{L1} and C_{L2}. In some MSP430 MCU versions, these load capacitors are fixed; in other MSP430 MCU versions, the internal load capacitor values can be programmed or external capacitors can be used. For details, see the data sheets and MSP430 MCU family user's guides. The various MSP430 MCU families have the following load capacitor configuration:

- MSP430x1xx: 6 pF (fixed effective capacitance with 12 pF per pin), external capacitors are not recommended
- MSP430F2xx: 0 pF to 12.5 pF (programmable effective capacitance), external capacitors are possible
- MSP430F4xx: 0 pF to 10 pF (programmable effective capacitance), external capacitors are possible

2.2 ESR Value

The ESR value is an electrical representation of losses of the mechanical crystal oscillation. A larger crystal loses less energy during oscillation, and this results in a lower ESR value. Small crystals, especially SMD crystals, tend to have higher ESR. A higher ESR value reflects the higher losses of a crystal.

The oscillator becomes unstable and stops oscillation if the ESR becomes too high. Hence, each oscillator has maximum limits of the ESR value. The lower the ESR than the recommended maximum value, the better the oscillator start up and stability.

A common test for oscillator stability is the negative resistance method (see Section 4.2). For this test, ESR must be increased with an external resistor. The maximum value of this increased ESR is called the oscillation allowance (OA). With this OA value, it is possible to make a judgment of the oscillator safety factor (SF) margin. It is good practice to do the negative resistance test, to avoid oscillator problems in high-volume applications.

Table 1 lists typical OA values for the 32-kHz oscillators of various MSP430 MCU families.

NOTE: If oscillation allowance for LF crystals (OALF) values are specified in an MSP430 MCU data sheet, this table does not apply, and only the data sheet values are valid.

Table 1. Typical Oscillation Allowance Values for the 32-kHz Oscillator

	MSP430x1xx	MSP430x2xx		MSP430x4xx	
	C_L = 6 pF	C_L = 6 pF	C_L = 12.5 pF	C_L = 6 pF	C_L = 12.5 pF
V_{CC} = 3 V	185 kΩ	500 kΩ	200 kΩ	460 kΩ	180 kΩ
V_{CC} = 2.2 V	88 kΩ	500 kΩ	200 kΩ	440 kΩ	170 kΩ

Refer to crystal manufacturer recommendation for 32-kHz crystals operating with MSP430 MCU oscillators.

2.3 Tolerance

The ppm tolerance value given in the data sheet expresses the possible frequency deviation of the resulting oscillator frequency, assuming that all other frequency-affecting parameters, such as effective capacitive load and temperature are at recommended values.

The amount of the frequency variation due to temperature depends very much on the crystal cut and the crystal shape. In comparison to some other crystal cuts, 32-kHz tuning-fork crystals exhibit a relative high frequency drift over temperature. Figure 6 shows the typical frequency deviation of a 0-ppm tuning-fork crystal over temperature. The ±ppm tolerance value, given in the crystal data sheet, shifts the graph of the tuning-fork crystal up and down.

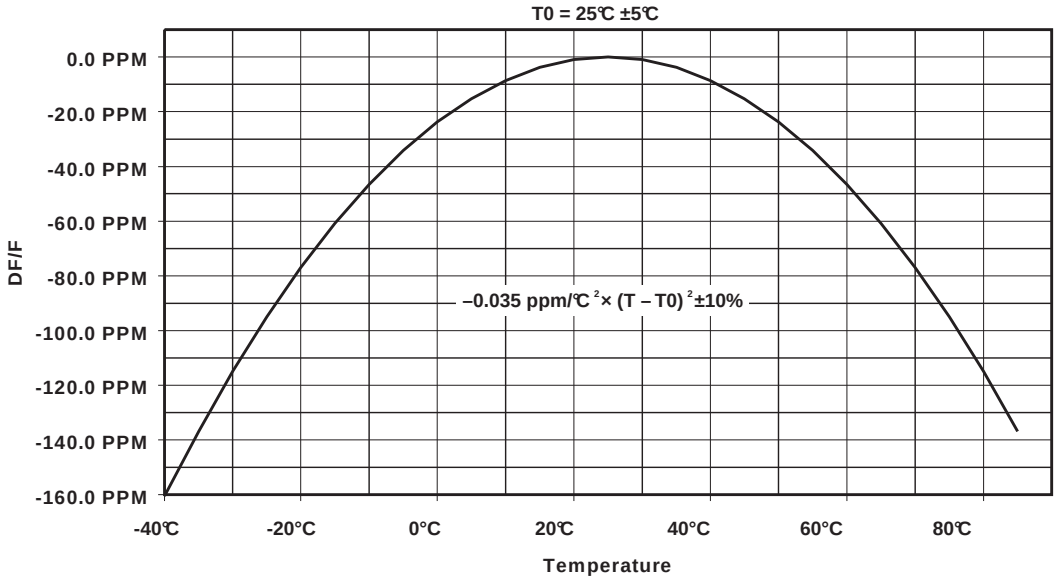


Figure 6. Frequency Deviation of a Tuning-Fork Crystal Over Temperature

If the 32-kHz crystal oscillator frequency is used for precision measurements over a wide temperature range, software can improve the measurement results by correcting the measured values according to a curve like Figure 6. In this case, obtain the real curve for the crystal from the crystal manufacturer.

Section 4.1 explains a test for oscillator frequency and a method to adjust the oscillator frequency.

2.4 Start-up Time

When initially energized, the only signal in the circuit is noise. That component of noise whose frequency satisfies the phase condition for oscillation is propagated around the loop with increasing amplitude. The amplitude continues to increase until the amplifier gain is reduced either by nonlinearities of the active elements ("self-limiting Pierce", MSP430x1xx) or by some automatic level control ("controlled Pierce" with AGC circuitry, MSP430x2xx and MSP430x4xx).

Start-up times between several hundred milliseconds and a few seconds are normal values for low-frequency tuning-fork crystals, like 32768-Hz crystals. The start-up time of a crystal oscillator depends on various factors:

- The oscillator frequency influences the start-up time. A 32-kHz crystal oscillator starts relatively slowly, compared to a crystal oscillator with a high frequency, e.g., above 1 MHz.
- High Q-factor crystal oscillators typically start slower than crystal oscillators with higher frequency tolerance.
- Crystal with low load capacitance typically start faster than crystals requiring high load capacitance.
- Crystals with low ESR start more quickly than high ESR crystals.
- Oscillators with high OA (Oscillation Allowance) start faster than low OA crystal oscillators.

3 PCB Design Considerations

The MSP430 MCU LFXT1 32-kHz crystal oscillator is designed for ultra-low-power consumption. According to the data sheets, most MSP430 MCU derivatives consume less than 1 µA when the 32-kHz oscillator, the clock signal (ACLK), and a timer are running. Hence, the current flowing between the MSP430 MCU pins, the crystal and, if used, the external capacitors is extremely low. Long signal lines make the oscillator very sensitive to EMC, ESD, and crosstalk. Even the best components cannot solve problems caused by a poor layout.

The crystal oscillator is an analog circuit and must be designed according to analog-board layout rules:

- Signal traces between the MSP430 MCU pins, the crystal and, if used, the external capacitors must be as short as possible. This minimizes parasitic capacitance and sensitivity to crosstalk and EMI. The capacitance of the signal traces must be considered when dimensioning the load capacitors.
- Keep other digital signal lines, especially clock lines and frequently switching signal lines, as far away from the crystal connections as possible. Crosstalk from digital signals may disturb the small-amplitude sine-shaped oscillator signal.
- Reduce the parasitic capacitance between XIN and XOUT signals by routing them as far apart as possible.
- The main oscillation loop current is flowing between the crystal and the load capacitors. Keep this signal path (crystal to C_{L1} to C_{L2} to crystal) as short as possible and use a symmetric layout. Hence, both capacitors' ground connections should always be as close together as possible. Never route the ground connection between the capacitors or all around the crystal, because this long ground trace is sensitive to crosstalk and EMI.
- Guard the crystal traces with ground traces (guard ring). This ground guard ring must be clean ground. This means that no current from and to other devices should be flowing through the guard ring. Connect this guard ring to AV_{SS} of the MSP430 MCU with a short trace. Never connect the ground guard ring to any other ground signal on the board. Also avoid implementing ground loops.
- With 2-layer boards, do not route any digital-signal lines on the opposite side of the PCB under the crystal area. In any case, it is good design practice to fill the opposite side of the PCB with clean ground and also connect this ground to AV_{SS} of the MSP430 MCU.
- Connect the crystal housing to ground.

  Before soldering the crystal housing, contact the crystal manufacturer to make sure not to damage the crystal. Overheating the crystal housing could lead to destruction of the crystal.
- In LF mode, the LFXT1 oscillator of MSP430x1xx requires a ≥5.1-MΩ resistor from XOUT to V_{SS} when V_{CC} < 2.5 V. This is used to increase the drive level of the MSP430 MCU amplifier at low V_{CC}. Refer to the data sheet for details.

Making use of the MSP430 MCU built-in capacitors gives a simple layout, with only the crystal connected to the XIN and XOUT pins of the MSP430 MCU. The traces between the MSP430 MCU and the crystal should be as short as possible, and a ground area should be placed under the crystal oscillator area. When using external capacitors instead of the internal capacitors, the traces between the crystal and the capacitors and the trace between the two capacitors should be as short as possible. Examples for recommended layouts are shown in Figure 7. An additional ground guard ring could improve the performance.

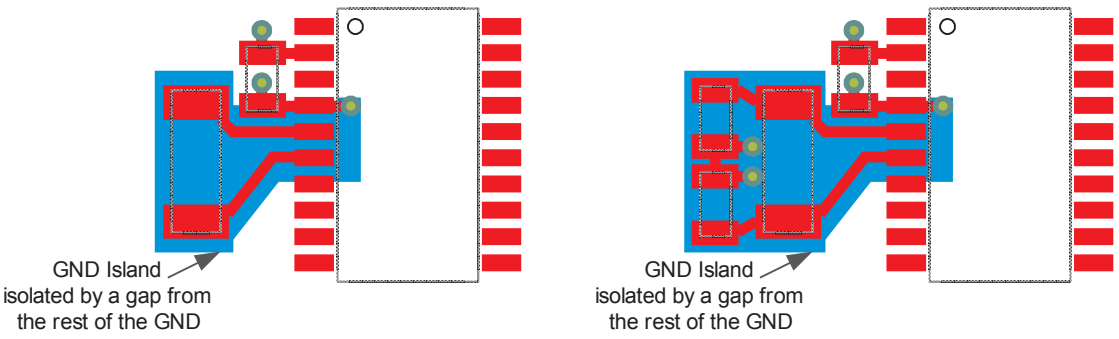
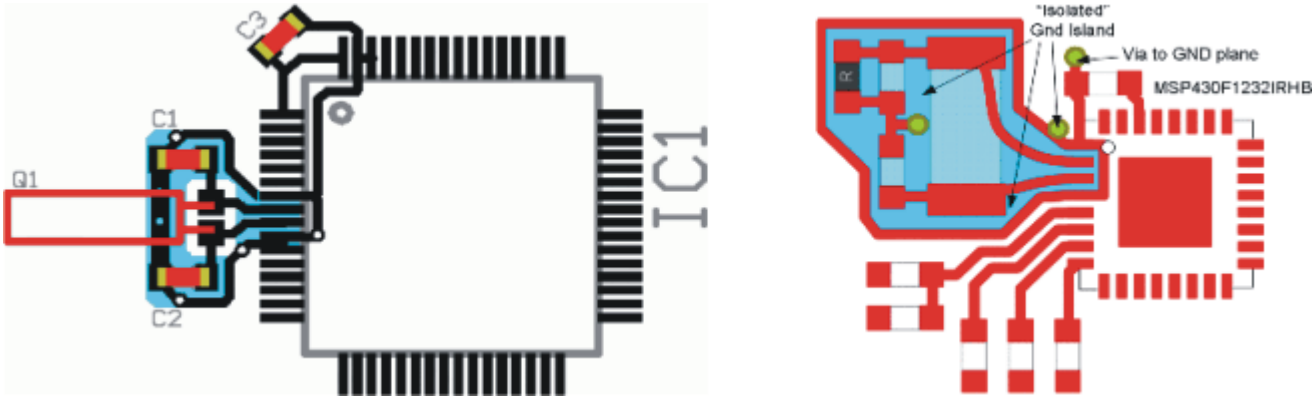


Figure 7. Layout Without and With External Load Capacitors (XIN and XOUT Neighboring Pins Are Standard Function Pins)

Some of the MSP430 MCU have NC (not connected) pins neighboring the XIN and XOUT crystal connection pins. In that case, it is recommended to make use of the situation and add a ground guard ring around the crystal signals. This ground guard ring should have a short connection to the MSP430 MCU V_{SS} pin. Layout examples for this scenario are shown in Figure 8. In all these examples, the section between crystal and the load capacitors is laid out symmetrically.



NOTE: The layout on the right side includes a resistor between XOUT and V_{SS}. The LFXT1 oscillator of MSP430x1xx (see data sheet) in LF-mode requires a resistor of ≥5.1 MΩ from XOUT to V_{SS} when V_{CC} < 2.5 V, to compensate for decreasing drive level with lower supply voltages.

Figure 8. Layout With External Capacitors and Ground Guard Ring (XIN and XOUT Neighboring Pins Are NC Pins) Examples for MSP430F41x and MSP430F1232IRHB

4 Testing the Crystal Oscillator

The following measurements help to verify the crystal oscillator stability:

- Oscillator frequency vs load capacitance
- Negative resistance method (Oscillation Allowance test)
  - Start allowance
  - Stop allowance

4.1 Oscillator Frequency vs Load Capacitance

As shown in Figure 5, the crystal oscillator frequency is very much dependent on the load capacitance that is connected. Hence, measuring the oscillator frequency gives a good indication if the load capacitors that are used match the crystal requirements. This measurement also automatically includes the parasitic PCB and pin capacitances of the application. The graph in Figure 5 shows typical 32-kHz crystal characteristics. The characteristics (pullability curve) of the crystal should be provided by the crystal manufacturer.

It is strongly recommended not to measure the oscillator frequency directly at the crystal pins. The capacitance at the crystal pins is in the range of 10 pF, and the impedance on this signal line is several megaohms. A typical passive probe has a capacitance in the range of 10 pF and an input impedance of approximately 10 MΩ. Both values are in the range of the oscillator characteristics and heavily influence the behavior of the crystal oscillators. The MSP430 MCU internal digital ACLK clock signal always carries the clock signal of the 32-kHz crystal oscillator. All MSP430 MCU have the capability to output ACLK at one of the I/O pins. Measuring at this digital ACLK output does not influence the crystal oscillator in any way. ACLK still gives all necessary information to determine the stability and performance of the setup.

A frequency counter with a resolution and accuracy of at least 0.1 ppm in the targeted frequency range should be used to measure the 32768-Hz clock signal. If, for example, the tolerance of the crystal is given with ±30 ppm, the 32768-Hz clock frequency should be ±0.9 Hz accurate at room temperature. For a ±5-ppm crystal, the frequency should be within ±0.16 Hz when the correct capacitive load is connected.

Assuming the crystal itself has no tolerance, too low a capacitive load results in a higher oscillator frequency than expected and, vice versa, the frequency is lower than the nominal value, if the load is too high. Hence, if the oscillation frequency is too high, the value of load capacitors must be increased. When a too low frequency is measured, it is necessary to decrease the value of the load capacitors. Comparing the finally optimized capacitors with the crystal data sheet value for load capacitance gives the parasitic capacitance added by the PCB layout and pins.

4.2 Negative Resistance Method

The negative resistance method is also called the Oscillation Allowance test or safety margin test. With this test, the ESR safety factor is measured. As already stated in previous sections, the ESR value in the equivalent circuit of a crystal (see Figure 2) represents the losses. These losses must be compensated by the amplifier in the MSP430 MCU. If the losses exceed the drive capabilities of the amplifier, the oscillation amplitude starts decreasing until it finally dies away, or the oscillator does not even start up. The ESR value of a crystal increases with temperature. Thus, the oscillator may be working fine at room temperature but may fail at higher temperatures. Also, higher humidity can increase the losses in the oscillator, due to lower parasitic resistive values. To avoid time-consuming oscillator tests over all possible environmental situations, the negative resistance test has been established. It gives a SF (Safety Factor) value that allows the designer to assess, relatively easily, the safety margin of a particular oscillator setup.

For the negative resistance test, an additional resistor is added in series with the crystal, as shown in Figure 9. The additional serial test resistance, R_Q, is increased until the oscillator does not start up or a running oscillation stops. It is good practice to lower the resistance until the oscillator works again, to determine the critical value. This can be done using an SMD potentiometer that is suitable for RF, to add as few parasitic values as possible. Because all parameters and the parasitic values of this potentiometer contribute to the resulting parameters of the oscillator circuit, the final value of R_{Qmax} should be verified with an SMD resistor.

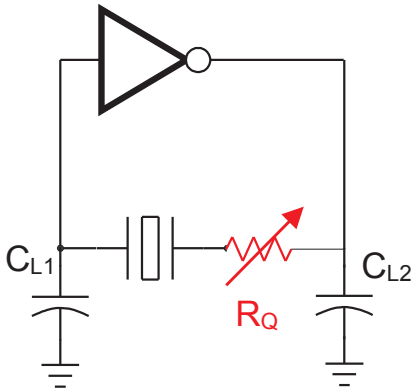


Figure 9. Negative Resistance Method With Added Resistor R_Q

The test can be done during the oscillator start (Start Allowance) and it can be repeated for a running oscillator to determine when oscillation dies away (Stop Allowance).

- Start Allowance: Resistor R_Q is placed in series to the crystal. The power is then turned on, and it is checked if the oscillator starts. For each new resistor value, the MSP430 MCU must be powered down and powered up again. The highest resistor value with which the oscillator still starts is the Start Allowance.
- Stop Allowance: When the oscillator is running, the R_Q potentiometer is increased until the oscillator stops. The potentiometer can then be reduced again until the oscillation starts again. The highest resistor value with which the oscillator still runs and does not stop is the Stop Allowance.

After the critical values of R_Q are measured, the OA and the SF should be calculated to allow a judgment of the oscillator stability, as shown in Equation 4 and Equation 5.

Oscillation Allowance (OA)

$$OA = R_{Qmax} + ESR \quad (4)$$

Safety Factor (SF)

$$SF = \frac{OA}{ESR} = \frac{R_{Qmax} + ESR}{ESR} \quad (5)$$

Table 2 gives a qualification of the SF and is based on the experience of major crystal manufacturers. If the outcome of the investigations is a sufficient SF, then the assumption can be made that all reasonable tolerances and variations of the parameters of the oscillator externals should be covered.

Table 2. Safety Factor

QUALIFICATION OF THE SAFETY FACTOR (SF)	QUALIFICATION
SF < 2	Unsafe
2 ≤ SF < 3	Suitable
3 ≤ SF < 5	Safe
SF ≥ 5	Very safe

4.3 Relationship Between Crystal ESR and Safety Factor

To further show the importance of ESR on a crystal's ability to oscillate properly, the negative resistance method detailed in Section 4.2 was used on a selection of crystal oscillators with varying packages, ESR values, and tolerances. The test was performed using a MSP430FE427A device populated on a MSP-TS430PM64 target board, a platform whose design does not follow the recommendations detailed by this application report. The R_{Qmax} value of each crystal was determined by placing a potentiometer in series followed by testing for the crystal's start and stop allowances. The nearest standard resistor value (±5%) was recorded as general reference. The exact oscillation allowances and safety factors were also

calculated using Equation 4 and Equation 5. Table 3 outlines the outcome of these tests. Note that results will differ based on variables such as PCB design, board cleanliness or amount of flux present, and quantity of solder used, all of which affect the system's parasitic capacitance. The size and dimensions of all crystals used in this example are similar, but accommodations were made to establish connections to the target board and the various package types.

Table 3. Safety Factor Test Results

Mouser Crystal Part Number	Package	ESR (kΩ)	Tolerance (±ppm)	R_{Qmax} (kΩ)	Standard Value (kΩ)	OA (kΩ)	SF[1]
AB26T-32.768KHZ	Radial	35	20	257	240	292	8.34
CFS206-32.768KEZB-U	Radial	35	10	254	240	289	8.26
AB26TRQ-32.768kHz-T	Radial	50	20	195	180	245	4.90
MC-306 32.7680K-A0	4-SOJ	35	20	233	220	268	7.66
ABS25-32.768KHZ-T	4-SOJ	50	20	250	240	300	6.00
CM200C-32.768KDZB-UT	4-SOJ	50	20	242	240	292	5.84
ABS25-32.768KHz-6-1-T	4-SOJ	50	10	238	220	288	5.76
FC-12M 32.7680KA-A3	2-SMD	90	20	178	160	268	2.98
ABS10-32.768KHZ-T	2-SMD	70	20	213	200	283	4.04
ABS07-32.768KHZ-1-T	2-SMD	70	10	197	180	267	3.81
FC-135R 32.7680KA	2-SMD	50	20	246	240	296	5.92

(1) While some tests resulted in safety factors in the suitable and safe categories, the target boards are not ideal test fixtures due to the socket.

As Table 3 shows, crystals with a lower ESR produce a higher R_{Qmax}, which proportionately results in higher oscillation allowances and safety factors.

5 Crystal Oscillator in Production

In general, it needs to be considered that the 32-kHz crystal oscillator is an ultra-low-power oscillator with very low current, in a range significantly below 1 µA. Thus it is critical, for the performance of the oscillator, that the PCB assembly process not introduce any materials or residue that would compromise the surface insulation resistance and lead to current leakage paths. One common source of residues and unwanted materials is the use of "no-clean" flux and the consequent lack of cleaning in the manufacturing process.

5.1 PCB Material, Quality, and Cleaning

In addition to other factors, which have been described in the previous sections and which are covered by circuit theory, optimization of the components, and layout, there is another group of factors significantly affecting the performance of the oscillator setup. These factors are the board-assembly production process and assembly quality. In the previous sections, the ultra-low-power character of the MSP430 MCU oscillators has been mentioned. Due to the optimization for the lowest possible current, the losses caused by parasitic currents can have a significant impact on the overall oscillator performance.

PCB quality and cleanliness are especially critical in applications with a long lifetime and under unfavorable conditions, like high humidity and fast temperature cycles that possibly cause humidity condensation on the printed circuit board. Requiring a high level of quality and cleanliness reduces process residuals, which can lead to a decrease of the insulation of the sensitive oscillator signal lines towards each other and neighboring signals on the PCB. High humidity can lead to moisture condensation on the surface of the PCB and, together with process residuals, reduce the surface resistivity of the board. Thus, TI strongly recommends to carefully select the materials for the soldering process and use clean PCB material for the assembly process and cleaning afterwards, if needed, especially when the previously described factors apply.

One specific target of cleaning is the removal of residuals associated with the flux used in soldering, which is discussed in Section 5.2.

5.2 Soldering and Contact Impedance

Soldering introduces flux materials that have the primary purpose of chemically removing oxides to ensure metallic surfaces are joined properly with minimal contact impedance. When soldering, there are basically two different types of flux material. There are water-soluble flux materials, which must be cleaned off after the soldering process by appropriate cleaning processes, and there are low-solid fluxes (LSF) or "no clean" flux materials on the market. For specific cleaning procedures, refer to the solder-paste manufacturer's recommendation for the specific soldering paste and flux. The main advantages of water-soluble fluxes are that they are typically the most highly active and more effective than "no-clean" products. Being more highly active, the water-soluble fluxes support a much better wetting process which leads to less soldering dwell time and consequently less thermal shock. The main disadvantage is the cost associated with the cleaning in the assembly process. The principle advantage of a "no-clean" product is lower cost, while the disadvantage revolves around post-soldering reliability.

Even when using the "no clean" products in ultra-low-power applications, PCB cleaning is recommended to achieve maximum performance by removing flux residuals from the board after assembly. The residuals left behind are typically weak organic acids and oils. The weak organic acids dissolve in water making them sources of leakage currents and failures in humid environments. Additionally the ester oil can act as an entrapment for dust which can also act as a humidity absorber. It is important to work with your manufacturer to identify sensitive or precision circuits that can be impacted by flux residuals and select a cleaning process to remove them. The flux residuals on the board can cause leakage current paths, especially in humid environments. In general, reduction of losses in the oscillator circuit leads to a better safety margin and, thus, also increases performance and reliability.

The MSP430 MCU package is qualified against JEDEC Std 020 to withstand the specified maximum peak reflow temperature allowed at certain moisture sensitivity level (MSL). This is the maximum allowed reflow profile. The solder-paste supplier usually supplies a suggested reflow profile that is within the JEDEC Std 020 maximum range. Thus, the JEDEC recommendations for the soldering profile for devices and the recommendations of the soldering materials supplier should be carefully followed, to achieve high reliability and quality solder joints.

If the MSP430 MCU package is to be exposed to any reflow temperatures after the liquid cleaning process, the board with the mounted MSP430 MCU package should be baked, to dry out the part before the following reflow process. In this case, the devices must be baked according to the JEDEC Std 020 (24 hours at 125°C) before processing through an additional solder-reflow step or performing a rework soldering.

Another important topic in the category of soldering is how to properly solder the metal housing or 'can' to the PCB. Without proper consideration of the manufacturer's guidelines, it is possible to damage the crystal from thermal stress. Adhering to specific guidelines can be hindered because of the large footprint that can remove heat from the area requiring higher temperatures or longer dwell times. Again, it is critical to adhere to the manufacturer's specification for soldering the crystal to prevent overheating and damaging the part.

5.3 Environmental Influences, Temperature, and Humidity

The most relevant environmental influences are temperature, humidity, and airborne contaminants. These environmental influences contribute to the general breakdown and introduction of electrochemical migration (ECM) on the PCB. These influences can also introduce leakage paths in the crystal oscillator circuit. And while the impact associated with ECM are generally seen after years of operation, the impact on the low power crystal-oscillator circuit can be immediately seen with the introduction of leakage paths. This impact may range from slow start up times to a complete inability to oscillate.

Temperature, specifically higher temperatures can have both positive effects and negative effects. A positive effect is that higher temperatures promote evaporation of weak organic acids found in flux residues and thus reduce leakage associated with the residue. A negative effect is that the higher temperature can reduce the drive strength of the output stage transistors thus, the safety margin of an oscillator setup decreases. As long as the safety factor test has shown good results, as classified in Table 2, and the crystal is being used in the standard industrial temperature range, the application should work safely.

In addition to high temperature, temperature cycles, especially fast temperature cycles combined with high ambient humidity, can result in condensed water on the PCB. Condensation and humidity in general contribute to the degradation of the PCB. And as already discussed, the humidity is drawn to the hygroscopic residue associated with no-clean flux, resulting in leakage paths and a higher ESR for the crystal.

Together with soldering residues and other board contaminations, dust (air-borne contaminants) can easily accumulate in applications with a lifetime of several years and non-air-proof housings. This debris can decrease the insulation of the oscillator signals towards each other and towards neighboring signals on the PCB. Thus, it is a good practice to introduce a protective coating of the crystal, the attached externals, and the MSP430 MCU oscillator pins. Examples of protective coatings are conformal coating, encapsulation, and potting.

Conformal coating is more popular, providing a transparent protective layer that allows visible inspection. Silicon coatings are typically superior to urethane and acrylic, but all three types can be used to preserve the parameters and performance of the oscillator over many years of operation in the field.

Potting and encapsulation materials offer similar benefits. Typically made of silicon or polyurethane, potting provides vibration dampening, heat dissipation, security (non-transparent), and mechanical protection. Working with the contract manufacturer will help avoid possible issues associated with potting materials coefficient of thermal expansion and the associated stress placed upon a surface mount crystal. High (>450V/mil) dielectric strength materials are recommended for coatings to ensure little or no performance difference is seen in the crystal-oscillator circuit. Table 4 lists examples of high-dielectric materials.

Table 4. Example Coating Materials

Manufacturer	Product	Dielectric Strength
Cramolin	Plastik	21 kV/mm (533 V/mil)
3M™	Novec™ 1901	3700 V/mil
MG Chemicals	419C	>1500 V for 1-mil coating per IPM-TM-650

If no coating is provided, then a continuous degradation of the oscillator performance can occur and should be taken into account. While a very effective defense against environmental influences, the use of protective coatings brings back into focus the importance of board cleanliness. Protective coatings introduce reliability risks which are associated with the contamination trapped under the coating into which moisture can diffuse.

5.4 Device-Specific Features to Support Better Start-up Behavior

Due to the influences to the start-up behavior of the MSP430 MCU ULP oscillator, described in the previous chapters, this section provides guidance to improve the overall start-up time of the low-frequency oscillator (LFO) by adding a simple piece of code.

The background for this kickstart feature lies in the architecture of the Pierce oscillator (see Figure 4). Normally the amplifier inverts the input signal coming from the crystal and amplifies the signal to further excite the tuning fork crystal to oscillate to its target frequency. Due to the ULP design and external environmental conditions like crystal ESR, load capacitance, shunt capacitance, humidity, PCB contamination, and temperature, the start-up behavior of the whole circuit might be different. This can lead to longer start-up times, which can conflict with the application requirements.

To work around this behavior, it is possible to create some kick-start noise on the amplifier output to help the crystal start oscillating more quickly. This is possible by simply changing the supply source of the amplifier by switching it between high-frequency mode and low-frequency mode multiple times. The created output noise significantly reduces the start-up time and does not require additional effort on PCB design or external components. However, the general requirements for LFO design described in Section 2.1, Section 2.2, Section 3, Section 5.1, Section 5.2, and Section 5.3, need to be considered and followed. The described methodology is not intended to revive a crystal that is failing to start at all.

The method that is introduced here is also called "XTS toggling", and it simply inverts the XTS bit inside a specific register of the clock module multiple times. Table 5 is an overview of the bit naming and the corresponding register for applicable MSP430 MCU families. In addition to using XTS toggling, TI recommends using the highest possible drive strength to further support a fast start-up of the crystal.

Table 5. MSP430 MCU Family Overview With Respect to XTS and Corresponding Registers

MSP430 MCU Family	Bit Name	Corresponding Register
F1xx family	XTS	BCSCTL1
F2xx and G2xx family(1)	XTS	BCSCTL1
F4xx family	XTS_FLL	FLL_CTL0
F5xx and F6xx family	XTS	UCSCTL6
FR5xx and FR6xx	No shared LF or HF oscillator available	
FR2xx and FR4xx	XTS	CSCTL6

(1) This does not include the MSP430x20xx and MSP430G2xx devices, which have no shared LF/HF oscillator.

The code snippet written in assembler shows the implementation in software (see Figure 10). This code toggles the XTS bit 400 times to create the described noise in the oscillator circuit to improve the start-up behavior. The number of toggles can be varied depending on the frequency, but it should be large enough to create enough noise to help the crystal to start. On the other side, this loop should not be too large that it is longer than the typical start-up time of a crystal oscillator, which is in the range of 1 to 4 seconds. This start-up help should applied to the crystal before the clock itself is used for any function; for example, as the reference clock for the FLL.

```
                mov     #400,R15
Toggle_XTS
                xor.b   #XTS_FLL,&FLL_CTL0
                dec     R15
                jnz     Toggle_XTS
                bic.b   #XTS_FLL,&FLL_CTL0
```

Figure 10. XTS Toggle Assembler Code for an F4xx Device

This methodology was applied on four MSP430FE427 sample devices, which are known as critical with respect to start-up time. Other devices falling into this category are:

- MSP430F449 and corresponding spins
- MSP430F437 and corresponding spins
- MSP430FE4252 and corresponding spins
- MSP430FE427A and corresponding spins
- MSP430FG4270 and corresponding spins
- MSP430FG439 and corresponding spins
- MSP430FW427 and corresponding spins
- MSP430FW429 and corresponding spins
- MSP430C413 and corresponding spins

All tests were performed using specific crystals with different ESR values to demonstrate the dependency to ESR and the impact of XTS toggling. In addition, different types of PCB were used:

1. The nonoptimized board was a lab PCB using socket and a connector to plug in the crystal (see Figure 11). This board added a lot of parasitic capacitance and inductance to the oscillator system.

Figure 11. Nonoptimized PCB for General Test Purpose

2. The optimized board had the MSP device soldered on the PCB and the crystal placed as close as possible to it following the layout guidelines described in this document (see Figure 12). This was done to reduce the negative effect of PCB influence due to bad LFO layout.

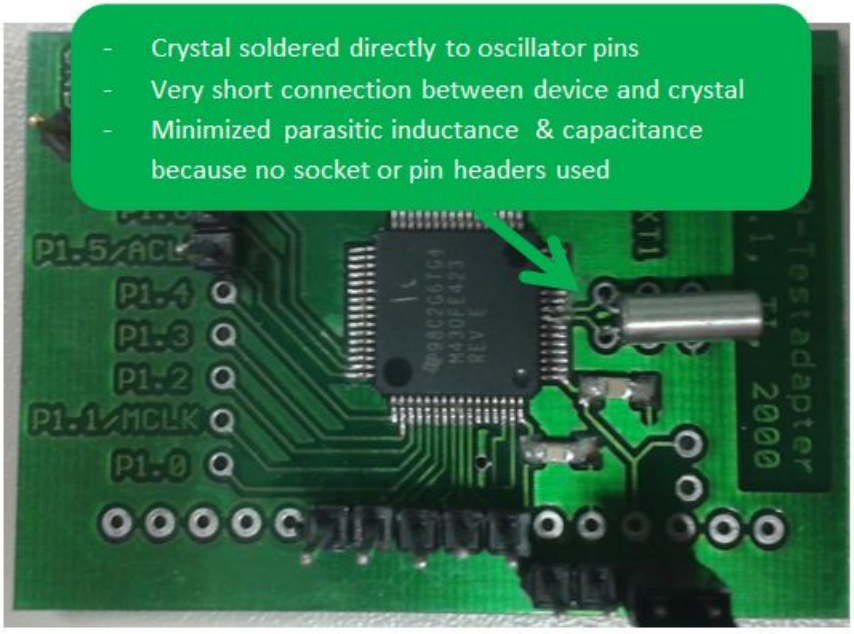


Figure 12. PCB Optimized for Low-Frequency Oscillator Measurements

The results in Table 6 clearly show the positive impact of the XTS toggle sequence to the start-up behavior of the LFO. While all four units had very long start-up times (above 16 s) on the nonoptimized PCB, the start-up time was reduced to approximately 2.3 s on average on an optimized PCB. This example shows that it very important to implement the oscillator fault flag loop before the crystal clock is used by the system to detect possible start-up issues on application level. In addition to the impact of XTS toggling, the results also show the significant impact of the PCB, which was designed according the guidelines in Section 3.

Table 6. Start-up Time Results Demonstrating the Effect of XTS Toggling Using 42-kΩ Crystal

Unit ID	Start-up Time With 42.4-kΩ Crystal (High ESR)			
	Nonoptimized PCB Without XTS Toggling	Nonoptimized PCB With XTS Toggling	Optimized PCB Without XTS Toggling (seconds)	Optimized PCB With XTS Toggling (seconds)
1	No start-up within 16 s	No start-up within 16 s	3.40	0.73
2	No start-up within 16 s	No start-up within 16 s	7.93	1.51
3	No start-up within 16 s	No start-up within 16 s	2.62	0.78
4	No start-up within 16 s	No start-up within 16 s	2.28	0.40

As a second experiment, the same measurements were taken using a different crystal with a much lower ESR. The results in Table 7 report the impact of XTS toggling using a low-ESR crystal to the LFO start-up time. The values can be brought down to approximately 1.9 s on average, which is an additional improvement of 0.4 s compared to the results using a 40-kΩ crystal. This clearly shows that the PCB, crystal, and XTS all contribute to a good and acceptable start-up

Table 7. Start-up Time Results Demonstrating the Effect of XTS Toggling Using 14-kΩ Crystal

Unit ID	Start-up Time With 13.7-kΩ Crystal (Low ESR)			
	Nonoptimized PCB Without XTS Toggling	Nonoptimized PCB With XTS Toggling	Optimized PCB Without XTS Toggling (seconds)	Optimized PCB With XTS Toggling (seconds)
1	2.95	0.63	1.59	0.23
2	4.16	0.83	2.13	0.34
3	2.82	0.75	1.17	0.24
4	2.71	0.54	1.34	0.21

In conclusion, the impact of the PCB, humidity, PCB contaminations, and parameters of the used crystal need to be considered when designing an LFO circuit with strict start-up requirements. If the start-up requirements cannot be achieved with the traditional firmware implementation, then the use of the XTS toggling sequence might be an extra option to improve the start-up behavior.

6 Hardware Troubleshoot for Crystal-Oscillator Start-up in Production

The purpose of this chapter is to provide a guideline for hardware troubleshooting when the 32-kHz crystal and MSP430 MCU LFXT oscillator do not work as expected in production. Specifically, when failures associated with slow starting or nonstarting crystal-oscillator circuits affect production yield.

Production start-up issues are divided into two categories. The first is simply crystal oscillators that will not start, and the second category is crystal oscillators that start slowly. This second category is a candidate for the XTS toggle method described in Section 5.4. The goal is to identify solutions that can improve the crystal-oscillator circuit. This improvement can be either a reduction in start-up time or changing the circuit from one that does not start to one that starts slowly. Before applying a solution, it is necessary to identify the issue that is preventing or delaying the start-up. To identify these issues, the following check points are recommended.

1. Check Firmware. While outside of the scope of this discussion, the firmware should follow best practices as found in the MSP430 MCU family user's guides and code examples.
2. Check the errata to determine if there are bugs related to LFXT and if the design violates the errata bugs.
    1. If errata number XOSC8 (ACLK failure when crystal ESR is below 40 kΩ) applies to the device (for instance, MSP430F4152), refer to *XOSC8 Guidance* for information regarding working with this erratum.
    2. If errata number XOSC7 (internal crystal load capacitance issue) applies to the device (for instance, MSP430F413), disable the internal crystal load capacitance.
3. Check board design if the Crystal + LFXT circuit design follows the recommendations in Section 3.
4. Check PCB cleanliness. If not clean, use an appropriate cleaning agent to clean it and test again.
5. Check the safety factor, following the guidelines in Section 4.2.

Figure 13 shows a flow chart for troubleshooting to identify possible causes and corrective actions.

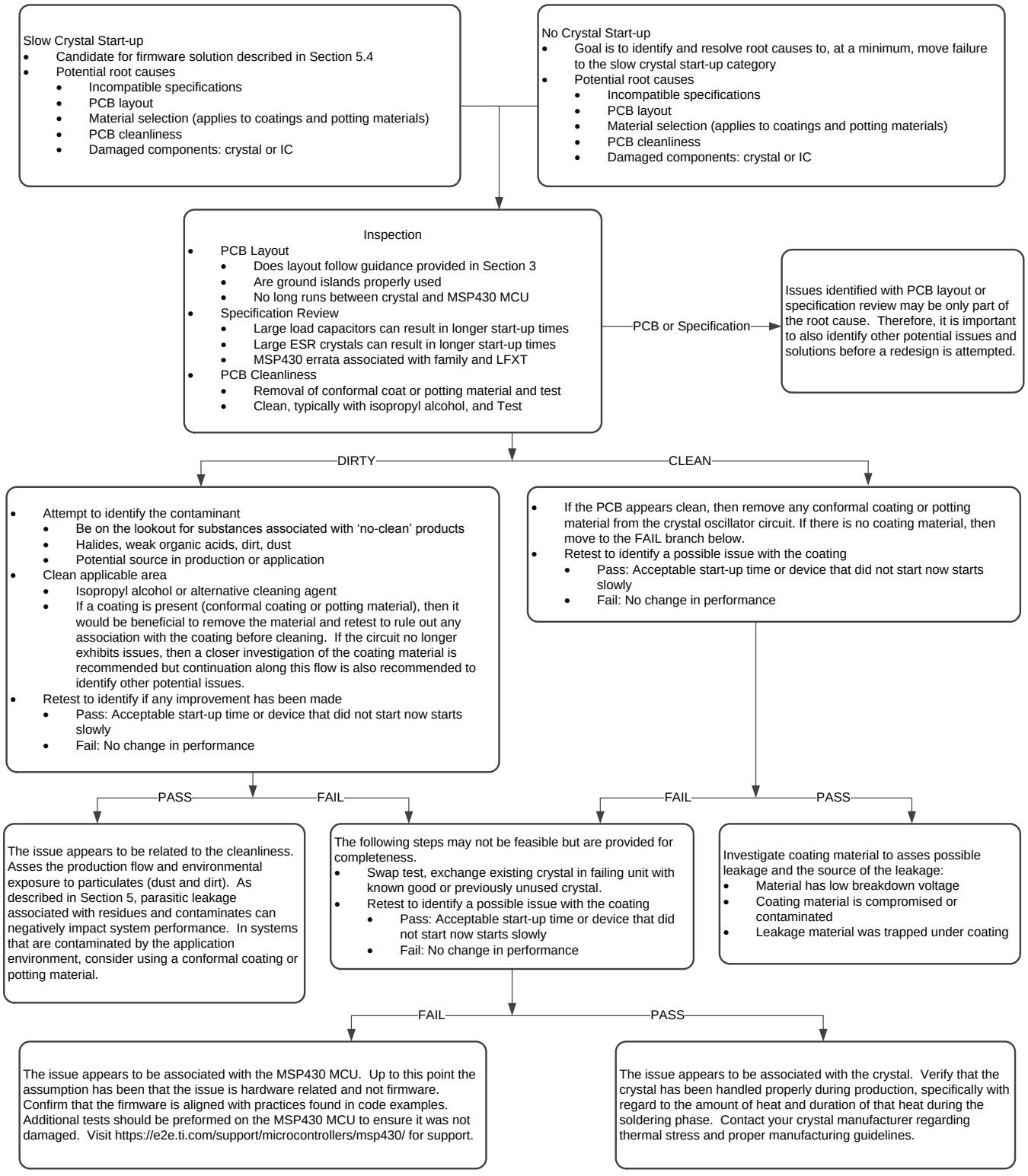


Figure 13. LFXT Troubleshooting Decision Tree

7 References

1. *MSP430FR4xx and MSP430FR2xx Family User's Guide*
2. *MSP430x2xx Family User's Guide*
3. *MSP430F2272 Device Erratasheet*
4. *MSP430F4152 Device Erratasheet*
5. *MSP430F413 Device Erratasheet*
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10. "Selection of Wave Soldering Fluxes for Lead-Free Assembly", Shea, Arora, Brown, APEX, Los Angeles, CA, Jan. 2007

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from June 30, 2016 to July 18, 2017	Page
• Added the last row "FC-135R 32.7680KA" in Table 3, *Safety Factor Test Results*	12

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